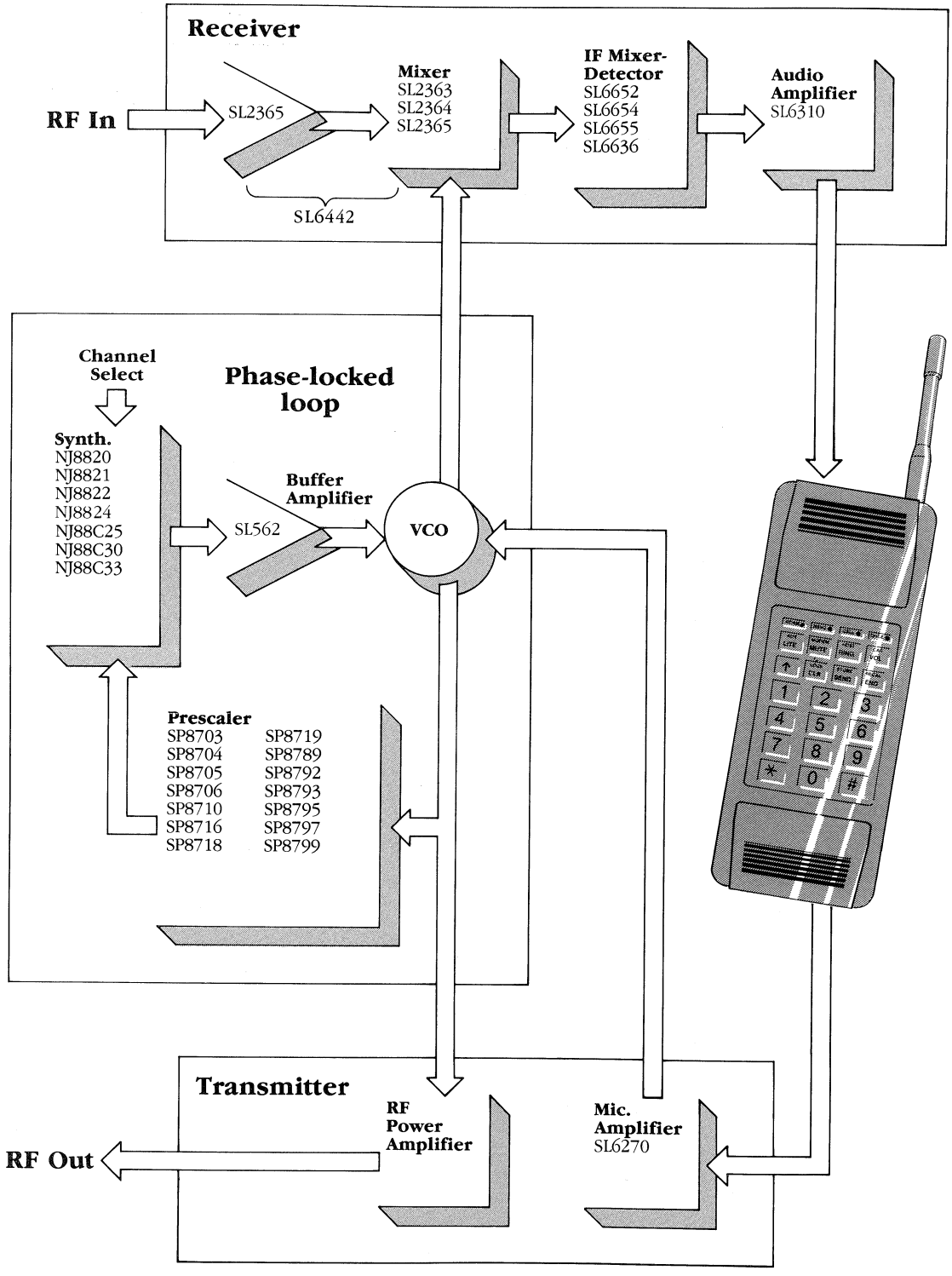
Personal Communications

IC Handbook

PLESSEY
SEMICONDUCTORS



Plessey products in a typical hand held radio.

PERSONAL COMMUNICATIONS

IC Handbook

PLESSEY
SEMICONDUCTORS

Foreword

Plessey Semiconductors has created a range of products specific to applications in the growing market for hand-held radio-communications.

The features which identify ICs as being suitable for this market area are *supply current* and *frequency*. Since battery life is all-important in hand-held equipment, every effort is made by our IC designers to develop products which require the absolute minimum current. New ICs such as the SL6639 pager chip and SP8705 (a programmable multi-modulus divider, which consumes only 5mA at 1000MHz) exemplify this philosophy.

New frequency band allocations have now been made in the 450 and 900MHz regions for pagers, cordless telephones and cellular radios. Plessey's bipolar processes have been developed to operate at these and even higher frequencies for dividers, IF amplifiers and single chip synthesisers. The 1.4-Micron CMOS process is also capable of operating at high frequencies and the latest generation of CMOS synthesisers are included in this handbook.

Also making its debut is a range of new low power FM receivers. Suited for use in paging, the new ICs offer ideal solutions for Direct Conversion or Superhet front ends.

All the relevant Plessey ICs can be supplied in surface mount miniature plastic and some in plastic quad packages in order to satisfy the requirement for small size in compact hand-held radio equipment.

Finally, the Quality Assurance Procedures that are applied to other Plessey Semiconductor products (from consumer electronics to Defence projects) are applied to radio-communications ICs with equal rigour. Performance and long term reliability are thereby guaranteed in what can be a demanding operating environment.

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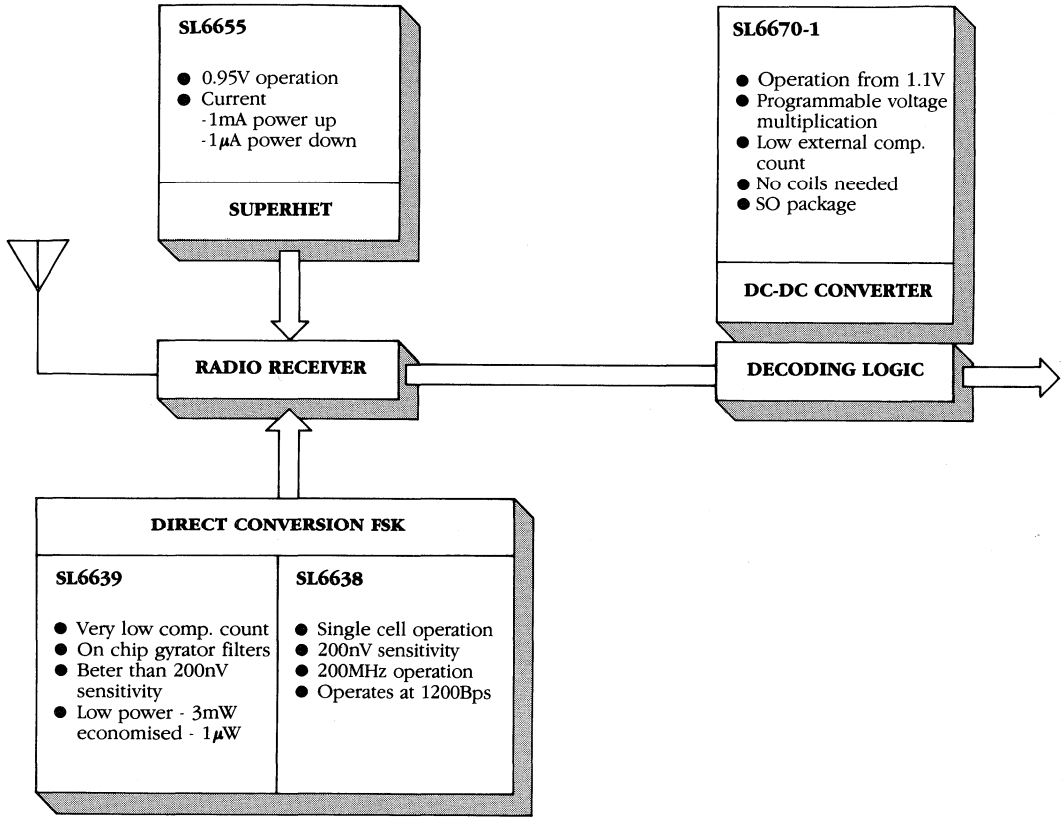


The Plessey pager solution

Product index - by application

Dividers

Ratio	Frequency (MHz)	Supply Current (mA,max)	Supply Voltage (V)	Type No.	Page
10/11	225	7	5.2 or 6.8 to 9.5	**SP8799**	141
20/21	225	7	5.2 or 6.8 to 9.5	**SP8789**	129
32/33	225	7	5.2 or 6.8 to 9.5	**SP8795**	135
32/33	225	7.8	4.5 to 9.5	**SP8797**	138
40/41	225	7	5.2 or 6.8 to 9.5	**SP8793**	132
40/41	520	10.5	5.2	**SP8716**	126
64/65	950	10	3 to 5	**SP8704**	117
64/65	1100	5	3 to 5	**SP8705**	119
64/65	520	10.5	5.2	**SP8718**	126
80/81	225	7	5.2 or 6.8 to 9.5	**SP8792**	132
80/81	520	10.5	5.2	**SP8719**	126
80/81	1000	10	3 to 5	**SP8706**	121
100/101	225	8.5	3 to 10	**SP8710B**	123
128/129	950	10	3 to 5	**SP8704**	117
128/129	1000	30	5	**SP8703**	114
128/129	1100	5	3 to 5	**SP8705**	119

Synthesisers

Input Frequency (MHz)	Supply Current (mA)	Supply Voltage (V)	Type No.	Page
10	3.5	5	**NJ8820/B**	144
10	3.5	5	**NJ8820GG**	151
10	3.5	5	**NJ8821GG**	162
10	6.3	5	**NJ8822/B**	167
10	3.5	5	**NJ8823/B**	172
10	6.3	5	**NJ8824/B**	177
20		3 to 5	**NJ88C25**	182
100	4	3 to 5	**NJ88C33**	269
200	4	5	**NJ88C30**	188

IF Amplifiers/Detectors

Input Frequency (MHz)	Supply Current (mA)	Supply Voltage (V)	Type No.	Page
100	1.5	2.5 to 7.5	**SL6652**[1]	77
100	1.5	2.5 to 7.5	**SL6653**[2]	85
100	1.5	2.5 to 7.5	**SL6654**[3]	90

1. With RSSI output and differential audio outputs. 2. Single audio output, no RSSI.
3. RSSI output, single audio output.

Low Power Radio Receivers (Pagers)

Input Frequency	Supply Current (mA)	Supply Voltage (V)	Type No.	Page
455kHz	2.3	7	**SL6601C**	47
100MHz	1.0	0.95 to 5	**SL6655**	96
200MHz	2.5	0.9 to 3.5	**SL6637**[1]	60
200MHz	2	0.9 to 3.5	**SL6638**	61
200MHz	2	0.9 to 3.5	**SL6639**	70
N/A	0.25	1.1 to 5	**SL6670-1**	279
455kHz		6	**SL6691C**	111

1. Not recommended for new designs; use SL6638 or SL6639.

Cordless Telephones

Input Frequency (MHz)	Supply Current (mA)	Supply Voltage (V)	Type No.	Page
N/A	4.5	5	**SL6636**	**53**
1000	4.1	4.5 to 6.5	**SL6442**	**43**

UHF Transistor Arrays

f_T (GHz)	Supply Current (mA)	Supply Voltage (V)	Type No.	Page
5	4	2.0	**SL2363C & SL2364C**[1]	29
5	4	2.0	**SL2365**[2]	31

1. 2 long-tailed pairs with tail transistors. 2. Two long tailed pairs with current mirrors.

Amplifiers

Function	Supply Current	Supply Voltage (V)	Type No.	Page
Audio	7.5mA	4.5 to 13	**SL6310C**	40
Microphone	10mA	4.5 to 10	**SL6270**	37
Op-amp	20mA	±1.5 to ±10	**SL562**	26
300MHz low noise amplifier	40μA[1]	2 to 5	**SL560C**	21

Product index - by circuit type (contd.)

Amplifiers

Type No.	Supply Voltage (V)	Supply Current	Bandwidth	Maximum Offset Voltage (mV)	Gain (dB)	Page
SL560C[1]	2 to 15V	20mA	300MHz	-	35	21
SL562[1]	±1.5 to +10	20μA to 5mA	50kHz to 4MHz	5	95	26
SL6310C	4.5 to 15V	15mA	1MHz	20	50	40

1. Noise figure 20nV/√Hz (Guaranteed)

Matched Transistors and Arrays

Type No.	LV_{CEO}(V) Min.	LV_{CEO}(V) Typ.	I_{CM}(mA)	Typ.Cut-off Frequency (GHz)	No. of Transistors	h_{FE} (I_C = 1mA) (Min.)	Page
SL2363C[1]	6	9	12	5.0	6	20	29
SL2364C[2]	6	9	12	5.0	6	20	29
SL2365[3]	6	9	12	5.0	8	20	31

1. TO-5 package (CM10) 2. DIL package (DC14,DP14). 3. Plastic DIL surface mount package (MP14).

Radiocoms

Type No.	Function	Page
SL6270C	Microphone amplifier with AGC	37
SL6652	FM IF and quadrature detector with RSSI and differential audio O/P	77
SL6653	FM IF and quadrature detector	85
SL6654	FM IF and quadrature detector with RSSI	90

Low Power Radio Receivers (Pagers)

Type No.	Function	Page
SL6601C	FM IF, PLL detector (double conversion) and RF mixer	47
SL6637	Direct conversion FSK receiver - not recommended for new designs	60
SL6638	Direct conversion FSK receiver	61
SL6639	Direct conversion FSK receiver with on chip filter	70
SL6655	Superhet receiver consuming 1mA at 0.95V	96
SL6670-1	Low power voltage multiplier (inverter)	279
SL6691C	FM IF and detector (455kHz only)	111

Cordless Telephones

Type No.	Function	Page
SL6636	Baseband receiver chip	53
SL6442	RF front end low noise amp with two mixers	43

SP8000 Series Variable Modulus Dividers - Bipolar

Type No.	Function	Supply Current (Typ.) (mA)	Page
SP8703	1GHz ÷ 128/129	20	114
SP8704	950MHz ÷ 128/129 64/65	10	117
SP8705	1100MHz ÷ 128/129 64/65	4	119
SP8706	950MHz ÷ 80/81	10	121
SP8710	225MHz ÷ 100/101	7	123
SP8716	520MHz ÷ 40/41	7	126
SP8718	520MHz ÷ 64/65	7	126
SP8719	520MHz ÷ 82/81	7	126
SP8789	225MHz ÷ 20/21	4	129
SP8792	225MHz ÷ 80/81	4	132
SP8793	225MHz ÷ 40/41	4	132
SP8795	225MHz ÷ 32/33	4	135
SP8797	225MHz ÷ 32/33		138
SP8799	225MHz ÷ 10/11	4	141

Radio Synthesisers

Type No.	Function	Page
NJ8820/B	CMOS control circuit with PROM interface	144
NJ8820GG	Flatpack version of **NJ8820**	151
NJ8821/B	CMOS control circuit with microprocessor parallel interface and resettable counters	157
NJ8821GG	Flatpack version of **NJ8821**	162
NJ8822/B	CMOS control circuit with microprocessor serial interface and resettable counters	167
NJ8823/B	As **NJ8821** with zero reset removed	172
NJ8824/B	As **NJ8822** with zero reset removed	177
NJ88C25	3V control circuit with microprocessor serial interface	182
NJ88C30	200MHz single chip synthesiser for General Application	188
NJ88C33	I²C interface 120MHz single chip synthesiser	269

Purchase of Plessey Semiconductors' I²C components conveys a licence under the Philips I²C Patents Rights to use these components in I²C systems, provided that the systems conform to the I²C Standard Specification as defined by Philips.

Product list - alpha numeric

TYPE No.	DESCRIPTION	PAGE
SL560C	300MHz low noise amplifier	21
SL562	Low noise programmable op-amp	26
SL2363C	Very high performance transistor array	29
SL2364C	Very high performance transistor array	29
SL2365	Very high performance transistor array	31
SL6140	400MHz wideband AGC amplifier	32
SL6270C	Gain controlled pre-amplifier	37
SL6310C	Switchable audio amplifier	40
SL6442	1GHz amplifier/mixer	43
SL6601C	FM IF, PLL detector (double conversion) and RF mixer	47
SL6636	Low power baseband demodulator for digital cordless telephones	53
SL6637	Direct conversion FSK receiver	60
SL6638	200MHz direct conversion FSK data receiver	61
SL6639	200MHz direct conversion FSK data receiver	70
SL6652	Low power IF/AF circuit for FM cellular radio	77
SL6653	Low power IF/AF circuit for FM receivers	85
SL6654	Low power IF/AF circuit for FM cellular radio	90
SL6655	Superhet receiver	96
SL6670-1	1.1V DC/DC voltage converter	279
SL6691C	IF system paging receivers	111
SP8703	1GHz low current divide by 128/129	114
SP8704	950MHz very low current divide by 128/129 or 64/65	117
SP8705	1100MHz very low current divide by 128/129 or 64/65	119
SP8706	950MHz very low current two-modulus divider	121
SP8710B	225MHz low power two-modulus divide by 100/101	123
SP8716	520MHz divide by 40/41	126
SP8718	520MHz divide by 64/65	126
SP8719	520MHz divide by 80/81	126
SP8789	225MHz divide by 20/21	129
SP8792	225MHz divide by 80/81	132
SP8793	225MHz divide by 40/41	132
SP8795	225MHz divide by 32/33	135
SP8797	225MHz divide by 32/33	138
SP8799	225MHz divide by 10/11	141
NJ8820/B	Frequency synthesiser (PROM interface)	144
NJ8820GG	Flatpack version of NJ8820	151
NJ8821/B	Frequency synthesiser (Microprocessor interface)	157
NJ8821GG	Flatpack version of NJ8821	162
NJ8822/B	Frequency synthesiser (Microprocessor serial interface)	167
NJ8823/B	Frequency synthesiser (Microprocessor serial interface)	172
NJ8824/B	Frequency synthesiser (Microprocessor serial interface)	177
NJ88C25	Frequency synthesiser at 3V (Microprocessor serial interface)	182
NJ88C30	Single chip VHF synthesiser	188
NJ88C33	Single chip I²C synthesiser	269

Semi-Custom design

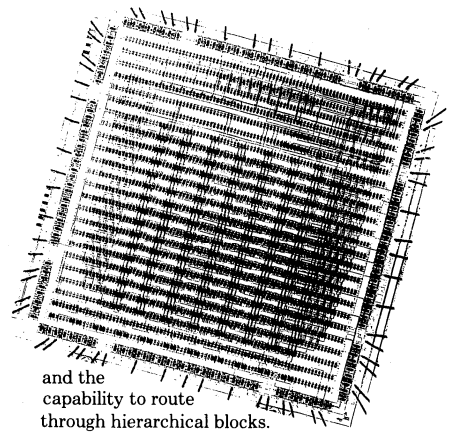
CMOS gate arrays

PLESSEY Semi Custom CMOS

• CLA SERIES •

The CLA 5000 family is a 2μm, 40 MHz, double layer metal CMOS product. There are 9 arrays ranging from 640 to 10044 gates.

Like all of our CMOS, the 2μm arrays use stacked vias over contacts, routing through cells and the capability to route through hierarchical blocks. All of these features have a direct impact on the utilisation and chip density of each array. 85 to 90% utilisation figures are normally achieved.



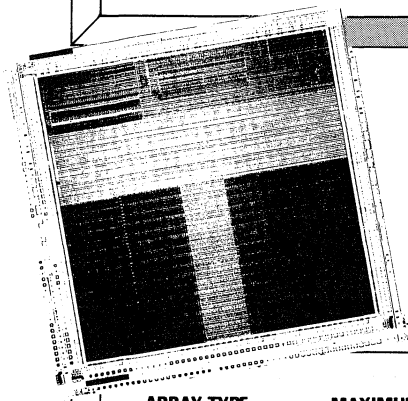
ARRAY TYPE	MAXIMUM GATES	MAXIMUM I/O	POWER PINS
CLA 51XX	640	36	4
CLA 52XX	1232	48	8
CLA 53XX	2016	64	8
CLA 54XX	3060	80	8
CLA 55XX	4408	96	16
CLA 56XX	5984	112	16
CLA 57XX	7104	128	16
CLA 58XX	8064	144	16
CLA 59XX	10044	160	16

CLA 5000 Features

- 2μm CMOS, DLM process
- 1.2 ns (typ), 2 input gate delay
- 40 MHz clock frequency
- 160 I/Os with TTL/CMOS compatibility
- Intrinsic latch-up immunity and over-voltage protection
- 3V to 5.5V operating range
- Full military spec (-55 to 125°C)
- 5μW/Gate/MHz power consumption

In the corners of each gate array, special circuit configurations have been included. A power-on reset circuit, crystal oscillator maintaining circuit, performance monitor and a bandgap reference circuit are currently available.

High density RAM and ROM configuration can also be programmed onto the arrays.



CLA 60000 1.4μm CMOS Channelless Arrays

New to the Plessey Semiconductors gate array family is the 1.5μm CMOS "CHANNELLESS ARRAY".

The "CHANNELLESS ARRAY" technique combines the advantages of gate arrays with the full layout flexibility of cell based designs.

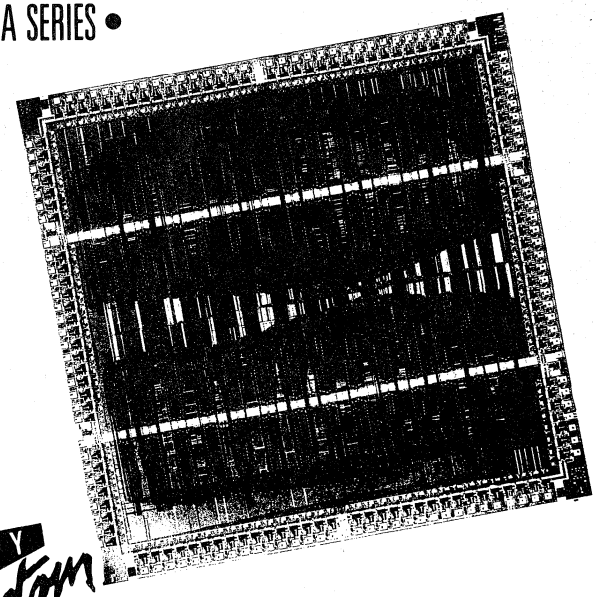
ARRAY TYPE	MAXIMUM GATES	TOTAL PADS
CLA 61XXX	2040	40
CLA 62XXX	5488	64
CLA 63XXX	10608	88
CLA 64XXX	19928	120
CLA 65XXX	35784	160
CLA 66XXX	55616	200
CLA 67XXX	80560	240
CLA 68XXX	110112	256

CLA 60000 Features

- 1.4μm CMOS, DLM process
- All pads may be programmed as Input, Output, I/O or Power
- 700 ps (typ), 2-input gate delay
- 5.5μW/Gate/MHz power consumption
- 70 MHz clock frequency
- 5 volt full military specification (-55 to 125°C)
- Analog functions available (op amp, comparator)

Bipolar gate arrays

•ULA SERIES•



All ULA products are designed to provide cost-effective solutions to a wide range of applications.

The DS series of bipolar digital arrays feature fast internal gates and differential logic functions for superior speed/power performance. These provide predictable and closely matched delays for system speeds of 100MHz at complexities to 10,000 gates. Easy interfacing to ECL, TTL and CMOS logic is combined with on-chip analog functions such as oscillators, comparators, schmitt triggers and operational amplifiers.

PLESSEY *SemiCustom* ULA

DS' SERIES

HIGH SPEED DIGITAL ARRAYS WITH HIGH PERFORMANCE ANALOG

ARRAY TYPE	EQUIVALENT GATE COUNT	PERIPHERAL I/O CELLS	BOND PADS
ULA 6DS	630	32	40
ULA 12DS	1210	44	52
ULA 19DS	1870	64	72
ULA 25DS	2550	74	82
ULA 32DS	3230	82	92
ULA 38DS	3990	90	100
ULA 47DS	4860	104	114
ULA 60DS	6210	122	132
ULA 80DS	7920	138	150
ULA 100DS	10000	138	150

DIGITAL ARRAYS WITH ANALOG FUNCTIONS

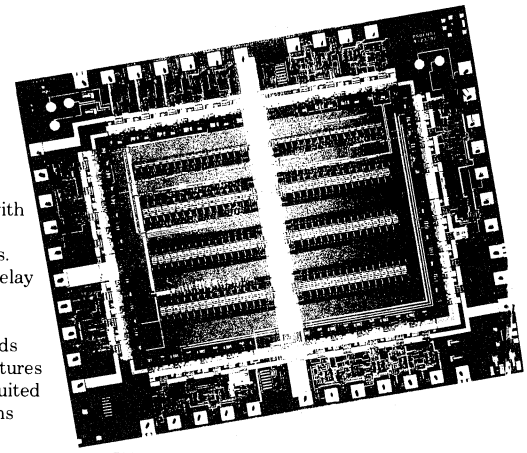
ULA DS series

- 100 MHz system speed
- Complexities to 10,000 gates
- 1.5 micron DLM process
- High performance analog functions on chip
- Good asynchronous performance
- Flexible interface capability
- Differential logic for superior speed/power product
- Closely matched components
- Silicon compilers
  48mA output drive per peripheral cell
- Digital & linear macros
- Comprehensive CAD support
- Range of speed/power options
- Full military operation

Bipolar analog/digital arrays

PLESSEY Semi Custom ULA

DF series arrays feature enhanced analog capabilities alongside the logic gates from the DS series. The 37 high performance linear components in each analog cell – and there are up to 58 cells – are designed to guarantee close matching and low offsets. These are optimised for producing 100MHz VCOs or crystal oscillators together with precision AGC amplifiers featuring 60MHz bandwidths. Comparators offering 10ns delay and only 1mV offsets are complemented by precision monostables with 20ns periods accurate to 500ps. These features make the DF series ideally suited to a wide range of applications such as data recovery in the computer peripherals and telecommunications fields.



'DF' SERIES

HIGH SPEED DIGITAL WITH ENHANCED ANALOG FUNCTIONS

ARRAY TYPE	EQUIVALENT GATE COUNT	ANALOG CELLS	BOND PADS
ULA 5DF	560	32	43
ULA 11DF	1100	44	55
ULA 14DF	1430	54	65
ULA 18DF	1725	58	69

'DA' SERIES

2 DA	20	6	18
8 DA	80	10	22
18 DA	176	14	26
25 DA	256	18	30
35 DA	352	18	34
50 DA	512	22	36
90 DA	924	32	44
150 DA	1428	40	52

The DA series combines complex analog and digital circuits allowing the integration of full systems on a single chip. The series is fully supported for customer designs using the Plessey advanced benchtop prototype modelling system allowing evaluation and verification of the design prior to silicon.

The chip architecture uses a central core of digital gates to implement the logic, surrounded by standard analog cells, for the analog and I/O functions characterised as an extensive range of macros. Each corner cell includes special components such as a voltage regulator, low offset and high current transistors, band gap reference and banks of closely matched resistors.

ULA DF series

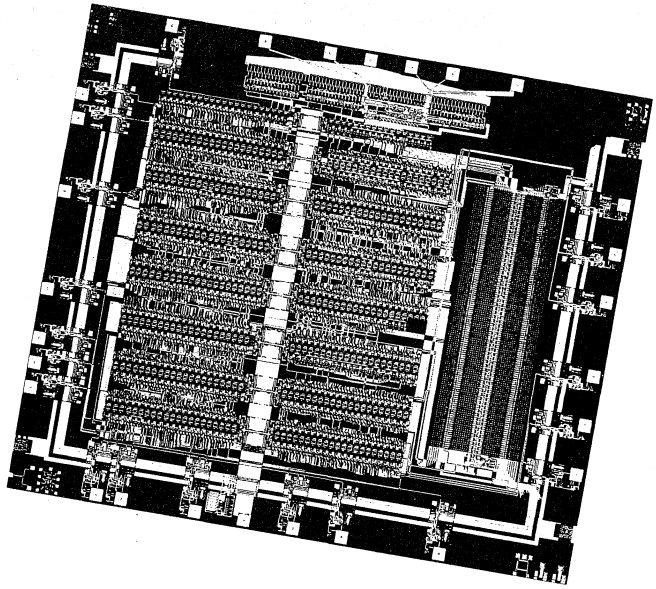
- 100MHz digital system speed
- 100MHz analog capability
- Close matching cell components
- Low offsets
- Digital and analog macros
- Complexities to 2000 gates
- Speed/power options
- Differential logic
- On chip bandgap reference
- 50mA drive capability
- Fully CAD supported
- Silicon compilers
- 1.5 micron feature size
- Full military operation

DA Series Features

- Combines complex analog and digital circuitry on a single chip
- NPN & PNP transistors allowing comprehensive analog designs
- Operation from 1 to 18 volt supply
- High current drive capability (120mA)
- Two gate switching speed options
- Fully supported customer design route
- Extensive range of analog and logic macros
- Proven hard analog macros in silicon
- Auto place and route
  Rapid physical turnaround to silicon
- Available to commercial, industrial & military requirements

Plessey compiled ASIC

• SYSTEMS IN SILICON •



An example of the implementation of a Compiled ASIC solution to a system integration is shown in the photograph.

The circuitry combines 4 and 8-bit converters and high linearity VCOs with counters, adders, interface logic and high access speed ROM and drivers together with on-chip voltage regulation.

PLESSEY
Semi Custom
COMPILED
ASIC

The Plessey Compiled ASIC is a technique developed through advances in CAE/CAD and the continuous development of Advanced Bipolar Process L. It allows the integration of complete systems, combining proven high performance analog, digital and memory functions. It is based on a single process technology.

Silicon compilation is used to design and optimise the digital sections of the chip and macros based on proven high performances off-the-shelf standard products provide the analog functions.

A comprehensive function/macrofunction CAD supported library is available. This library is separated into three different areas, logic, memory and analog and interface.

Plessey Compiled ASICs offer the benefits of greater cost effectiveness – via increased levels of integration, reduced inter-chip delays, and reduced noise and interference, with no compromise in performance, together with development timescales which allow faster entry into the market for the end product. To these benefits must be added the attributes of Process L, in respect of speed, analog performance, including accuracy and flexibility of I/O, and off-chip drive capability.

The basic analog and digital performance capability of the Compiled ASIC currently includes such features as:

Digital system speeds of up to 200MHz

Sub nanosecond gate delays

- A to D and D to A converters to 10 bit resolution
- Oscillators and Amplifiers up to 250MHz/250mW
- Comparators and Voltage references
- Control and bus drive interface protocol circuits
- High speed systolic array digital multipliers
- ROM to 8K bits with access times to 5ns
- RAM to 2K bits with access time to 5ns
- Output drive capability to a few hundred mA

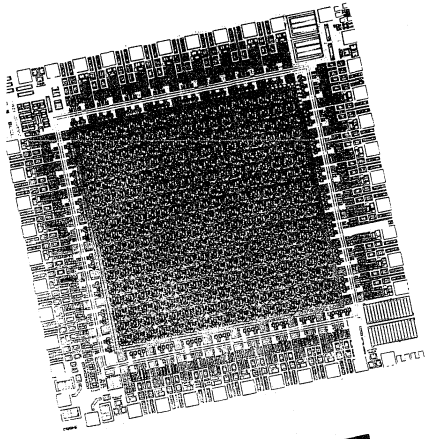
Key to the performance of Compiled ASIC is Process L. This technology offers minimum feature sizes of 1.5 microns and double layer metal with pitches on both layers of 6 microns.

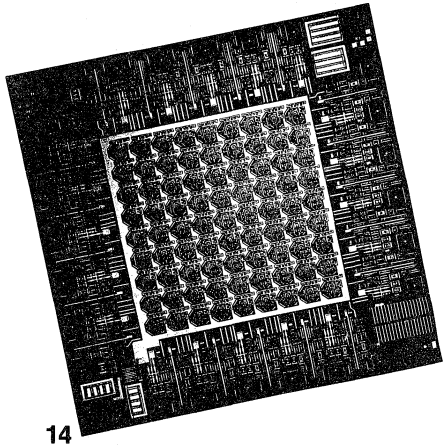
Bipolar analog/digital arrays

PLESSEY Semi Custom DIGILIN

•DIGILIN™•

The DIGILIN array series combines high performance analog and digital functions on the same chip. The chips contain a core of Matrix cells, for implementing logic, surrounded by peripheral cells, for analog and I/O functions. Special components are located in the chip corners





'P' SERIES DIGILIN ARRAYS

ARRAY TYPE	LOGIC GATE COUNT	ANALOG CELL COUNT	ANALOG NPN COUNT	BOND PADS
1P	128	16	128	26
2P	208	20	160	30
3P	338	24	192	34
4P	442	28	224	38
6P	578	32	256	42
9P	882	40	320	50
11P	1152	44	352	54

'G' SERIES DIGILIN ARRAYS

ARRAY TYPE	LOGIC GATE COUNT	ANALOG CELL COUNT	ANALOG NPN COUNT	BOND PADS
03G	30	10	120	18
1G	98	16	192	24
2G	162	20	240	28
3G	242	24	288	32
4G	338	28	336	36
5G	450	32	384	40
6G	578	35	420	44

such as: a band gap reference, high current transistors, capacitors and banks of closely matched resistors. Typical analog functions include Schmitt triggers, regulators, comparators, op-amps, monostables, oscillators, ceramic resonators, white noise sources, peak reading circuits, data converter functions.

Features:

- Digital and analog circuitry on a single chip.
- Operation from 1 to 15 volt supply. (12 volts on 'G' Series)
- High current drive capability (250mA 'G' Series, 120mA 'P' Series).
- Complete system integration capability.
- Reduced system space and power
- Rapid development time.

The 'P' and 'G' series of Digilin arrays both have 7 arrays of varying complexity. The G series is intended for analog dominated systems with 50% of the chip devoted to analog and I/O functions. The P series has a higher digital content with 75% of the chip allocated to the digital matrix.

Peripheral transistors have a typical gain of 150 which is flat over 8 current decades. Matching is typically 1%.

High performance analog designs are accomplished using the tight matching of the peripheral active and passive components. Precharacterised analog macros and full CAD simulation support gives a complete design environment for total system integration.

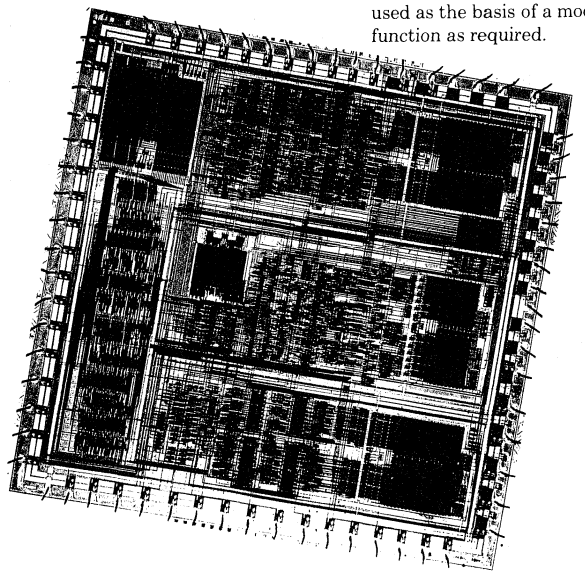
Plessey MEGACELL™

•SYSTEMS IN SILICON•

The MEGACELL approach provides a cell-based design methodology for high-efficiency CMOS designs. All cells are committed (unlike gate arrays) so in general more complex designs are possible. Plessey MEGACELL is very suitable for integrating up to full-custom complexity, without the long development timescales and high costs associated with full-custom. Fast circuit development is possible by using the Plessey Design System (PDS2) linked to the MEGACELL design libraries.

Plessey Megacell is available in both 2 micron and 1.4 micron technologies. These are designated MVA 5000 series and MVA 60000 series respectively and allow circuits of up to 35,000 gate equivalents to be realised on MVA 5000 and 80,000 on MVA 60000.

MEGACELL libraries provide functional, dynamic and physical models of a wide range of functions, both analog and digital. These cells range from simple logic functions (microcells) to complex parameterisable functions (Paracells) and complex standard functions (Supracells).



Cell Library Types

For both Gate Arrays and MEGACELL designs, Plessey Semiconductors classifies library cells into groups. Every cell is supported by a logical design model, which includes all relevant data for the software design tools (eg, testability, functional and timing data), plus a physical design model for the software layout (eg, cell boundaries, pin nodes, routing areas). The cell groups are as follows:-

Microcells

Microcells are the simplest cells in the library. They are similar in function and complexity to those available in 74 series TTL and 4000 series CMOS standard products and include basic logic gates such as NAND, NOR, D-type flip-flops, etc.

Macrocells

Macrocells are the next level in the hierarchy of cells and have been designed using microcells. Plessey Macrocells comprise a collection of the larger functions most used in the 74 series TTL and 4000 series CMOS MSI products. A full cell-list description of these macrocells is provided to the user and may be changed and used as the basis of a modified function as required.

PLESSEY Semi Custom MEGA CELL

Some of the advantages of using macrocells over building circuit functions up from microcells are:

- Shorter design time – large functions need not be designed from scratch;
- Designers can use more familiar MSI design blocks;
- Some circuits can be translated directly from breadboards built from standard TTL/CMOS parts.

Supracells

Supracells are equivalent to large complex functions, which again have their own specific logical and physical design models for the software design tools.

These cells include complex multipliers, DSP functions, bit slice processors etc.

Paracells

Paracells are medium to large scale cells which are algorithmically generated by the PDS2 software from simple descriptions entered by the designer.

Functions available as Paracells include RAM, ROM, PLA, Register Files, Multipliers and ALUs.

In the case of RAM, for example, the user simply specifies the address length, the word length and the number of words, as a one line command to PDS2. The software then compiles both the simulation model and the physical models of the required memory, working only from this simple instruction.

Analog Functions

Appreciating that in real applications both digital and analog functions must interface to each other, the MEGACELL library supports a range of analog functions, including:-

- Op Amps
- Comparators
- R-C Oscillators
- ADC and DAC functions.
- Capacitive and Resistive elements.

The Quality Concept

Quality cannot be inspected into a product; it is only by careful design and evaluation of materials, parts and processes (followed by strict control and ongoing assessment) that quality products will be produced.

All designs conform to standard layout rules, all processes are thoroughly evaluated and all new piece part designs and suppliers are investigated before authorisation for production use.

The same basic procedures are used on all products up to and including device packing. It is only then that extra operations are performed for certain customers in terms of lot qualification or release procedure.

By working to common procedures all users benefit; the high reliability user gains the advantage of scale hence improving the confidence factor in the quality achieved, whilst the volume user gains the benefits of basic high reliability design concepts.

Plessey Semiconductors have the following factory approvals:

BS9300 and **BS9400** (BSI Approval No. 1053/M).

CECC50000 and **CECC90000** (Reg. No. M/0020/CECC/UK-1053/M).

DEF-STAN 05-21 (DCL Reg. No. 1SB PO1).

Plessey Semiconductors conforms to **MIL-M-38510F** and is qualified to supply to **MIL-STD-883C.**

Screening

Different screening procedures are carried out by Plessey Semiconductors Limited, a brief description of the differences involved are explained in the next few pages.

Stage/Operation	PLESSEY HI-REL CLASS B (References are to MIL-STD-883C)	MIL-STD-883C CLASS B Method 5004
Internal Visual	Method 2010 Test Condition B 100%	Method 2010 Test Condition B 100%
Stabilisation Bake	Method 1008 24 Hrs at Condition C 100%	Method 1008 24 Hrs at Condition C 100%
Temperature Cycling	Method 1010 Test Condition C 100%	Method 1010 Test Condition C 100%
Constant Acceleration	Method 2001 Test condition E Y1 only. 100%	Method 2001 Test Condition E Y1 only. 100%
Visual Inspection	-	100 %
Initial Electrical	Those parameters requiring Delta calculations. 100%	Those parameters requiring Delta calculations. 100%
Burn-In	Method 1015 160 Hrs at 125 °C min. 100%	Method 1015 160 Hrs at 125 °C min. 100%
Post Burn-In Electrical Test	Full Electrical Test to guarantee Data Sheet. 100%	Those parameters requiring Delta Calculations. 100%
PDA Calculation	5 % max. All lots.	5 % max. All lots.
Final Electrical Test	Done as Post Burn-in Test 100%	Full Group A tests as Method 5005 100%
Seal (a) Fine Seal (b) Gross	Method 1014 100%	Method 1014 100%
Qualification/Quality Conformance Test	-	Method 5005 Class B Samples as necessary
External Visual	Plessey Spec. sample	Method 2009 100%

Stage/ Operation	Standard Product	Plessey Hi-Rel B	MIL-STD-883C Class B	MIL-STD-883C Class S	BS9400 Level S2
Coding (example)	SPxxxxA	SPxxxxAB	SPxxxxAC	SPxxxxAS	SPxxxxABSS2
Wafer-fab				Wafer-lot accept Method 5007	
Probe test	100 %	100 %	100 %	100 %	100 %
Visual inspect chips	Usually 2010 Cond B	2010 Cond B	2010 Cond B	2010 Cond A	BS9400 1.2.10 Cond B
Assemble				Includes 100 % bond pull	
Screen	None	As list attached	Method 5004 Class B	Method 5004 Class S	BS9400 1.2.9 Level B
Test	100 %	100 %	100 %	100 %	100 %
Conformance testing	None	None	Method 5005 Class B Group A Group B Group C Group D	Method 5005 Class S Group A Group B Group D	BS9400 Group A Group B Group C Group D
Ship					

NOTES
1. Visual inspection BS9400 1.2.10 Cond B is equivalent to MIL-STD-883 Method 2010 Cond B.
2. Screening BS9400 1.2.9 Level B is equivalent to MIL-STD-883 Method 5004 Class B EXCEPT it does not include 100% hot and cold test.
3. Conformance testing BS9400 is similar to MIL-STD-883 Class B EXCEPT:
   Group A does not necessarily include hot and cold testing.
   Group B does include 160 hour operating life test.
   Group C does include 2000 hour operating life test and hot and cold testing.
   Group D only usually includes 8000 hour life test and dimension checks.

Technical Data

PLESSEY
Semiconductors

SL560C

300MHz LOW NOISE AMPLIFIER

This monolithic integrated circuit contains three very high performance transistors and associated biasing components in an eight-lead TO-5 package forming a 300MHz low noise amplifier. The configuration employed permits maximum flexibility with minimum use of external components. The SL560C is a general purpose low noise, high frequency gain block.

The device is also available as the SL560AC which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883C Class B. Data is available separately.

FEATURES

- Gain up to 40dB
- Noise Figure less than 2dB (Rs 200 ohm)
- Bandwidth 300MHz
- Supply Voltage 2-15V (Depending on Configuration)
- Low Power Consumption

APPLICATIONS

- Radar IF Preamplifiers
- Infra-Red Systems Head Amplifiers
- Amplifiers in Noise Measurement Systems
- Low Power Wideband Amplifiers
- Instrumentation Preamplifiers
- 50 ohm Line Drivers
- Wideband Power Amplifiers
- Wide Dynamic Range IF Amplifiers
- Aerial Preamplifiers for VHF TV and FM Radio

ABSOLUTE MAXIMUM RATINGS

Supply voltage (Pin 4)	+15V
Storage temperature	-55°C to 150°C (CM) -55°C to 125°C (DP)
Junction temperature	150°C (CM) 125°C (DP)
Thermal resistance	
Junction-case	60°C/W (CM)
Junction ambient	220°C/W (CM) 230°C/W (DP)
Maximum power dissipation	See Fig.15
Operating temperature range	-55°C to +125°C (CM) at 100mW -55°C to +100°C (DP) at 100mW

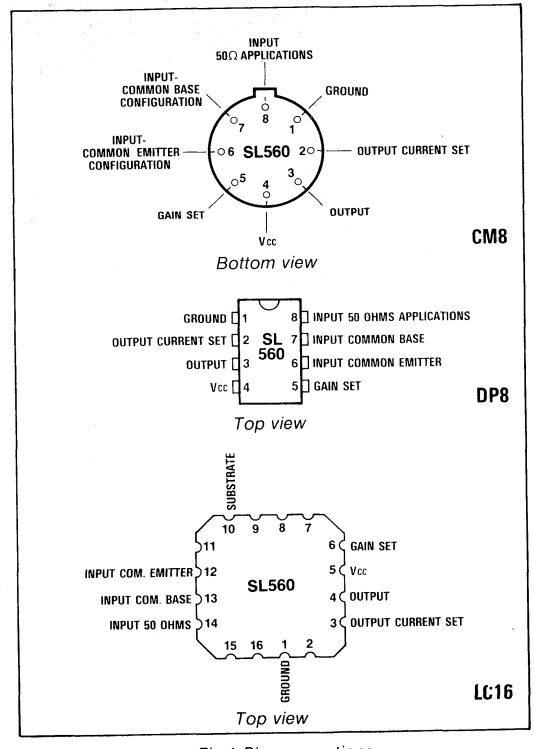


Fig.1 Pin connections

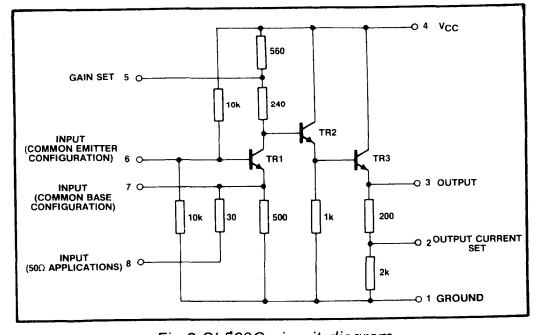


Fig.2 SL560C circuit diagram

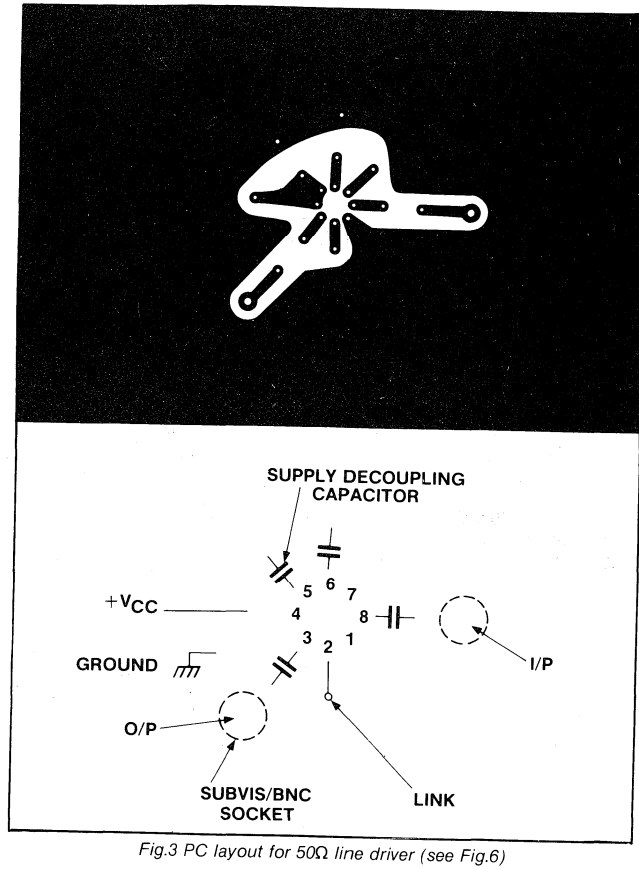


Fig.3 PC layout for 50Ω line driver (see Fig.6)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Frequency = 30MHz; V_{CC} = 6V; $R_S = R_L$ = 50Ω; T_{amb} = 25°C; Test Circuit: Fig.6

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Small signal voltage gain	11	14	17	dB	
Gain flatness		±1.5		dB	10MHz - 220MHz
Upper cut-off frequency		250		MHz	
Output swing	+5	+7		dBm	V_{CC} 6V } See Fig.5
		+11		dBm	V_{CC} = 9V }
Noise figure (common emitter)		1.8		dB	R_S = 200Ω
		3.5		dB	R_S = 50Ω
Supply current		20	30	mA	

CIRCUIT DESCRIPTION

Three high performance transistors of identical geometry are employed. Advanced design and processing techniques enable these devices to combine a low base resistance ($R_{bb'}$) of 17Ω (for low noise operation) with a small physical size - giving a transition frequency, f_T, in excess of 1GHz.

The input transistor (TR1) is normally operated in common base, giving a well defined low input impedance. The full voltage gain is produced by this transistor and the output voltage produced at its collector is buffered by the two emitter followers (TR2 and TR3). To obtain maximum bandwidth the capacitance at the collector of TR1 must be minimised. Hence, to avoid bonding pad and can capacitances, this point is not brought out of the package. The collector load resistance of TR1 is split, the tapping being accessible via pin 5. If required, an external roll-off capacitor can be fixed to this point.

The large number of circuit nodes accessible from the outside of the package affords great flexibility, enabling the operating currents and circuit configuration to be optimised for any application. In particular, the input transistor (TR1) can be operated in common emitter mode by decoupling pin 7 and using 6 as the input. In this configuration, a 2dB noise figure (R_S = 200Ω) can be achieved. This configuration can give a gain of 35dB with a bandwidth of 75MHz (see Figs. 8 and 9) or, using feedback 14dB with a bandwidth of 300MHz (see Figs. 10 and 11).

Because the transistors used in the SL560C exhibit a high value of f_T, care must be taken to avoid high frequency instability. Capacitors of small physical size should be used, the leads of which must be as short as possible to avoid oscillation brought about by stray inductance. The use of a ground plane is recommended.

Further applications information is available in the 'Broadband Amplifier Applications' booklet.

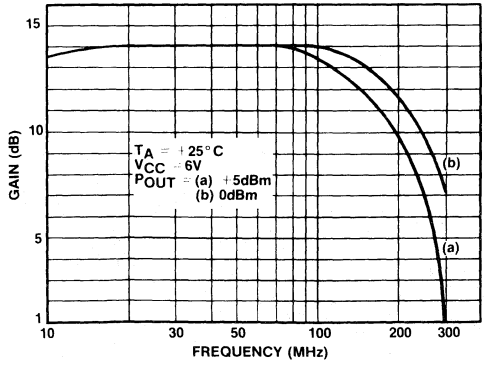


Fig.4 Frequency response, small signal gain is of a typical device

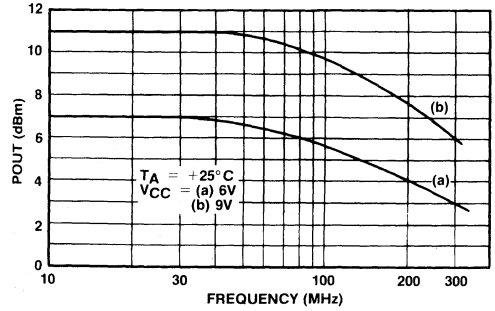


Fig.5 Frequency response, output capability (loci of maximum output power with frequency, for 1dB gain compression (typical)

TYPICAL APPLICATIONS

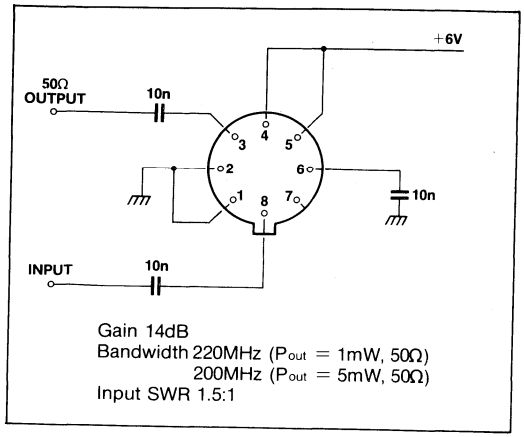


Fig.6 50Ω line driver. The response of this configuration is shown in Fig.4.

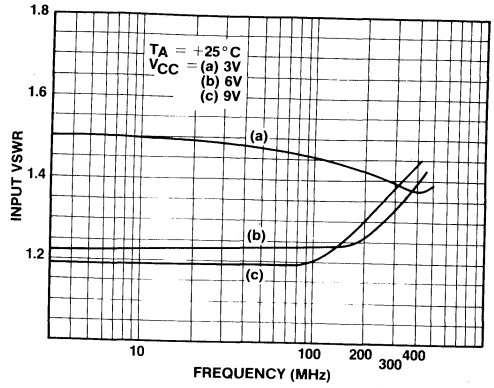


Fig.7 Input standing wave ratio plot of circuit shown in Fig.6 (typical)

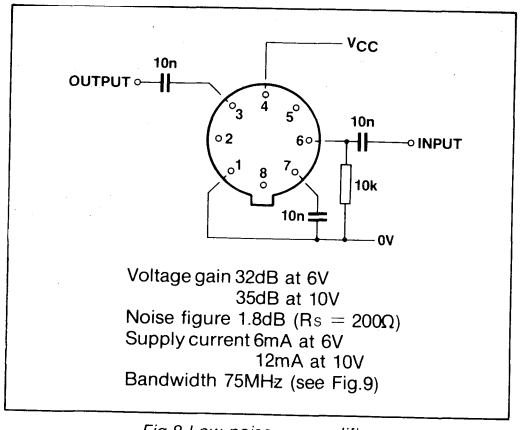


Fig.8 Low noise preamplifier

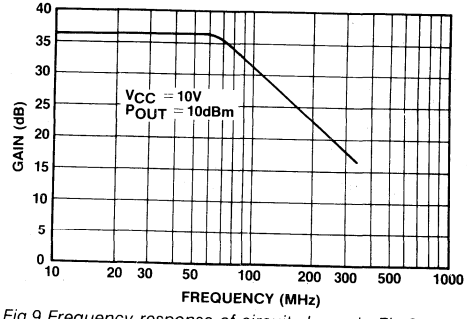


Fig.9 Frequency response of circuit shown in Fig.8 (typical)

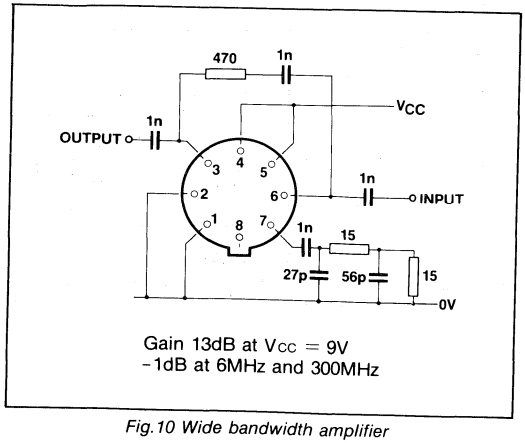


Fig.10 Wide bandwidth amplifier

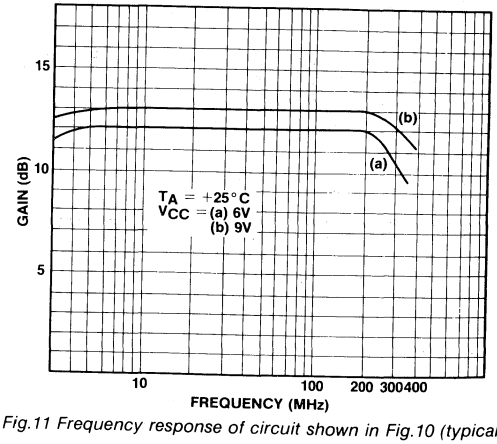


Fig.11 Frequency response of circuit shown in Fig.10 (typical)

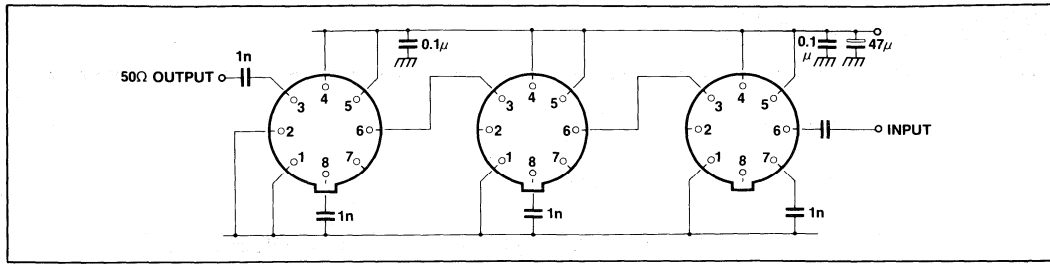


Fig.12 Three-stage directly-coupled high gain low noise amplifier

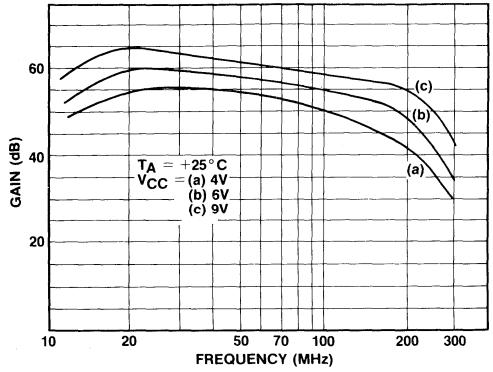


Fig.13 Frequency response of circuit shown in Fig.12 (typical)

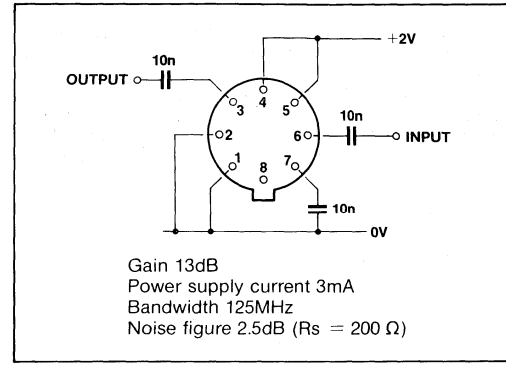


Fig.14 Low power consumption amplifier

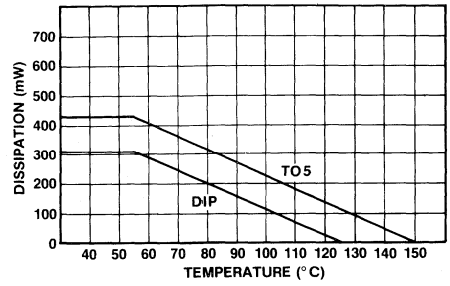


Fig.15 Ambient operating temperature v. degrees centigrade (typical)

PLESSEY
Semiconductors

SL562

LOW NOISE PROGRAMMABLE OPERATIONAL AMPLIFIER

The SL562 is an advanced bipolar integrated circuit containing a single programmable operational amplifier. The amplifier can be programmed by current into a bias pin which determines the main characteristics of the amplifier's, supply current, frequency response and slew rate. With a suitable choice of bias current the SL562 can be used where low power and low noise characteristics are a necessity.

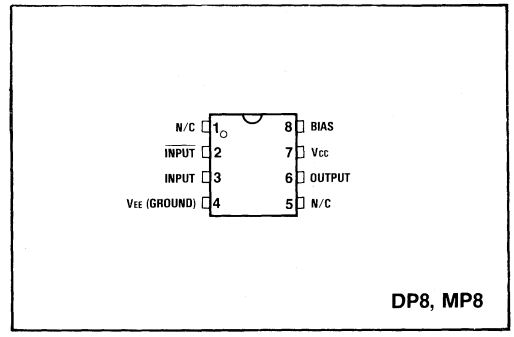


Fig.1 Pin connections - top view

FEATURES

- Low Noise Guaranteed (25nV/√Hz at 1kHz)
- Low Supply Current (40uA)
- Bias Conditions Adjustable to Optimise Performance
- Built In Short Circuit Protection
- Available In Small Outline

APPLICATIONS

- Active Filters
- Oscillators
- Low Voltage Amplifiers
- Frequency Synthesisers
- Hand Held Radio Applications

QUICK REFERENCE DATA

- Supply Voltages ±1.5V to ±10V
- Supply Current ±40μA to ±2mA
- Operating Frequency Range 1MHz
- Gain 95dB
- Operating Temperature Range -40°C to +85°C

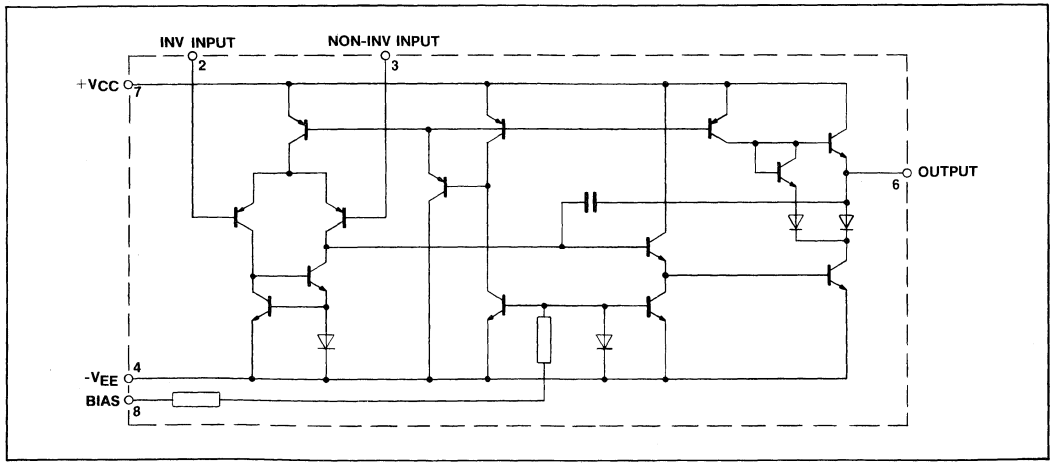


Fig.2 Circuit diagram.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 25° C
Operating mode A : Supply volts ±10V Bias set current 75μA
Operating mode B : Supply volts ±3.5V Bias set current 15μA
Operating mode C : Supply volts ±1.5V Bias set current 1μA

Characteristic	Operating mode									Units	Conditions
	A			B			C				
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Input offset voltage		1	5		1	5		1	5	mV	R_S = 10kΩ
Input offset current		20	190			150			49	nA	
Input bias current		250	800			350			95	nA	
Input resistance	0.1	0.6		0.2	0.5		0.3	2		MΩ	
Supply current	1000	1600	2200	50	200	1000	20	40	60	μA	
Large signal voltage gain	74	95		74	90		74	90		dB	R_L = 4kΩ(A) R_L = 100kΩ(B) R_L = 100kΩ(C)
Input voltage range	10	10.5		10	10.5		0.2	0.4		±V	R_S = 10kΩ
Common mode rejection ratio	70	110		70	85		70	82		dB	
Output voltage swing	8			1.5			0.7	0.8		±V	R_L = 4kΩ(A) R_L = 10kΩ(B) R_L = 4kΩ(C)
Supply voltage rejection ratio	74			85			85			dB	R_S = 10kΩ
Short circuit current	12		40				1	2.2		mA	T_{amb} = 0° C to +70° C
Gain bandwidth product		3.5			1			50		kHz MHz	Gain = 20dB
Slew rate		1.5			0.5			0.02		V/μs	Gain = 20dB
Input noise voltage		10	25		25	40		50	85	nV√Hz	fo = 1kHz
Input noise current		1.6			1.6			1.0		pA√Hz	f = 1kHz

OPERATING NOTES

Bias set current

The amplifier is programmed by the I_{SET} current into the BIAS pin to determine the frequency response, slew rate and the value of supply current. The relationship is summarised as follows:

Gain bandwidth product	I_{SET} x 50kHz
Power supply current (each supply)	I_{SET} x 25μA
Slew rate	I_{SET} x 0.02V/μs
	(I_{SET} in μA)

The open loop voltage gain is largely unaffected by change in bias set current but tends to peak slightly at 10μA.

Since the voltage on the BIAS pin is approximately 0.65V more positive than the negative supply, a resistor may be connected between the bias pin and either 0V or the positive supply to set the current. Thus, if the resistor is connected to 0V, the I_{SET} current is determined by:

$$I_{SET} = \frac{V_S - 0.65}{R}$$

where R is value of the 'set' resistor.

The output goes high if the non-inverting input is taken lower than 1V above the negative power supply.

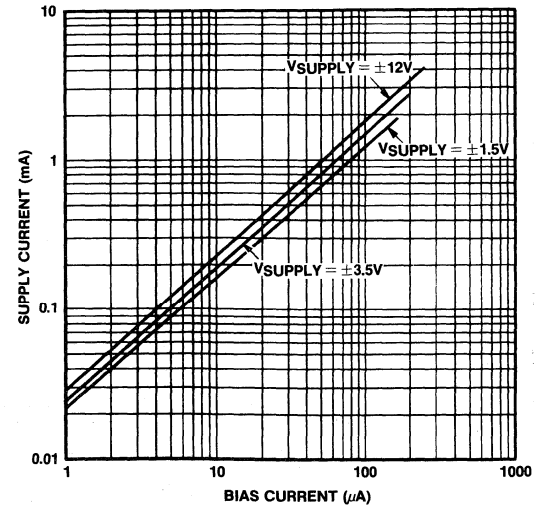


Fig.3 Supply current v. bias set current.

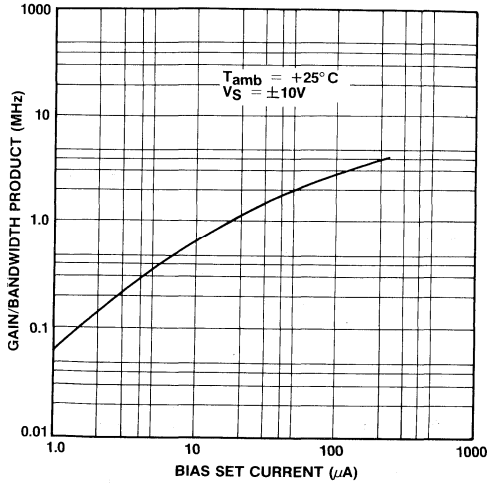


Fig.4 Gain bandwidth product v. ISET

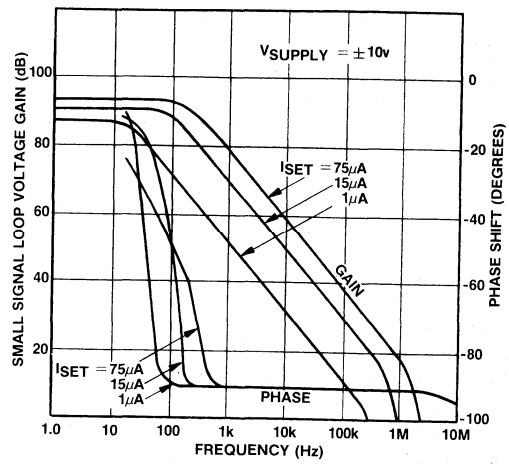


Fig. 5 Typical frequency response

APPLICATION EXAMPLE

The SL562 is especially suitable for use in loop filters for frequency synthesisers, the low noise and low power characteristics of the SL562 making it ideally suited for use with the Plessey low power frequency synthesiser circuits (NJ8820, SP87XX). All three integrated circuits are available in surface mounting packages, thus making a compact hybrid.

ABSOLUTE MAXIMUM RATINGS

Supply voltages	±15V
Common mode input voltage	Not greater than supplies
Differential input voltage	±25V
Bias set current	10mA
Storage	-55° C to +125° C
Power dissipation	800mW at 25° C
	Derate at 7mW/° C above 25° C
Operating temperature range	-40° C to +85° C

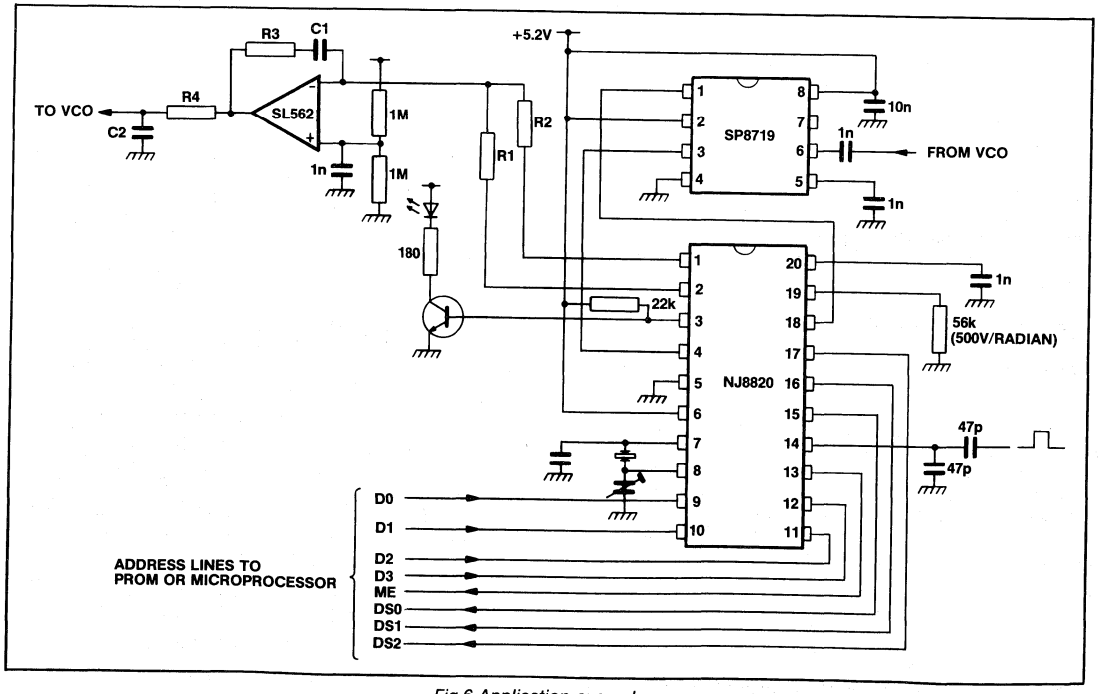


Fig.6 Application example.

PLESSEY
Semiconductors

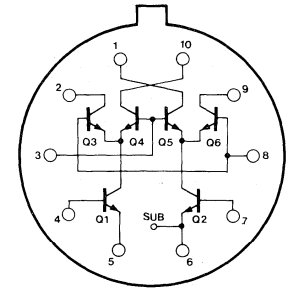
SL2363C & SL2364C

VERY HIGH PERFORMANCE TRANSISTOR ARRAYS

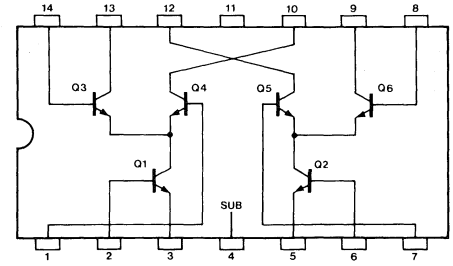
The SL2363C and SL2364C are arrays of transistors internally connected to form a dual long-tailed pair with tail transistors. They are monolithic integrated circuits manufactured on a very high speed bipolar process which has a minimum useable f_T of 2.5GHz, (typically 5GHz).

The SL2363 is in a 10 lead TO5 encapsulation.

The SL2364 is in a 14 lead DIL plastic encapsulation and a high performance Dilmon encapsulation.



SL2363C CM10



SL2364C DC14 DP14 MP14

Fig. 1 Pin connections (top view)

FEATURES

- Complete Dual Long-Tailed Pair in One Package.
- Very High f_T – Typically 5 GHz
- Very Good Matching Including Thermal Matching

APPLICATIONS

- Wide Band Amplification Stages
- 140 and 560 MBit PCM Systems
- Fibre Optic Systems
- High Performance Instrumentation
- Radio and Satellite Communications

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 22°C ±2°C

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
BV_{CBO}	10	20		V	I_C = 10µA
LV_{CEO}	6	9		V	I_C = 5mA
BV_{EBO}	2.5	5.0		V	I_E = 10µA
BV_{CIO}	16	40		V	I_C = 10µA
h_{FE}	50	80			I_C = 8mA, V_{CE} = 2V
f_T	2.5	5		GHz	I_C (Tail) = 8mA, V_{CE} = 2V
ΔV_{BE} (See note 1)		2	5	mV	I_C (Tail) = 8 mA, V_{CE} = 2V
$\Delta V_{BE}/T_{AMB}$		-1.7		mV/°C	I_C (Tail) = 8 mA, V_{CE} = 2V
C_{CB}		0.5	0.8	pF	V_{CB} = 0
C_{CI}		1.0	1.5	pF	V_{CI} = 0

NOTE 1. ΔV_{BE} applies to $|V_{BEQ3} - V_{BEQ4}|$ and $|V_{BEQ5} - V_{BEQ6}|$

TYPICAL CHARACTERISTICS

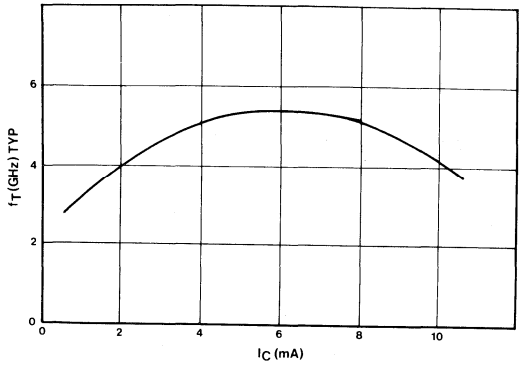


Fig. 2 Collector current

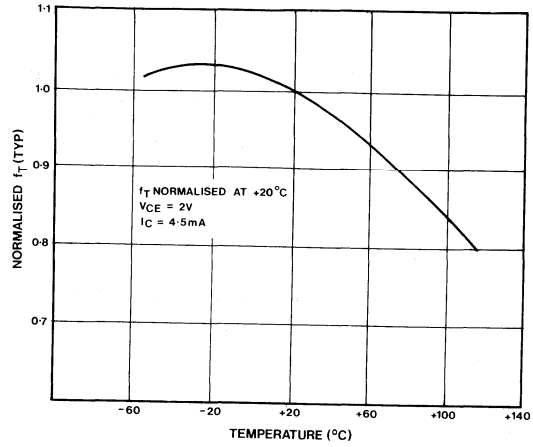


Fig. 3 Chip temperature

ABSOLUTE MAXIMUM RATINGS

Maximum individual transistor dissipation 200mW

Storage temperature −55°C to +150°C
Maximum junction temperature +150°C
Package thermal resistance (°C/W):
Chip to case 65 (CM10)
Chip to ambient 225 (CM10) 175 (DP14)
V_{CBO} = 10V, V_{EBO} = 2.5V, V_{CEO} = 6V, V_{CIO} = 15V, IC (any one transistor) = 20mA

The substrate should be connected to the most negative point of the circuit to maintain electrical isolation between the transistors.

PLESSEY
Semiconductors

SL2365

VERY HIGH PERFORMANCE TRANSISTOR ARRAY

The SL2365 is an array of transistors internally connected to form a dual long-tail pair with current mirrors whose bases and collectors are connected internally. The ICs are manufactured on a very high speed bipolar process, which has a minimum usable f_T of 2.5GHz (typically 5GHz). The current mirror enables a well defined gain at low current levels to be achieved.

FEATURES

- Complete Dual Long Tailed Pair in One Package
- Very High f_T - Typically 5GHz
- Well Defined Gain at Low Current Levels
- Available in Small Outline Package

CAUTION

Pins 4 and 11 should be equal and at the most negative voltage on the array.

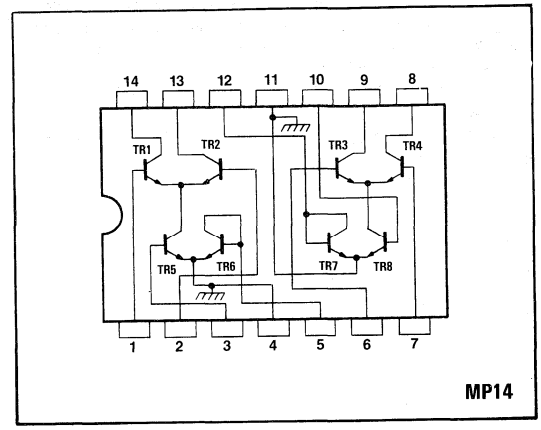


Fig.1 Pin connections - top view

ELECTRICAL CHARACTERISTICS

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
BV_{cbo}	10	20		V	$I_C = 10\mu A$
LV_{ceo}	6	9		V	$I_C = 5mA$
BV_{ebo}	2.5	5		V	$I_E = 10\mu A$
BV_{cio}	16	40		V	$I_C = 10\mu A$
H_{fe}	50	80			$I_C = 8mA$, $V_{ce} = 2V$
f_T	2.5	5		GHz	I_C (tail) $= 8mA$, $V_{ce} = 2V$
ΔV_{be}		2	5	mV	I_C (tail) $= 8mA$, $V_{ce} = 2V$
$\Delta V_{be}/T_{amb}$		-7		mV/°C	I_C (tail) $= 8mA$, $V_{ce} = 2V$
C_{CB}		0.5	0.8	pF	$V_{CB} = 0V$
C_{CI}		1.0	1.5	pF	$V_{CI} = 0V$

SL6140

400MHz WIDEBAND AGC AMPLIFIER

(Supersedes edition in September 1988 Linear IC Handbook)

The SL6140 is an integrated broadband AGC amplfier, designed on an advanced 3-micron all implanted bipolar process. The amplifier provides over 15dB of linear gain into 50Ω with a 400MHz bandwidth.

Accurate gain control is also provided with over 70dB of dynamic range.

The SL6140 provides over 45dB of voltage gain with an R_L of 1kΩ.

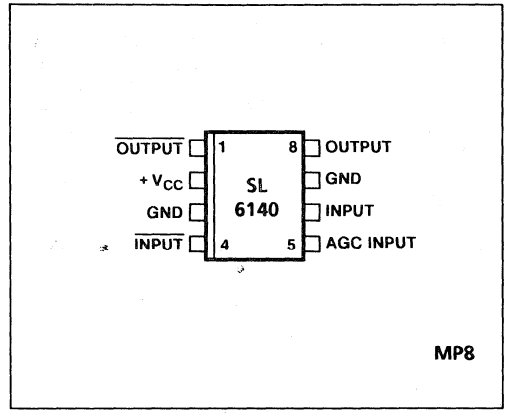


Fig.1 Pin connections (top view)

FEATURES

- 400MHz Bandwidth (R_L = 50Ω)
- High Voltage Gain 45dB (R_L = 1kΩ)
- 70dB Gain Control Range
- High Output Level at Low Gain
- Accurate Gain Control
- MC1590 Replacement

APPLICATIONS

- RF/IF Amplifier
- High Gain Mixers
- Video Amplifiers

ORDERING INFORMATION

SL6140 MP (Industrial - Miniature Plastic DIL Package)

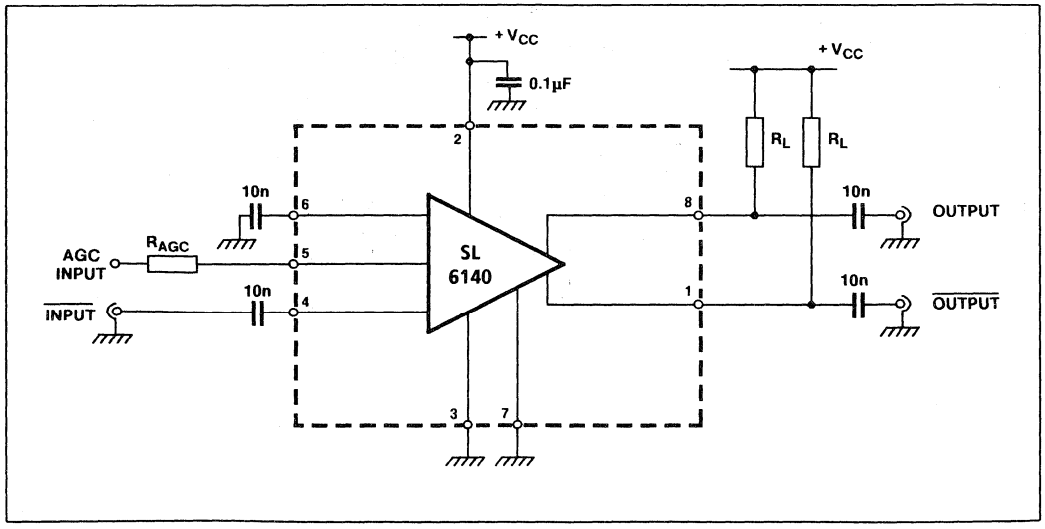


Fig.2 Typical wideband application (R_{AGC} = 5.6k)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = 25°C$, $V_{CC} = +12V$

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	1,2,8	-	19	23	mA	
Output stage current	1,8 (sum)	5	7	9	mA	
Output current matching (magnitude of difference of output currents)	1,8	-	0.5	-	mA	
AGC range	5	60	75	-	dB	See Fig. 4
Voltage gain (single ended)	1,8	40	45	-	dB	$R_L = 1k\Omega$ See Fig.5
			55		dB	Tuned input and output
	1,8	-	15	-	dB	$R_L = 50\Omega$
Bandwidth (-3dB)	1,8	-	25	-	MHz	$R_L = 1k\Omega$ See Fig. 5
			400		MHz	$R_L = 50\Omega$
Maximum output level (single ended)						
0dB AGC	1,8	2.5	3.5	-	V p-p	$R_L = 1k\Omega$
-30dB AGC	1,8	2.5	3.5	-	V p-p	$R_L = 1k\Omega$

DESCRIPTION

The SL6140 (Fig.3) is a high gain amplifier with an AGC control capable of reducing the gain of the amplifier by over 70dB. The gain is adjustable by applying a voltage to the AGC input via an external resistor (R_{AGC}, the value of which adjusts the curve of gain reduction versus control voltage (see Fig. 4) As the output stage of the amplifier is an open collector the maximum voltage gain is determined by R_L. With load resistance of $1k\Omega$ the single ended voltage gain is 45dB and with a load resistance of 50Ω the voltage gain is 15dB ($20\log_{10} V_{OUT}/V_{IN}$). Another parameter that depends on the load resistance is the bandwidth: 25MHz for $R_L = 1k\Omega$, as compared with 400MHz for $R_L = 50\Omega$. R_L is chosen to give either the required bandwidth or voltage gain for the circuit.

Fig. 7 shows the input impedance of the device. Accurate impedance matching to both inputs and outputs of this device (by resonant circuit or other means) can raise the gain to 55dB but for most circumstances a 50Ω source impedance is adequate.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+15V
Input voltage (differential)	+5V
AGC Supply	V_{CC}
Storage temperature	-55°C to +125°C
Operating temperature	0°C to 70°C

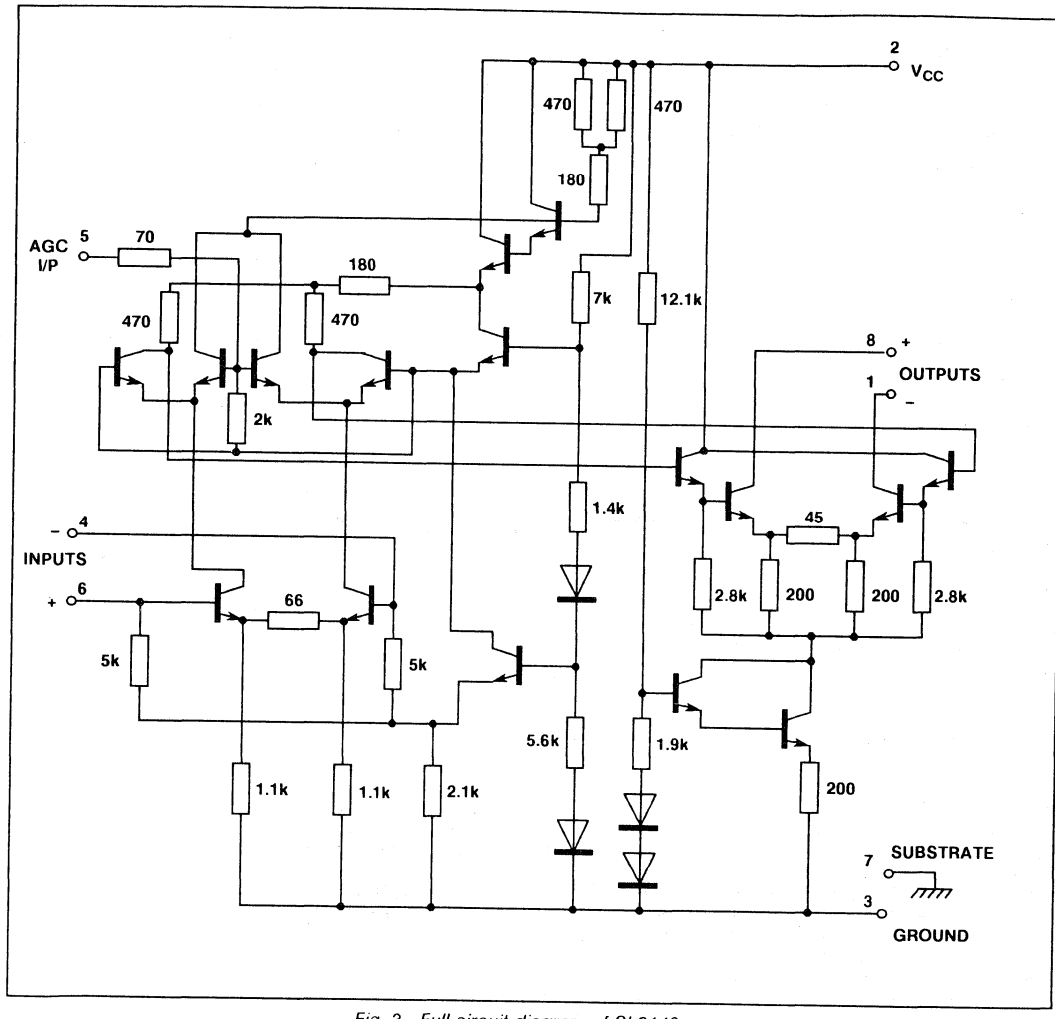


Fig. 3 - Full circuit diagram of SL6140

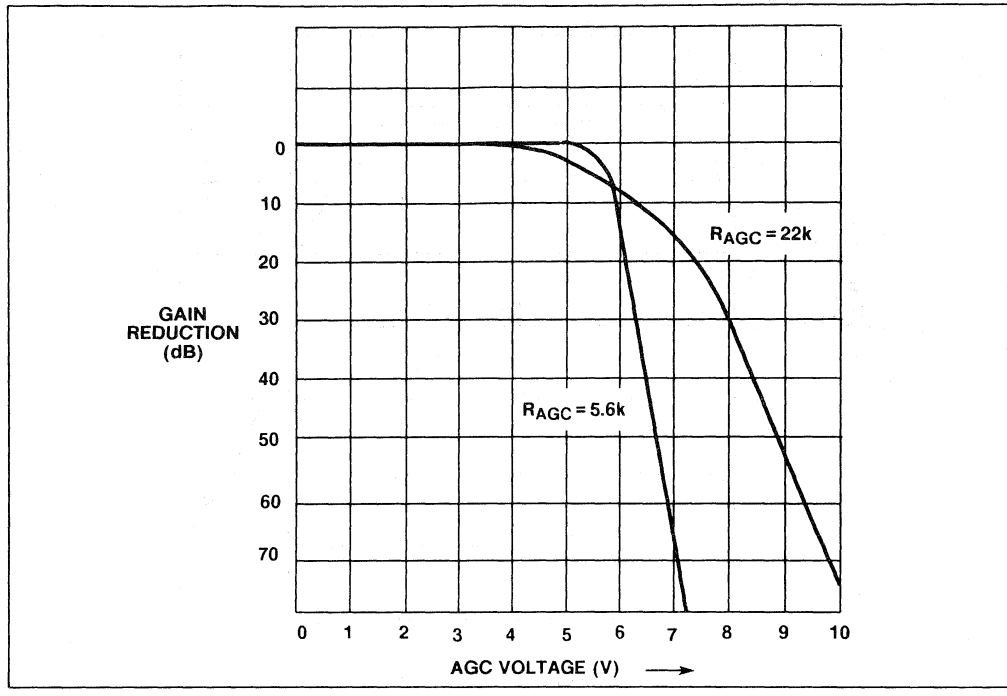


Fig. 4 - Gain reduction v. AGC Voltage

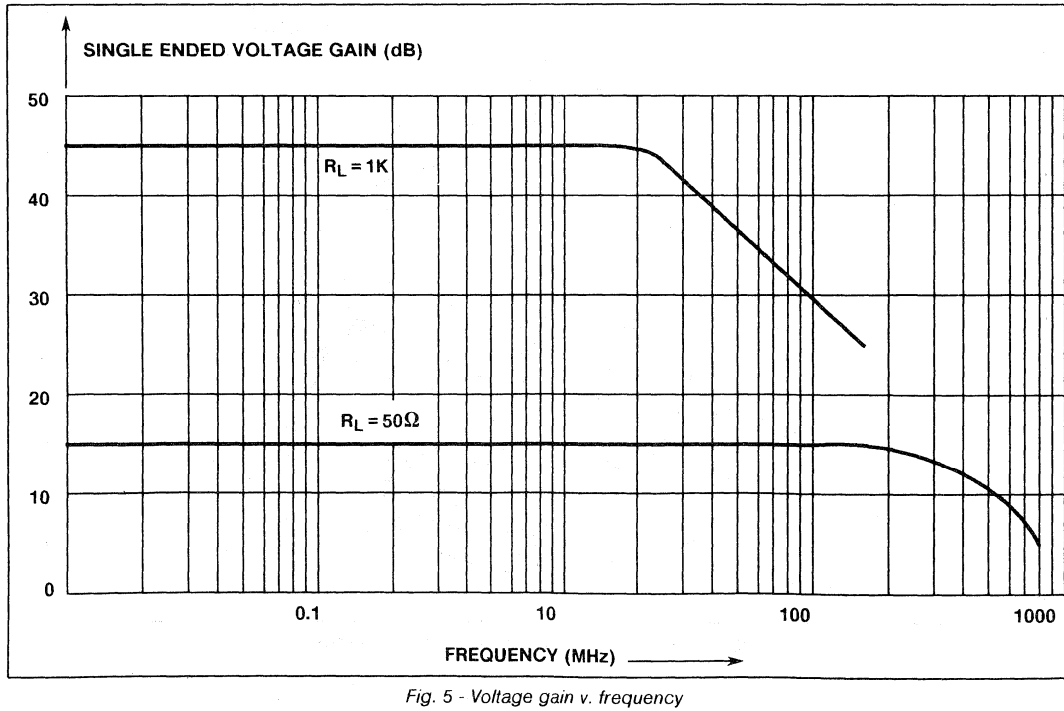


Fig. 5 - Voltage gain v. frequency

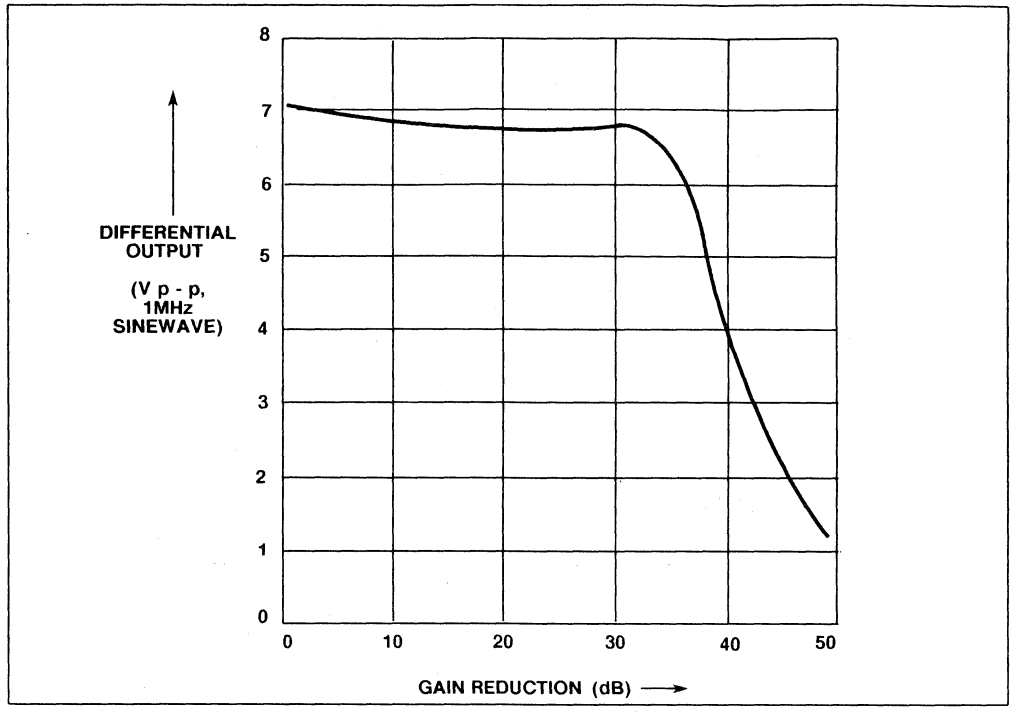


Fig. 6 - Maximum differential output v. gain reduction

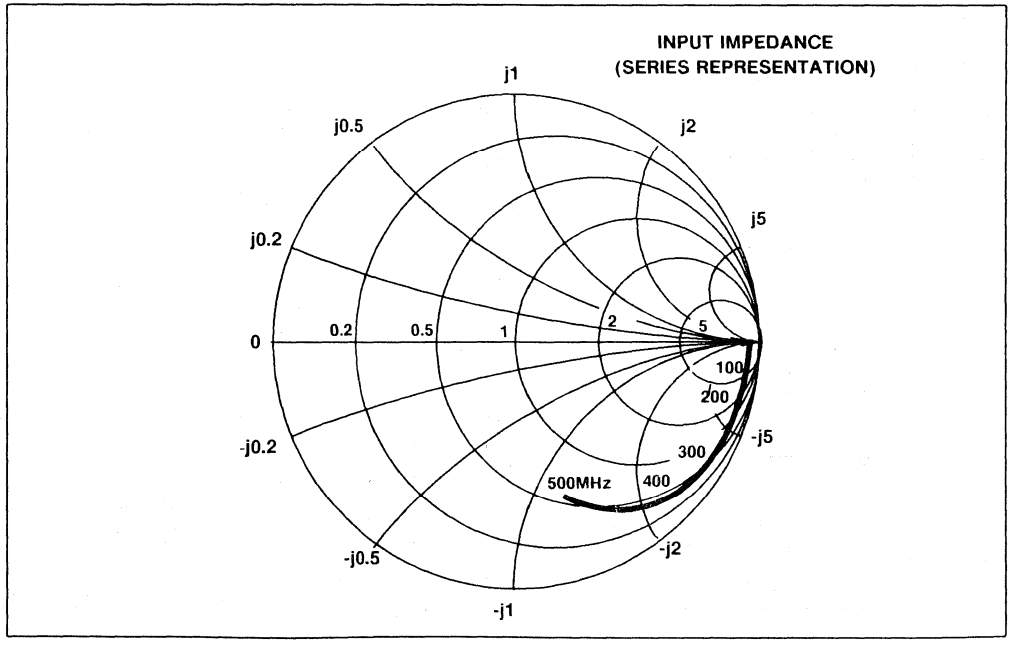


Fig. 7 Input impedance of SL6140 (50Ω normalised)

PLESSEY
Semiconductors

SL6270C

GAIN CONTROLLED MICROPHONE PREAMPLIFIER/VOGAD

The SL6270 is a silicon integrated circuit combining the functions of audio amplifier and voice operated gain adjusting device (VOGAD).

It is designed to accept signals from a low sensitivity microphone and to provide an essentially constant output signal for a 50dB range of input. The dynamic range, attack and decay times are controlled by external components.

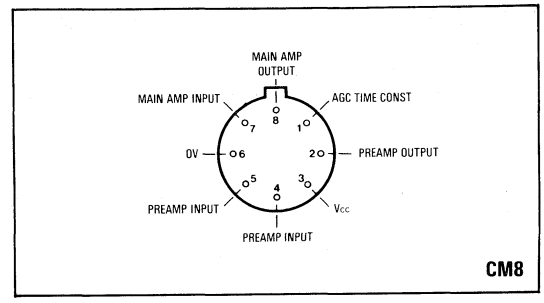


Fig.1 Pin connections, SL6270 - CM (bottom view)

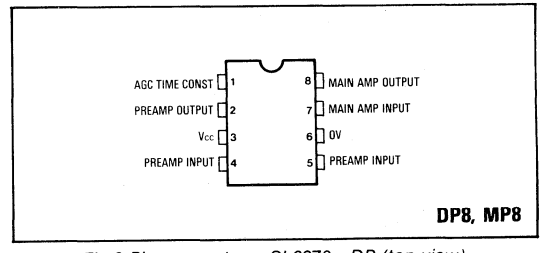


Fig.2 Pin connectons, SL6270 - DP (top view)

FEATURES

- Constant Output Signal
- Fast Attack
- Low Power Consumption
- Simple Circuitry

APPLICATIONS

- Audio AGC Systems
- Transmitter Overmodulation Protection
- Tape Recorders

QUICK REFERENCE DATA

- Supply Voltage: 4.5V to 10V
- Voltage Gain: 52dB

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: −55°C to +125°C

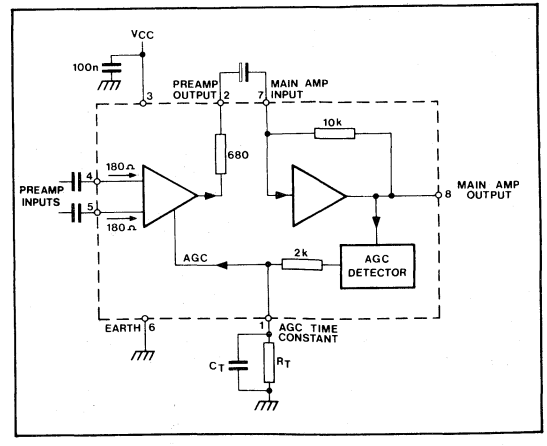
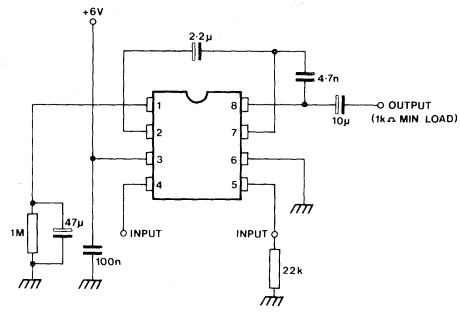


Fig.3 SL6270 block diagram

ELECTRICAL CHARACTERISTICS

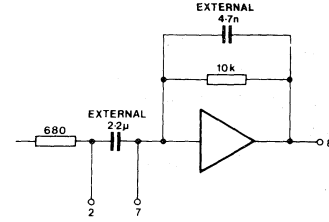
Test conditions (unless otherwise stated):
Supply voltage Vcc: 6V
Input signal frequency: 1kHz
Ambient temperature: −30°C to +85°C
Test circuit shown in Fig. 4

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5	10	mA	
Input impedance		150		Ω	Pin 4 or 5
Differential input impedance		300		Ω	
Voltage gain	40	52		dB	72μV rms input pin 4
Output level	55	90	140	mV rms	4mV rms input pin 4
THD		2	5	%	90mV rms input pin 4
Equivalent noise input voltage		1		μV	300Ω source, 400Hz to 25kHz bandwidth



N.B. If input not AC coupled the resistance between pins 4 and 5 must be less than 10 ohms.

Fig.4 SL6270 test and application circuit



$$\text{Voltage gain} = \frac{10k\Omega}{680\Omega}$$

Upper frequency response 10kΩ/4.7nF = 3kHz
Lower frequency response 680Ω/2.2μF = 300Hz

Fig.5 SL6270 frequency response

APPLICATION NOTES

Voltage gain

The input to the SL6270 may be single ended or differential but must be capacitor coupled. In the single-ended mode the signal can be applied to either input, the remaining input being decoupled to ground. Input signals of less than a few hundred microvolts rms are amplified normally but as the input level is increased the AGC begins to take effect and the output is held almost constant at 90mV rms over an input range of 50dB.

The dynamic range and sensitivity can be reduced by reducing the main amplifier voltage gain. The connection of a 1k resistor between pins 7 and 8 will reduce both by approximately 20dB. Values less than 680Ω are not advised.

Frequency response

The low frequency response of the SL6270 is determined by the input, output and coupling capacitors. Normally the coupling capacitor between pins 2 and 7 is chosen to give a -3dB point at 300Hz, corresponding to 2.2μF, and the other capacitors are chosen to give a response to 100Hz or less.

The SL6270 has an open loop upper frequency response of a few MHz and a capacitor should be connected between pins 7 and 8 to give the required bandwidth.

Attack and delay times

Normally the SL6270 is required to respond quickly by holding the output level almost constant as the input is increased. This 'attack time', the time taken for the output to return to within 10% of the original level following a 20dB increase in input level, will be approximately 20ms with the circuit of Fig.4. It is determined by the value of the capacitor connected between pin 1 and ground and can be calculated approximately from the formula:

$$\text{Attack time} = 0.4\text{ms}/\mu\text{F}$$

The decay time is determined by the discharge rate of the capacitor and the recommended circuit gives a decay rate of 20dB/second. Other values of resistance between pin 1 and ground can be used to obtain different results.

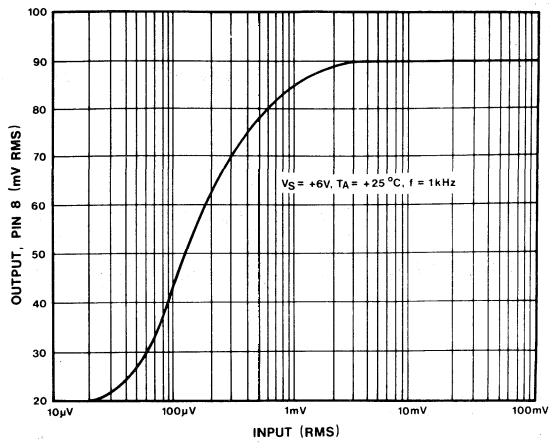


Fig. 6 Voltage gain (single ended input) (typical)

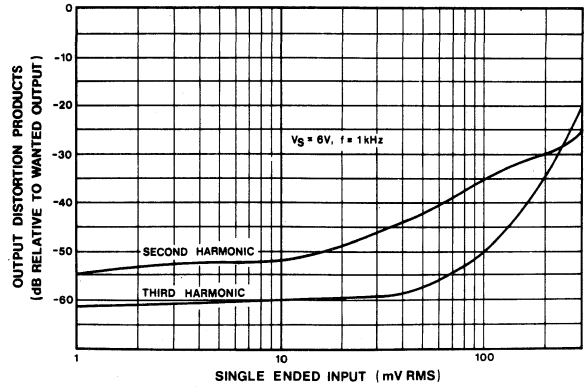


Fig. 7 Overload characteristics (typical)

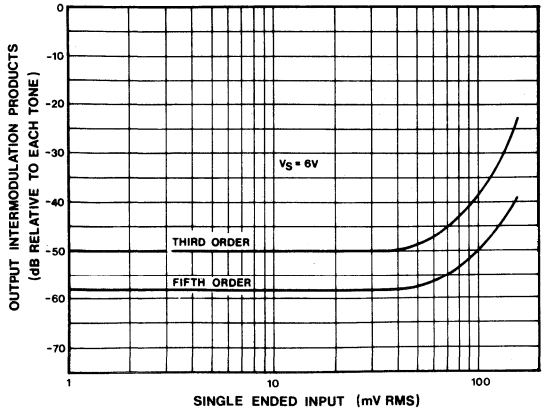


Fig. 8 Typical Intermodulation distortion (1.55 and 1.85kHz tones)

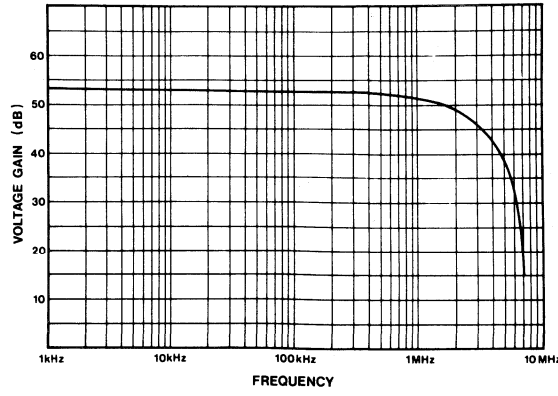


Fig. 9 Open loop frequency response (typical)

SL6310C

500mW SWITCHABLE AUDIO AMPLIFIER/OP AMP

The SL6310C is a low power audio amplifier which can be switched off by applying a mute signal to the appropriate pin. Despite the low quiescent current consumption of 5mA (only 0.6mA when muted) a minimum output power of 400mW is available into an 8Ω load from a 9V supply.

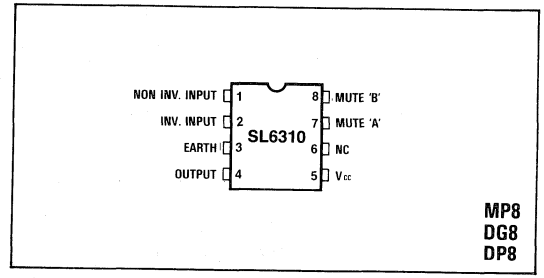


Fig.1 Pin connections SL6310 - (top view)

FEATURES

- Can be Muted with High or Low State Inputs
- Operational Amplifier Configuration
- Works Over Wide Voltage Range

APPLICATIONS

- Audio Amplifier for Portable Receivers
- Power Op. Amp
- High Level Active Filter

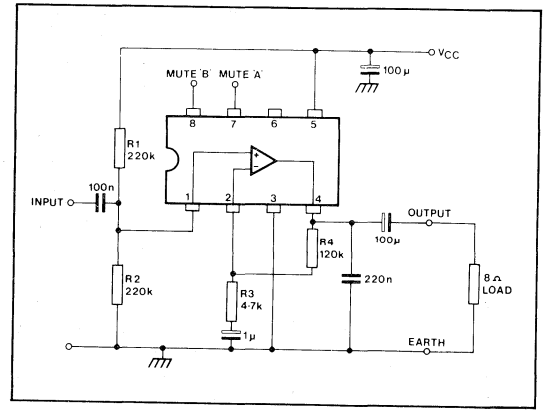


Fig.2 SL6310 test circuit

QUICK REFERENCE DATA

- Supply Voltage: 4.5V to 13.6V
- Voltage Gain: 70dB
- Output into 8Ω on 9V Supply: 400mW (min.)

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 15V
Storage temperature: −55°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC} : 9V
Ambient temperature: −30°C to +85°C
Mute facility: Pins 7 and 8 open circuit frequency = 1kHz

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5.0	7.5	mA	
Supply current muted (A)		0.55	1	mA	Pin 7 via 470k to earth
Supply current muted (B)		0.6	0.9	mA	Pin 8 = V_{CC}
Input offset voltage		2	20	mV	$R_S \leq 10k$
Input offset current		50	500	nA	
Input bias current (Note 1)		0.2	1	µA	
Voltage gain	40	70		dB	
Input voltage range		2.1		V	V_{CC} = 4.5V
		10.6		V	V_{CC} = 13V
CMRR	40	60		dB	$R_S \leq 10k$
Output power	400	500		mW	$R_L = 8\Omega$
THD		0.4	3	%	P_{OUT} = 400mW, Gain = 28dB

NOTE
1. The input bias current flows **out** of pins 1 and 2 due to PNP input stage

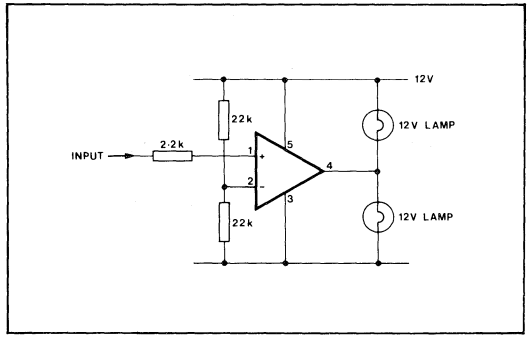


Fig.3 SL6310 lamp driver

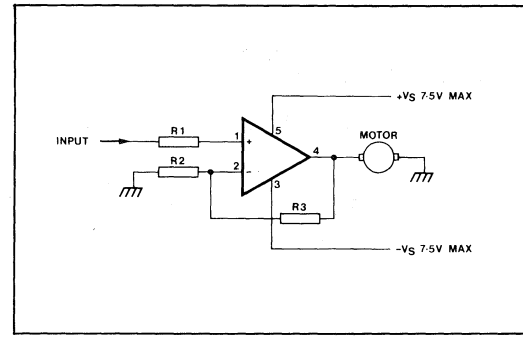


Fig.4 SL6310 servo amplifier

OPERATING NOTES

Mute facility

The SL6310 has twomute control pins to allow easy interfacing to inputs of high or low levels. Mute control 'A', pin 7, is left open circuit or connected to a voltage within 0.65 volt of V_{CC} (via a 100kΩ resistor) for normal operation. When the voltage on pin 7 is reduced to within 1 volt of earth (via a 100kΩ resistor) the SL6310 is muted.

Audio amplifier

As the SL6310 is an operational amplifier it is easy to obtain the voltage gain and frequency response required. To keep the input impedance high it is wise to feed the signal to the non-inverting input as shown in Fig.2. In this example the input impedance is approximately 100kΩ. The voltage gain is determined by the ratio (R3 + R4)/R3 and should be between 3 and 30 for best results. The capacitor in series with R3, together with the input and output coupling capacitors, determines the low frequency rolloff point. The upper frequency limit is set by the device but can be restricted by connecting a capacitor across R4.

Operational amplifier

It is impossible to list all the application possibilities in a single data sheet but the SL6310 offers considerable advantages over conventional devices in high output current applications such as lamp drivers (Fig.3) and servo amplifiers (Fig.4).

Buffer and output stages for signal generators are another possibility together with active filter sections requiring high output current.

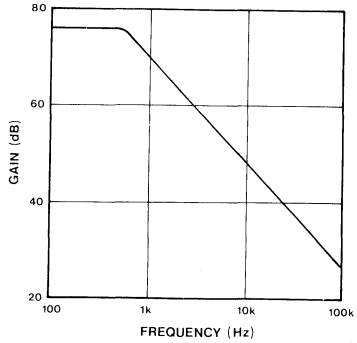


Fig.5 Gain v. frequency

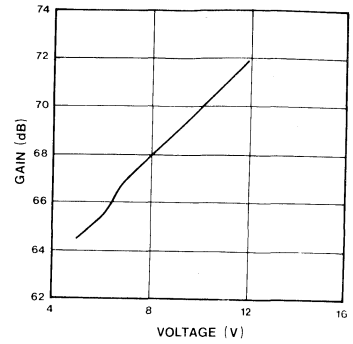


Fig.6 Gain v. supply voltage

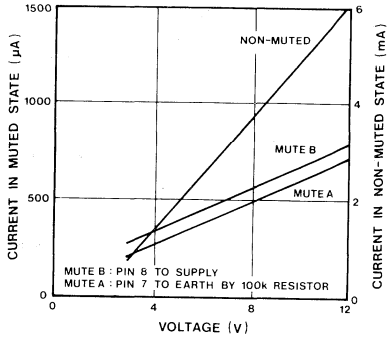


Fig.7 Supply current v. supply voltage

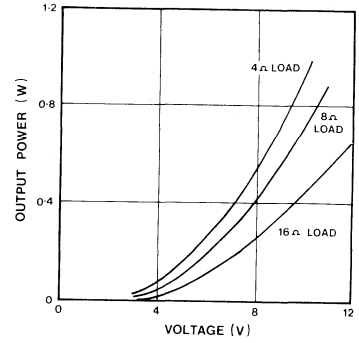
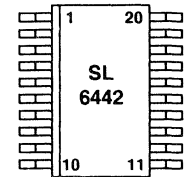


Fig.8 Output power v. supply voltage at 5% (max) distortion

SL6442

1GHz AMPLIFIER / MIXER

The SL6442 EHF Amplifier and Mixer is designed for use in Cordless Telephones, Cellular Telephones and Pagers, and low power receivers operating at frequencies up to 1GHz. It contains a low noise amplifier with AGC facility and two mixers for use in I and Q direct conversion receivers or image cancelling in superheterodyne receivers. Operating from a single supply of 5V it requires a current of typically 4 mA and has a power down facility.



MP20

Pin	Function	Pin	Function
1	RF V_{CC}	11	Mixer A Output
2	V_{REG}	12	Ground
3	RF Input (CB)	13	LO A Input
4	RF Input (CE)	14	LO B Input
5	RF Decouple	15	Mixer B Output
6	RF Output	16	LO Decouple
7	RF Ground	17	VCC
8	Mixer Input	18	Mixer Decouple
9	Bandgap	19	AGC Decouple
10	Battery Economy	20	AGC

Fig.1 Pin connections

FEATURES

- 1GHz Operation
- Very Low Power
- Suitable for Direct Conversion or Superheterodyne Architectures
- On board RF Amplifier
- Power Down Facility for Battery Economy
- AGC Capability
- Common Emitter or Common Base RF Input

ORDERING INFORMATION

SL6442 MP Miniature Plastic DIL Package

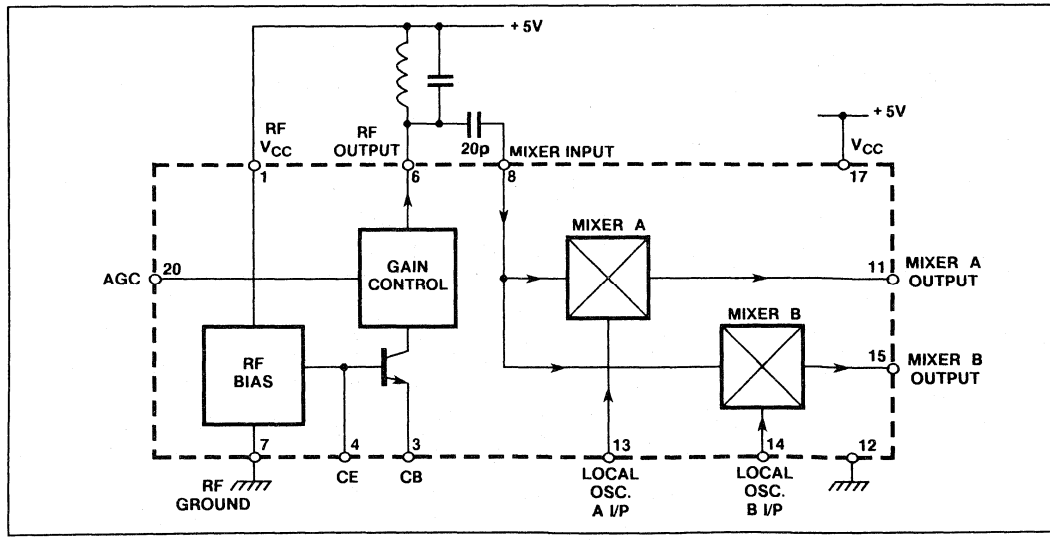


Fig. 2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
$T_{amb} = 25°C$, $V_{CC} = 5V \pm 5\%$ Freq. = 866MHz

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage		4.5	5.0	6.5	V	
Bandgap	9		1.2		V	
V_{REG}	2		1.6		V	
Supply current			4.3		mA	Supply at 5.0V Battery economy at 0V
Power down current			7		µA	Battery economy at V_{CC}
RF Amplifier						
Supply current			2		mA	
Power gain			14		dB	600 Ω tuned load at pin 6
AGC range	20		28		dB	V_{AGC} 1V to3V
Input intercept		-15	-12		dBm	Third order
1dB gain compression		-24			dBm	
Noise figure			4.5 6		dB	Common emitter Common base
Input impedance	4 3		90 15		Ω Ω	Common emitter Common base
Mixers						
Power conversion gain			0		dB	
L O drive level	13, 14		60		mV	p - p measured at pin
Input intercept point	8	-6	–1		dBm	Third order
1dB gain compression		-15			dBm	
Mixer current			1		mA	
Mixer A to Mixer B gain input match				±1.0	dB	LO drive levels equal ±1.0dB
Mixer A to Mixer B phase input match				±4	deg	LO inputs 90 ± 0.1 deg phase difference
Input impedance	8		600		Ω	at 866MHz
Noise figure			19		dB	
Operating frequency range		0.2		1.0	GHz	
Mixer output impedance	11, 15		4		kΩ	

Pin No.	Name	Description
1	RF V_{CC}	This is the supply to the RF amplifier. Normally connected to +5V, It should be adequately bypassed.
2	V_{REG}	This is a 1.6Volt regulated output capable of supplying up to 0.5mA with an output impedance of 35Ω.
3	CB	This is the common base input to the emitter of the RF transistor. It should be returned to ground for DC using an RF choke or tuned circuit when in common base mode. It should be connected directly to ground in common emitter mode.
4	CE	This is the common emitter input to the base of the RF transistor. It is DC biased internally but should be decoupled in common base mode.
5	RF decouple	Decoupling of DC bias line.
6	RF output	Output port of the RF amplifier. It should be returned to +5V via an RF load: current typically of 2mA can flow.
7	RF ground	A separate ground is provided for the RF amplifer to promote stability.
8	Mixer input	This is coupled to the output of the RF amplifier (pin 6). It should be DC coupled to V_{REG} via an RF choke.
9	Bandgap	Temperature compensated DC reference Voltage. It should not be loaded.
10	Battery econ	Turns device 'OFF' when 'HIGH" (>3.0V); LOW is <1.5V for 'ON'
11	Mixer 'A' output	The output impedance is about 4kΩ; quiescent voltage is approximately 4V (V_{CC} = 5.0V)
12	Ground	Mixer and biasing ground
13	Local oscillator 'A' input	Input level of 60mV p - p. DC level is approximately 2.3V.
14	Local oscillator 'B' input	Input level of 60mV p - p. DC level is approximately 2.3V
15	Mixer 'B' output	The output impedance is about 4kΩ; quiescent voltage is approximately 4V (V_{CC} = 5.0V)
16	LO decouple	Decoupling of DC bias line
17	V_{CC}	+5V Supply should be bypassed effectively
18	Mixer decouple	Decoupling of DC bias line
19	AGC decouple	Decoupling of AGC input line
20	AGC	Varies RF amplifier gain. Gain reduces with increasing voltage, with RF gain reduced by 6dB when AGC = V_{REG}. Full range of AGC requires only typically 300mV DC range on this pin.

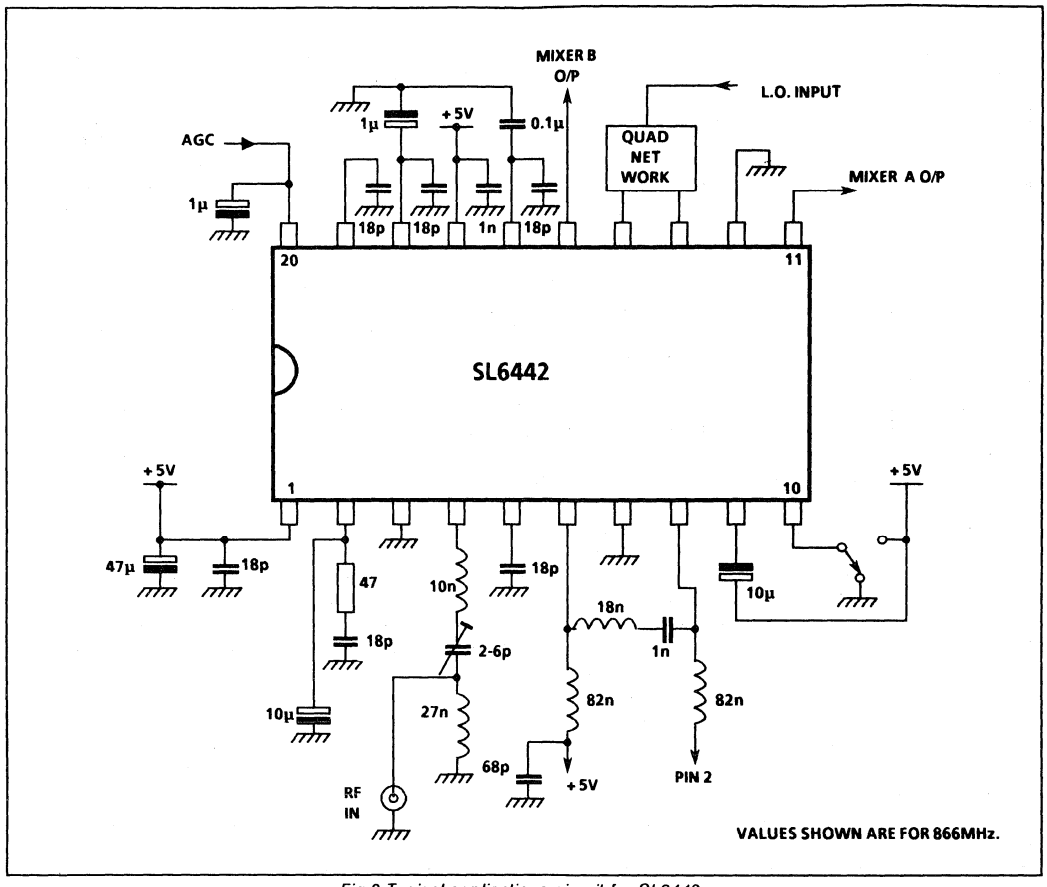


Fig.2 Typical applications circuit for SL6442

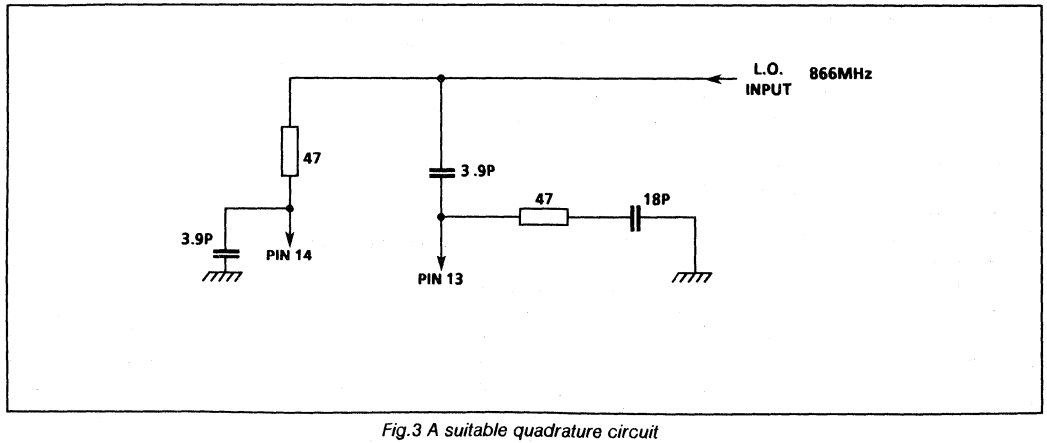


Fig.3 A suitable quadrature circuit

PLESSEY
Semiconductors

SL6601C

FM IF, PLL DETECTOR (DOUBLE CONVERSION) AND RF MIXER

The SL6601 is a straight through or single conversion IF amplifier and detector for FM radio applications. Its minimal power consumption makes it ideal for hand held and remote applications where battery conservation is important. Unlike many FM integrated circuits, the SL6601 uses an advanced phase locked loop detector capable of giving superior signal-to-noise ratio with excellent co-channel interference rejection, and operates with an IF of less than 1MHz. Normally the SL6601 will be fed with an input signal of up to 17MHz: there is a crystal oscillator and mixer for conversion to the IF amplifier, a PLL detector and squelch system.

FEATURES

- High Sensitivity: 2μV Typical
- Low Power: 2·3mA Typical at 7V
- Advanced PLL Detector
- Available in Miniature 'Chip Carrier' Package
- 100% Tested for SINAD

APPLICATIONS

- Low Power NBFM Receivers
- FSK Data Equipment
- Cellular Radio Telephones

QUICK REFERENCE DATA

- Supply Voltage 7V
- 50dB S/N Ratio

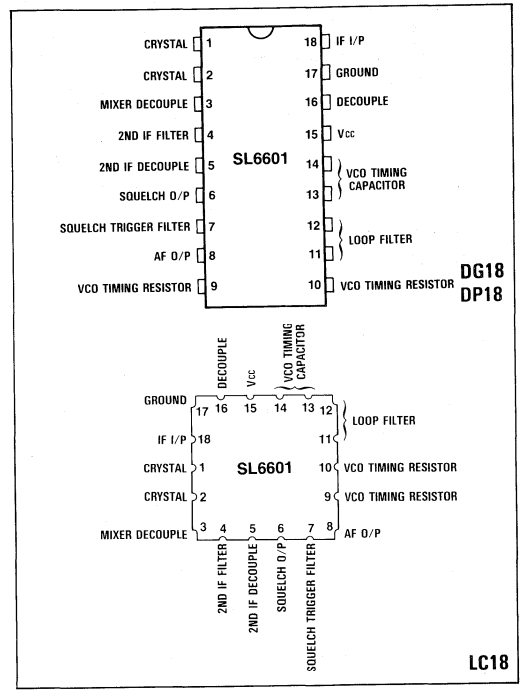


Fig.1 Pin connections - top view

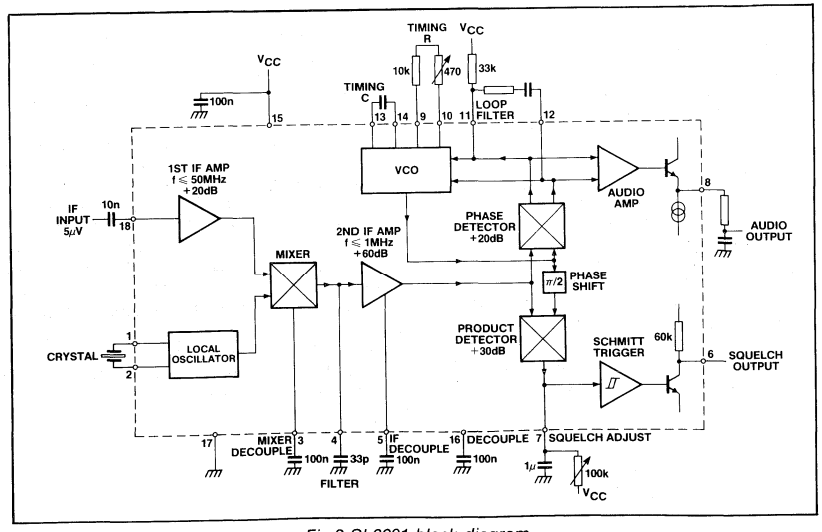


Fig.2 SL6601 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage Vcc : 7V

Input signal frequency: 10.7MHz, frequency modulated with a 1kHz tone with a ±2.5kHz frequency deviation

Ambient temperature: -30° C to +85° C; IF = 100kHz; AF bandwidth = 15kHz

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		2.3	2.7	mA	
Input impedance	100		300	Ω	Source impedance = 200Ω
Input capacity	0.5	2.0	3.5	pF	
Maximum input voltage level	0.5			V rms	At pin 18
Sensitivity	5	2		μV rms	At pin 18 for S + N/N = 20dB
Audio output	35	90	140	mV rms	
Audio THD		1.3	3.0	%	1mV rms input at pin 18
S + N/N	30	50		dB	1mV rms input at pin 18
AM rejection	30	Note 1		dB	100μV rms input at pin 18, 30% AM
Squelch low level		0.2	0.5	V dc	20μV rms input at pin 18
Squelch high level	6.5	6.9		V dc	No input
Squelch hysteresis		1	6	dB	3μV input at pin 18
Noise figure		6		dB	50Ω source
Conversion gain		30		dB	Pin 18 to pin 4
Input gain compression		100		μV rms	Pin 18 to pin 4, 1dB compression
Squelch output load	250			kΩ	
Input voltage range	80	100		dB	At pin 8; above 20dB S + N/N
3rd order intercept point (input)		-38		dBm	Input pin 18, output pin 4
VCO frequency					
Grade 1	85		100	kHz	390pF timing capacitor } No input
Grade 2	95		110	kHz	390pF timing capacitor } No input
Grade 3	105		120	kHz	390pF timing capacitor } No input
Source impedance (pin 4)		25	40	kΩ	
AF output impedance		4	10	kΩ	
Lock-in dynamic range	±8			kHz	20μV to 1mV rms at pin 18
External LO drive level	50		250	mV rms	At pin 2
Crystal ESR			25	Ω	10.8MHz

APPLICATION NOTES

IF Amplifiers and Mixer

The SL6601 can be operated either in a 'straight through' mode with a maximum recommended input frequency of 800kHz or in a single conversion mode with an input frequency of 50MHz maximum and an IF of 100kHz or ten times the peak deviation, whichever is the larger. The crystal oscillator frequency can be equal to either the sum or difference of the two IF's; the exact frequency is not critical.

The circuit is designed to use series resonant fundamental crystals between 1 and 17MHz.

When a suitable crystal frequency is not available a fundamental crystal of one third of that frequency may be used, with some degradation in performance.

E.G. If an external oscillator is used the recommended level is 70mV rms and the unused pin should be left O/C. The input is AC coupled via a 0.01μF capacitor.

A capacitor connected between pin 4 and ground will shunt the mixer output and limit the frequency response of the mixer output and limit the frequency response of the input signal to the second IF amplifier. A value of 33pF is advised when the second IF frequency is 100kHz; 6.8pF is advised for 455kHz.

Phase Locked Loop

The Phase Locked Loop detector features a voltage controlled oscillator with nominal frequency set by an external capacitor equal to (40 ± 7)/f pF, where f is the VCO frequency in MHz. The nominal frequency may differ from the theoretical but there is provision for a fine frequency adjustment by means of a variable resistor between the VCO output pins; a value of 470k has negligible effect while 6.8k (recommended minimum value) increases the frequency by approximately 20%.

Care should be taken to ensure that the free running VCO frequency is correct; because the VCO and limiting IF amplifier output produce square waves, it is possible to obtain lock with the VCO frequency fractionally related to the IF, e.g. IF = 100kHz, VCO = 150kHz. This condition can produce good SINAD ratios but poor squelch performance.

The loop filter is connected between pins 11 and 12; a 33k resistor is also required between pin 11 and Vcc.

The values of the filter resistor R2 and capacitor C1 must be chosen so that the natural loop frequency and damping factor are suitable for the FM deviation and modulation bandwidth required. The recommended values for various conditions are tabulated below:

Centre frequency kHz	Deviation kHz	Resistor kΩ	Capacitor pF
100	5	6.2	2200
100	10	5.6	1800
455	5	4.7	1500
455	10	3.9	1200

Note that the values of loop filter are not critical and in many cases may be omitted.

The AF output voltage depends upon the % deviation and so, for a given deviation, output is inversely proportional to centre frequency. As the noise is constant, the signal to noise ratio is also inversely proportional to centre frequency.

VCO Frequency Grading

The SL6601 is supplied in 3 selections of VCO centre frequency. This frequency is measured with a 390pF timing capacitor and no input signal.

Devices are coded 'SL6601C' and a '/1', '/2', '/3' to indicate the selection.

Frequency tolerances are:

/1 85 - 100kHz (or uncoded)
/2 95 - 110kHz
/3 105 - 120kHz

Note that orders cannot be accepted for any particular selection, but all devices in a tube will be the same selection.

Squelch Facility

When inputs to the product detector differ in phase a series of current pulses will flow out of pin 7. The feature can be used to adjust the VCO; when a 1mV unmodulated input signal is applied to pin 18 the VCO frequency should be trimmed to maximise the voltage on pin 7.

The squelch level is adjusted by means of a preset variable resistor between pin 7 and V_{CC} to set the output signal to noise ratio at which it is required to mute the output. The capacitor between pin 7 and ground determines the squelch attack time. A value between 10nF and 10μF can be chosen to give the required characteristics.

Operation at signal to noise ratios outside the range 5-18dB is not recommended. Where the 'front end' noise is high (because of very high front end gain) the squelch may well never operate. This effect can be obviated by sensible receiver gain distribution.

The load on the squelch output (pin 6) should not be less than 250kΩ. Reduction of the load below this level leads to hysteresis problems in the squelch circuit.

The use of an external PNP transistor allows hysteresis to be increased. See Fig.4. The use of capacitors greater than 1000pF from pin 6 to ground is not recommended.

Outputs

High speed data outputs can be taken direct from pins 11 and 12 but normally for audio applications pin 8 is used. A filter network will be needed to restrict the audio bandwidth and an RC network consisting of 4.7kΩ and 4.7nF may be used.

Layout Techniques and Alignment

The SL6601 is not critical in PCB layout requirements except in the 'straight through' mode. In this mode, the input components and circuits should be isolated from the VCO components, as otherwise the VCO will attempt to 'lock' to itself, and the ultimate signal to noise ratio will suffer.

The recommended method of VCO adjustment is with a frequency measurement system on pin 9. The impedance must be high, and the VCO frequency is adjusted with no input signal.

LOOP FILTER DESIGN

The design of loop filters in PLL detectors is a straight forward process. In the case of the SL6601 this part of the circuit is non-critical, and in any case will be affected by variations in internal device parameters. The major area of importance is in ensuring that the loop bandwidth is not so low as to allow unlocking of the loop with modulation.

Damping Factor can be chosen for maximum flatness of frequency response or for minimum noise bandwidth, and values between 0.5 and 0.8 are satisfactory, 0.5 giving minimum noise bandwidth.

Design starts with an arbitrary choise of f_n, the natural loop frequency. By setting this at slightly higher than the maximum modulation frequency, the noise rejection can be slightly improved. The ratio f_m/f_n highest modulating frequency to loop frequency can then be evaluated.

From the graph, Fig.3 the value of the function

$$\frac{\Phi_e f_n}{\Delta f}$$

can be established for the desired damping factor.

Φ_e - peak phase error
f_n - loop natural frequency
Δf - maximum deviation of the input signal

and as f_n and Δf are known, Φ_e is easily calculated. Values for Φ_e should be chosen such that the error in phase is between 0.5 and 1 radian. This is because the phase detector limits at $\pm\pi/2$ radians and is non linear approaching these points. Using a very small peak phase error means that the output from the phase detector is low, and thus impairs the signal to noise ratio. Thus the choice of a compromise value, and 0.5 to 1 radian is used. If the value of Φ_e achieved is far removed from this value, a new value of f_n should be chosen and the process repeated.

With f_n and D established, the time constants are derived from

$$t_1 + t_2 = \frac{K_o K_D}{(2\pi f_n)^2}$$

$$\text{and } t_2 = \frac{D}{\pi f_n} - \frac{1}{K_o K_D}$$

$K_o K_D$ is $0.3f_o$, where f_o is the operating frequency of the VCO. t_1 is fixed by the capacitor and an internal 20kΩ resistor: t_2 is fixed by the capacitor and external resistor.

$$\text{so } C = \frac{t_1}{2C \times 10^3}$$

$$\text{and } R_{ext} = \frac{t_2 \times 20 \times 10^3}{t_1}$$

In order that standard values may be used, it is better to establish a value of C and use the next lowest standard value e.g. $C_{calc} = 238pF$, use 220pF, as it is better to widen the loop bandwidth rather than narrow it.

The value of R_{ext} is then 'rounded up' by a similar process. It is, however, better to increase R_{ext} to the nearest preferred value as loop bandwidth is proportional $(R_{ext}) - \frac{1}{2}$ while damping factor is proportional to R: thus damping factor is increasing more quickly which gives a more level response.

Example

A frequency modulated signal has a deviation of 10kHz and a maximum modulating frequency of 5kHz. The VCO frequency is 200kHz.

Let f_n = 6kHz and D = 0.5

Then from the graph

$$\frac{\Phi_e f_n}{\Delta f} = 0.85$$

$$\Phi_e = \frac{0.85\Delta f}{f_n} = \frac{0.85 \times 10}{6} = 1.4 \text{ rads.}$$

This is too large, so increase f_n e.g. to 10kHz.

$$\frac{f_m}{f_n} = 0.5 \quad \frac{\Phi_e f_n}{\Delta f} = 0.45$$

$$\Phi_e = \frac{0.45 \times 10}{10} = 0.45$$

- which is somewhat low

Therefore set f_n = 7.5kHz

$$\frac{f_m}{f_n} = 0.666$$

$$\frac{\Phi_e f_n}{\Delta f} = 0.66$$

$$\Phi_e = \frac{0.66 \times 10}{7.5} = 0.88 \text{ rads.}$$

$$t_1 + t_2 = \frac{K_o K_D}{(2\pi f_n)^2}$$

$K_o K_D = 0.3 f_o$ where f_o is the VCO frequency

$$t_1 + t_2 = \frac{0.3 \times 200 \times 10^3}{(2\pi \times 7.5 \times 10^3)^2} = 27\mu s$$

$$t_2 = \frac{D}{\pi f_n} - \frac{1}{K_o K_D}$$

$$= \frac{0.5}{\pi \times 7.5 \times 10^3} - \frac{1}{0.3 \times 200 \times 10^3}$$

$$= 4.5\mu s$$

$$t_1 = 22.5\mu s$$

$$C = \frac{t_1}{20 \times 10^3} = \frac{22.5 \times 10^{-6}}{20 \times 10^3} = 1.125\text{nF (use 1nF)}$$

$$R = \frac{t_2}{t_1} \times 20 \times 10^3$$

$$= \frac{4.5}{22.5} \times 20 \times 10^3$$

$$= 4\text{k}\Omega \text{ (use 3.9k)}$$

Actual loop parameters can now be recalculated

$t_1 = 20\mu s$ $t_2 = 3.9\mu s$

$$2\pi f_n = \frac{(K_o K_D)}{(t_1 \times t_2)} = \frac{(2 \times 10^5 \times 0.3)}{(23.9 \times 10^{-6})} = 50.1\text{k rad/sec} = 7.97\text{kHz}$$

$$D = f_n(t_2 + \frac{1}{K_o K_D}) = \underline{0.515}$$

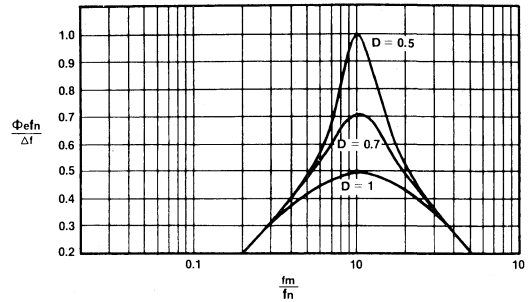


Fig.3 Damping factor

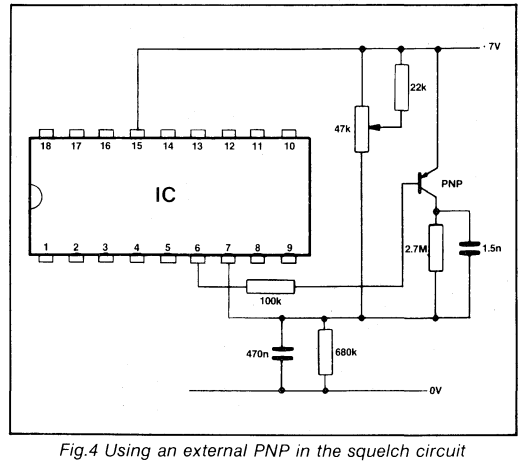


Fig.4 Using an external PNP in the squelch circuit

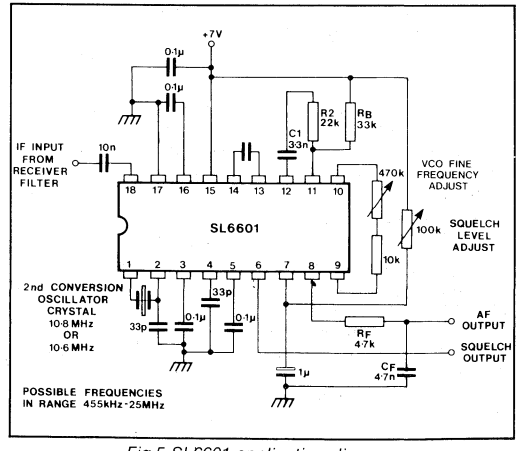


Fig.5 SL6601 application diagram
(1st IF = 10.7MHz, 2nd IF = 100kHz)

TYPICAL CHARACTERISTICS

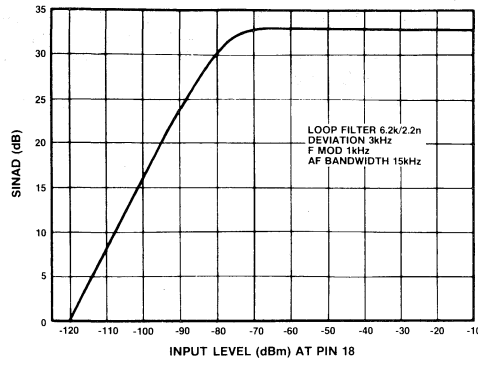


Fig.6 Typical SINAD
(signal + noise + distortion/noise + distortion)

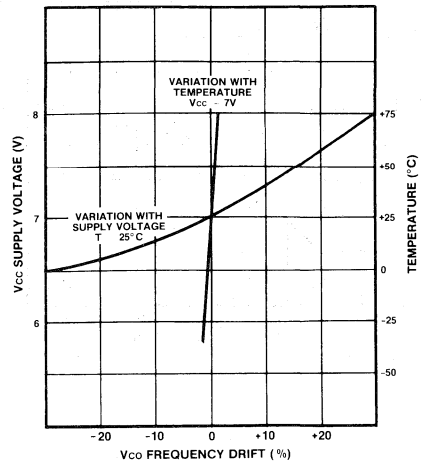


Fig.9 Typical VCO characteristics

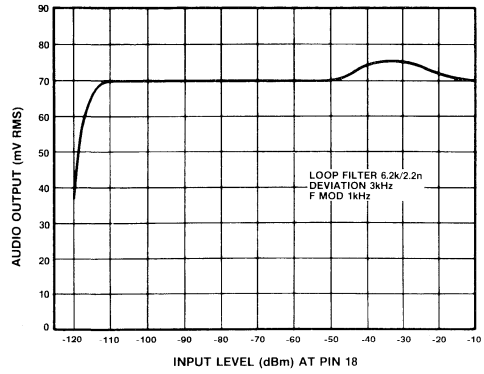


Fig.7 Typical recovered audio v. input level (3kHz deviation)

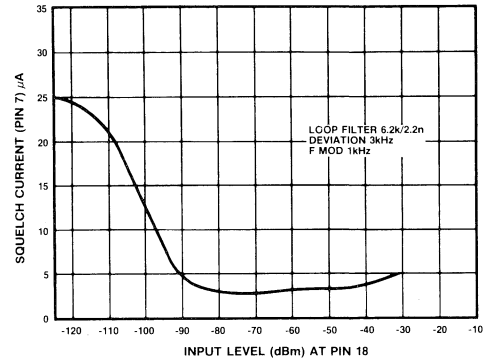


Fig.10 Typical squelch current v. input level

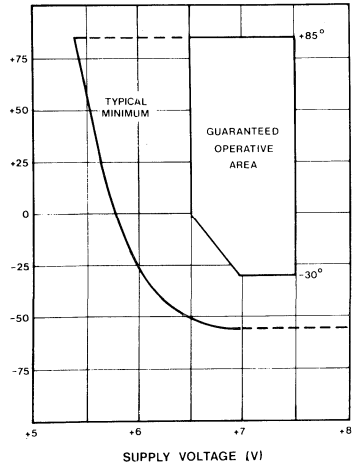


Fig.8 Supply voltage v. temperature

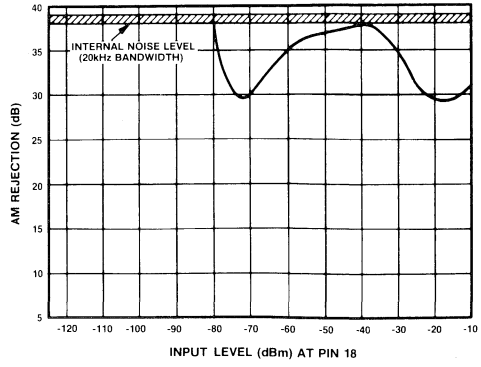


Fig.11 Typical AM rejection

(the ratio between the audio output produced by:
(a) a 3kHz deviation 1kHz modulation FM signal and
(b) a 30% modulated 1kHz modulation AM signal at the same input voltage level.)

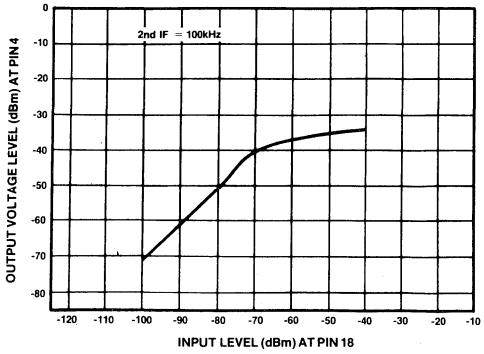


Fig.12 Typical conversion gain (to pin 4)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	9V
Storage temperature	-55° C to +125° C (DP package)
	-55° C to +150° C (DG)
Operating temperature	-55° C to +125° C
(see Electrical Characteristics)	
Input voltage	1V RMS at pin 18

SL6636

LOW POWER BASEBAND DEMODULATOR FOR HIGH SPEED RF DATA LINKS, CT2 DIGITAL CORDLESS TELEPHONES ETC.

The SL6636 is a complete single-chip baseband FM demodulator, primarily intended for use in cordless telephones.

Maximum system integration ensures minimum external component count. On-chip tunable active filters ensure the required adjacent channel and selectivity performance. Special pre-channel filters are also used to provide the required dynamic range.

AGC and RSSI circuits are included to provide the necessary control of suitable PIN attenuator and RF amplifier AGC circuits. Supply current is less than 5mA (excluding PIN drive circuits) from a supply voltage of 5V.

The SL6636 is intended to be used with a high frequency LNA/mixer I/Q IC which will be available shortly.

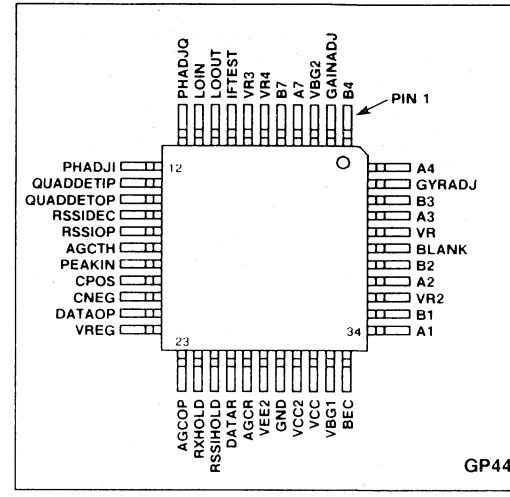


Fig. 1 Pin connections (top view)

FEATURES

- Complete Baseband FM Demodulator in one Package
- CAI Compatible
- On-Chip Filtering
- Minimal External Component Count
- Burst Mode Capability
- AGC and RSSI Detectors
- Low Power Consumption: Typ. 5mA
- Data Slicer with Hold Function
- Power Down Facility for Battery Economy

APPLICATIONS

- Digital Cordless Telephones
- Cordless Data Links

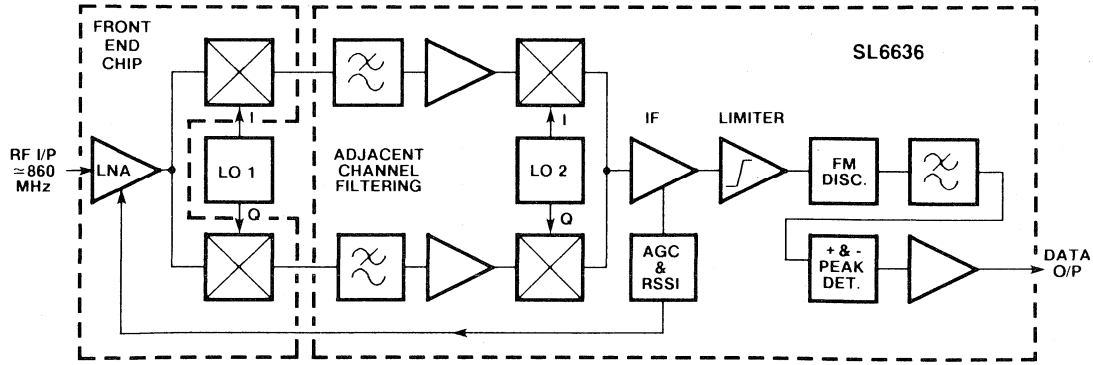


Fig. 2 SL6636 block diagram

PIN DESIGNATIONS

Pin	Pin Name	Description	Pin	Pin Name	Description
1	B4	Channel B output from baseband amp	19	CPOS	Positive data peak detector capacitor
2	GAINADJ	Gain adjust for channel B baseband amp An open emitter that should linked to ground via a series resistor, variable between 10k and 100k (27k nom.)	20	CNEG	Negative data peak detector capacitor
			21	DATAOP	Chip dat output
			22	VREG	VREG from front end chip
			23	AGCOP	AGC output for front end chip
3	VBG2	Bandgap temperature compensated reference voltage. Should be decoupled to VCC	24	RXHOLD	Transmit/Receive reset input
			25	RSSIHOLD	RSSI hold capacitor
			26	DATAR	Data reset input
4	A7	Baseband input to channel A mixer	27	AGCR	AGC reset input
5	B7	Baseband input to channel B mixer	28	VEE2	Data and AGC ground - not connected internally to baseband ground
6	VR4	Mixer voltage reference. Should be decoupled to VCC	29	GND	Baseband ground
7	VR3	IF voltage reference. Should be decoupled to VCC	30	VCC2	Data and AGC VCC - not connected internally to baseband VCC
8	IFTEST	IF waveform inspection pin	31	VCC	Baseband VCC
9	LOOUT	Local oscillator output. Shielded tuned circuit should be connected to LOIN	32	VBG1	Bandgap temperature compensated reference voltage. Should be decoupled to VCC. Internally connected to VBG1
10	LOIN	Local oscillator input			
11	PHADJQ	Local oscillator phase adjust. Open			
12	PHADJI	emitters that should have a 50k pot across them, with the centre tap to ground	33	BEC	Battery economy input
			34	A1	Channel A baseband input
			35	B1	Channel B baseband input
13	QUADDETIP	Quadrature detector input. Shielded quadrature circuit should be connected to VCC	36	VR2	Baseband voltage reference. Should be decoupled toVCC
			37	A2	Channel A roofing filter output
14	QUADDETOP	Quadrature detector output. DC linked to PEAKIN via LC low pass filter	38	B2	Channel B roofing filter output
			39	BLANK	Blanking control input
15	RSSIDEC	RSSI decouple. Capacitor to ground	40	VR	Gyrator voltage reference. Should be decoupled to VCC
16	RSSIOP	RSSI output. DC voltage related to signal level	41	A3	Channel A blanking circuit input
17	AGCTH	AGC threshold adjust. An open emitter that should be linked to ground via a series resistor, variable between 10k and 100k	42	B3	Channel B blanking circuit input
			43	GYRADJ	Gyrator current adjust. An open emitter that should be connected to ground via a series resistor, variable from 5k to 20k (16k nom.)
18	PEAKIN	Data peak detectors input			
			44	A4	Channel A output from baseband amp

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated);

T_{amb} = 0°C to + 70°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	4	5	6	V	
Supply current	I_{CC}	4	5	6	mA	BECLO
				10	µA	BECHI
Bandgap reference	V_{BG}	1.1	1.2	1.3	V	
Voltage reference 1	VR		3.4		V	V_{CC} = 5V
Voltage reference 2	VR2		2.9		V	
Voltage reference 3	VR3		4.3		V	
Voltage reference 4	VR4		3.6		V	
BECHI	BEC	V_{CC}-0.3		0.3	V	
BECLO	BEC				V	Active low
Power supply ripple rejection			50		dB	DC -100kHz
AGC voltage reference from front end chip	V_{REG}		1.6		V	

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = 5V Tamb = +25°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
PREAMP & SALLEN-KEY FILTER						
Input impedance	A1(B1)		50		kΩ	
Frequency response	A1-A2 (B1-B2)		-3		dB	At 130kHz
Absolute delay	A1-A2 (B1-B2)		2.5		μs	At 10kHz
Gain	A1-A2 (B1-B2)		22		dB	At 10kHz
BLANKING						
Input impedance	A3(B3)		50		kΩ	
Gain	A3(B3)		6		dB	At 10kHz
Blanking	A3-A4 (B3-B4)	30			dB	At 10kHz
Blanking pin - Signal	BLANK	V_{CC}-0.3			V	
Blanked	BLANK			0.3	V	
CHANNEL FILTER						
Gain	A4(B4)		-6		dB	At 10kHz
Frequency response	A4(B4)		-35		dB	at 100kHz
	A4(B4)		-3		dB	At 52.5kHz Set by GYR ADJ
Differential group delay			10		μs	1kHz to 50kHz
Absolute delay			11.5		μs	At 10kHz
BASEBAND AMPLIFIERS						
Gain	A4(B4)		25		dB	At 10kHz
Gain adjust range	GAINADJ	±3			dB	Using GAIN ADJ Channel B only
WHOLE BASEBAND ARM						
Gain	A1--A5 (B1-B5)		47		dB	At 10kHz
Equivalent input noise	A1(B1)			28	nV/√Hz	
Absolute delay	A1-A5 (B1-B5)		14		μs	At 10kHz
Third order intercept	A1(B1)	1.6			V	pk-pk with input pole at 150kHz and f_1 = 400kHz, f_2 = 820kHz Intercept at f_2-2f_1 = 20kHz
SECOND MIXERS						pk-pk
Signal input	A7(B7)	2	50	500	mV	pk-pk (internal)
Mixer input from LO (I/Q)			50		mV	
Conversion gain	Note 1		-18		dB	Single input 50mV pk-pk
Carrier leak			-40		dB	
LO leak			-40		dB	
Input impedance (signal)	A7(B7)		50		kΩ	(internal)
Input impedance (LO)			50		kΩ	
LO frequency range			0.6	2	MHz	(AC coupled externally)
Signal frequency range	A7(B7)	0.01	0.03	2000	kHz	

NOTE
1. Conversion gain is measured from A7 (B7) to the internal mixer output

AC ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
SECOND LO						
Frequency range	LOOUT		0.6		MHz	Determined by external L & C
Level	LOOUT		10		mV	pk-pk
I/O phase adjust range	PHADJI/ PHADJQ		±6		degrees	
IF AMPLIFIER						
Gain	IF input-QUADDETIP		70		dB	At 600kHz
QUADRATURE DETECTOR						
Output impedance	QUADDETOP	2.4			kΩ	
Demod sensitivity	PEAKIN		2.2		mV/kHz	With L = 390μH C = 150pF R = 5kΩ
DATA PEAK DETECTOR						
Input impedance	PEAKIN		2.4		kΩ	
Input signal level	PEAKIN		80		mV	pk-pk
Detector attack slew rate			60		mV/μs	C = 4.7nF in peak detector
Positive peak detector sink current	CPOS		0.5		mA(pk)	V_{IN} = 160mV pk
Negative peak detector sink current	CNEG		0.5		mA(pk)	VIN = -160mV pk
Peak detectors discharge current	CPOS/CNEG		2		μA	RXHOLD HI
			100		nA	RXHOLD LO
Data reset input range	DATAR	0.7 V_{CC}				Active Hi
				0.3 V_{CC}		Lo
Data reset I/P impedance	DATAR		100		kΩ	
RXHOLD input range	RXHOLD	0.7 V_{CC}				Active Hi
				0.3 V_{CC}		Lo
RXHOLD I/P impedance	RXHOLD		100		kΩ	
Data output range	DATAOP	V_{CC}-0.3		0.3	V	Hi
					V	Lo
Data output rise time	DATAOP		2		μs	
AGC AND RSSI						
RSSI dynamic range	RSSIOP	20			dB	No AGC feedback loop
Output voltage range	RSSIDEC	0		2.2	V	
Output impedance	RSSIDEC		100		kΩ	
Output voltage range	RSSIOP	0		2.2	V	
Output impedance	RSSIOP		500		Ω	
RSSI attack slew rate			300		mV/μs	V_{IN} = 0-2.2V C = 3.3nF
AGC/RSSI peak detector discharge current	RSSIHOLD		2		μA	RXHOLD Hi
			100		nA	RXHOLD Lo
AGC threshold adjust current	AGCTH		7		μA	External resistor
AGC O/P voltage range closed loop	AGCOP	V_{REG} -350		V_{REG} +350	mV	V_{REG} = V_{REG} on front end chip
Input voltage range	AGCRESET	0.7 V_{CC}				Active Hi
				0.3V_{CC}		Lo
Input impedance	AGCRESET		100		kΩ	
Output impedance	AGCOP		500		Ω	

Hi / Lo: R_L = 25kΩ, C_L = 30pF

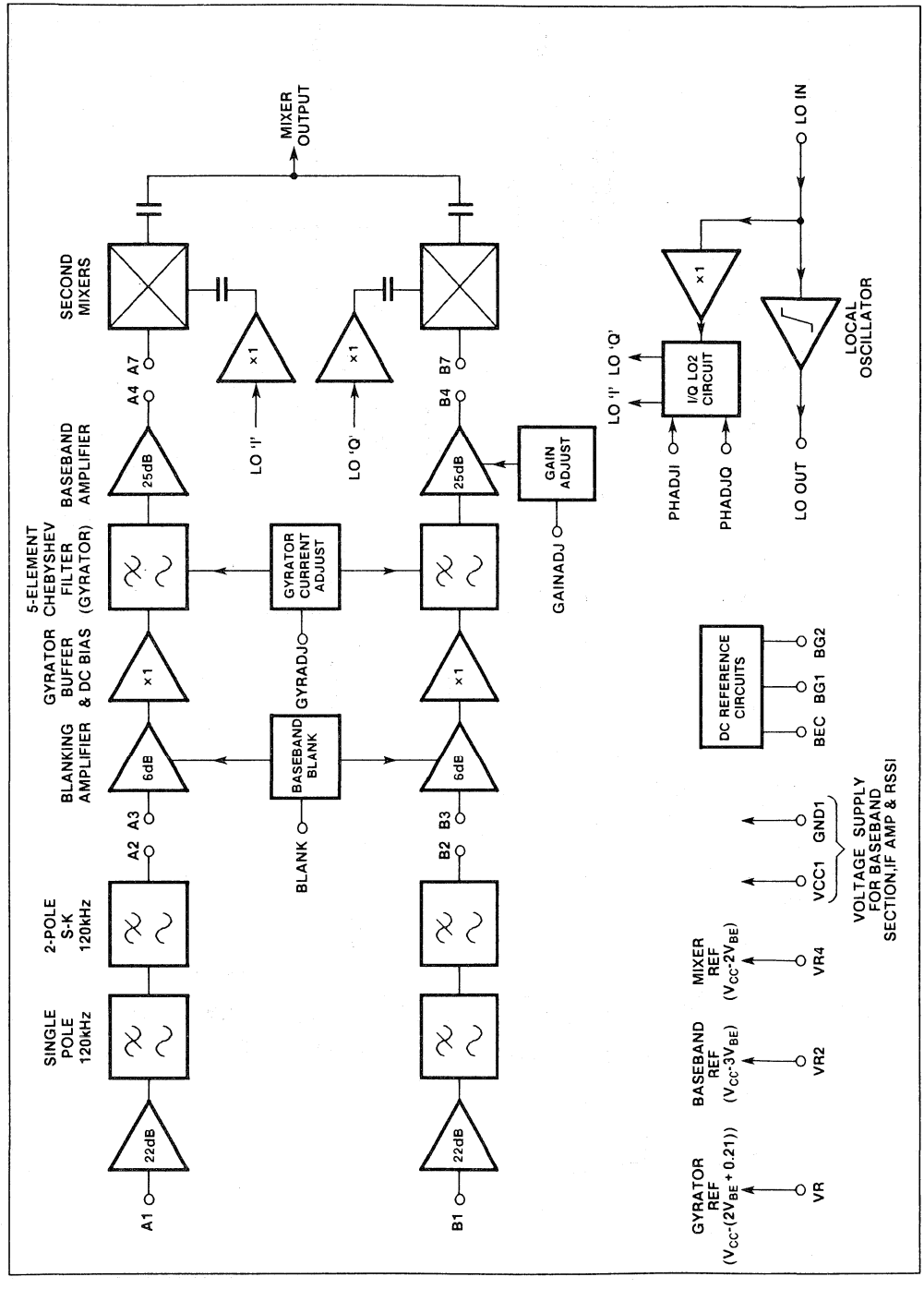


Fig.3 SL6636 block diagram (section 1)

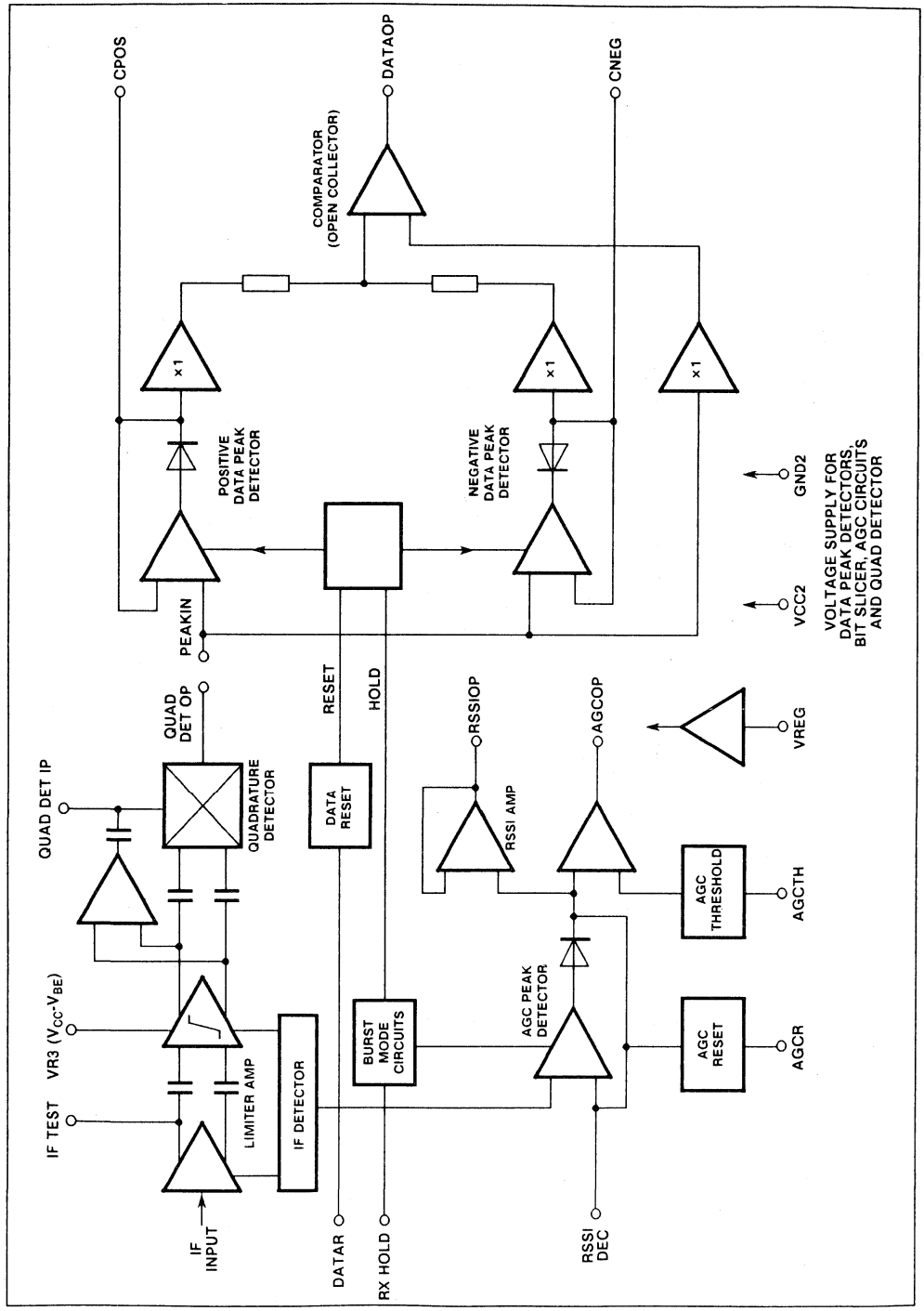


Fig.4 SL6636 block diagram (section 2)

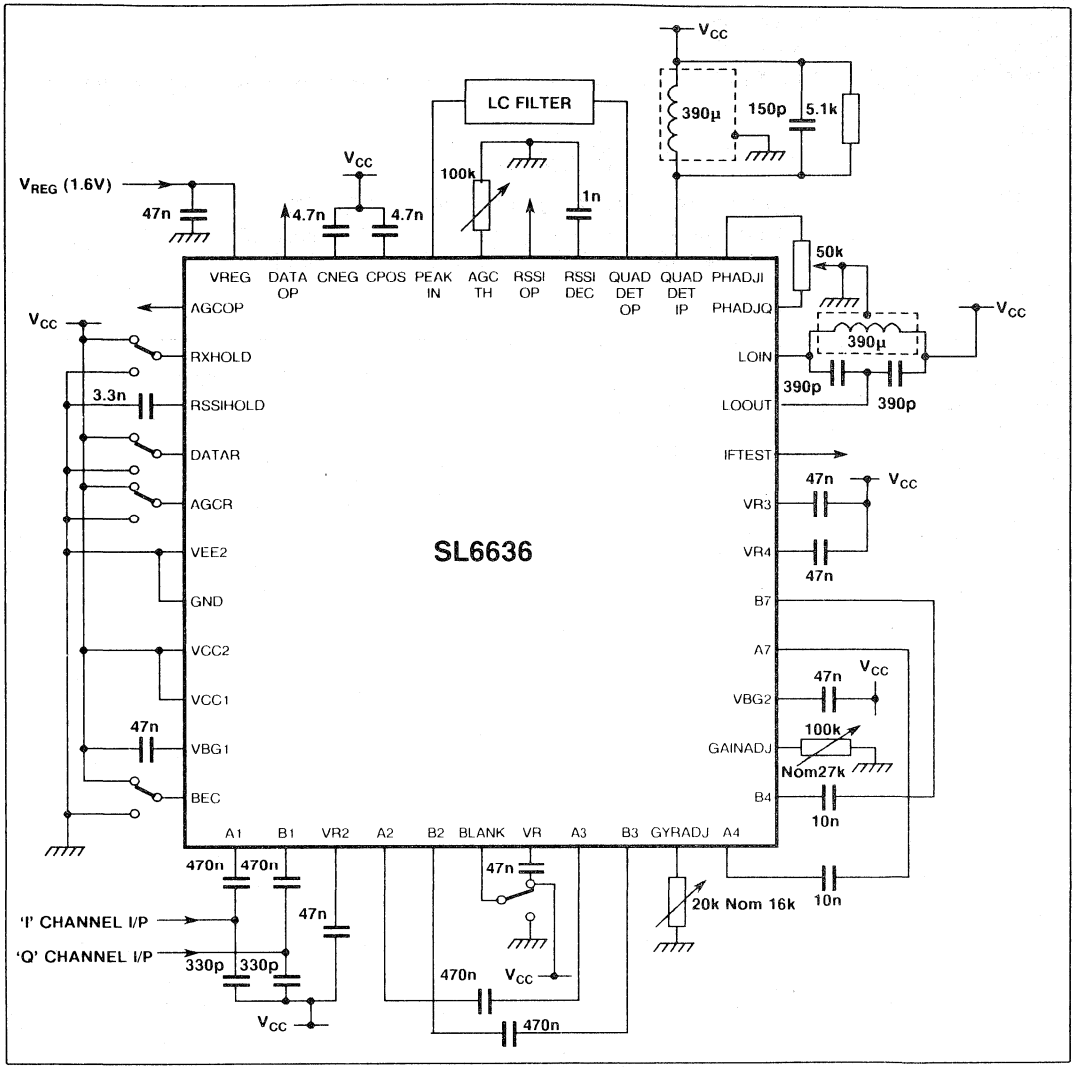


Fig.5 SL6636 test board

SYSTEM DESCRIPTION

The SL6636 and a suitable front end LNA/mixer together form a CT2 radio receiver based on an analog direct conversion FM receiver architecture, as shown in Fig.2. This type of receiver translates the 900 MHz input signal spectrum to baseband and then reproduces the input spectrum centred on an IF of 600kHz. The intermediate conversion to baseband stops the formation of an image frequency and therefore removes the need for image filtering.

The receiver selectivity is achieved at baseband using on-chip gyrator channel filters with an adjustable knee frequency. System signal-to-noise ratio is optimised by cancelling the unwanted sideband which is generated during up conversion to 600 kHz.

Both the knee frequency adjust and the removal of the unwanted sideband by gain and phase adjusts need only to be performed once during initial receiver set-up. Demodulation of the translated signal at 600kHz then takes place using a conventional FM discriminator. Data peak detectors are provided to determine the correct data slice level for the discriminator.

An RSSI (Received Signal Strength Indicator) with a peak hold function is included and from this signal an AGC control signal is generated.

The minimal number of external components required by the SL6636 is shown in Fig.5.

PLESSEY
Semiconductors

SL6637

DIRECT CONVERSION FSK RECEIVER

FOR COMMITMENT ONLY - NOT TO BE USED FOR NEW DESIGNS
RECOMMENDED ALTERNATIVES: SL6638 OR SL6639

The SL6637 is a lower power direct conversion radio receiver for the reception of frequency shift keyed transmissions. It features the capabilities of 'power down' for battery conservation and control of an external DC-DC converter if single cell operation is required. The device also comes equipped with high current beeper drive and low battery flag indicator.

FEATURES

- Very Low Power Operation - Typ. 4mW
- Single Cell Operation
- Complete Radio Receiver in One Package
- Operation Optimised at 200MHz
- 200nV Typical Sensitivity
- Operates at 1200 BPS

APPLICATIONS

- Low Power Radio Data Receiver
- Radio Paging
- Ultrasonic Direction Indication
- Security Systems

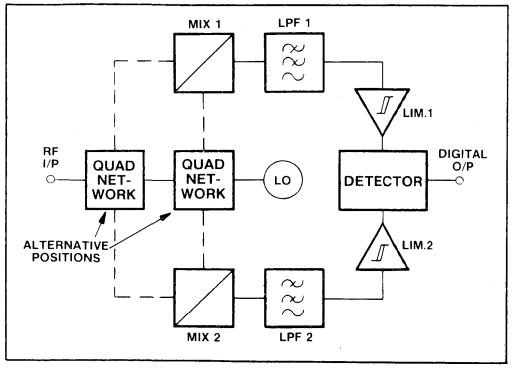
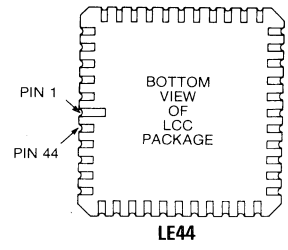


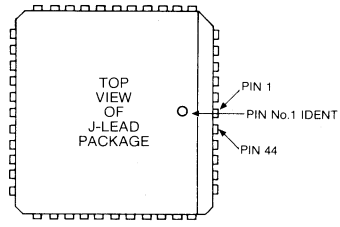
Fig.2 Block diagram

If waveform at limiter '1' input leads waveform on limiter '2' input by 90°, output at detector output will be a high level and low at Data Output.

If waveform at limiter '1' input lags waveform on limiter '2' input by 90°, output at detector output will be a low level and high at Data Output.



LE44



HP44

PIN	FUNCTION	PIN	FUNCTION
1	Detector O/P	23	Mixer 1 O/P
2	BRF I/P	24	Power Down
3	BRF O/P Decoder I/P	25	Vcc2
4	LF Bias Decouple	26	Ground
5	Limiter '1' FB Decouple	27	Ground (Beep)
6	Limiter '1' I/P	28	Low Battery Control
7	Follower Filter O/P	29	Beep O/P
8	Follower Filter I/P	30	Beep Vcc1
9	Amplifier Filter O/P	31	Beep I/P
10	Amplifier Filter I/P	32	Mixer '2' RF I/P
11	Current Source Control (2)	33	Mixer '1' RF I/P
12	Current Source O/P (2)	34	Amplifier Filter I/P
13	Battery Flag	35	Amplifier Filter O/P
14	Osc.Current Source O/P(1)	36	Follower Filter I/P
15	Mixer '1' LO I/P	37	Follower Filter O/P
16	Mixer '2' LO I/P	38	RF Bias Decouple
17	Mixer Bias	39	RF Amplifier O/P
18	Inverter Control O/P	40	RF Ground
19	Reference O/P	41	RF I/P
20	Vcc1	42	Limiter '2' I/P
21	Inverter Control Threshold Adjust	43	Limiter '2' FB Decouple
22	Mixer 2 O/P	44	Decoder O/P

Fig.1 Pin connections

PLESSEY
Semiconductors

SL6638

200MHz DIRECT CONVERSION FSK DATA RECEIVER

The SL6638 is a lower power direct conversion radio receiver for the reception of frequency shift keyed transmissions. It features the capabilities of 'power down' for battery conservation and control of an external DC-DC converter if single cell operation is required. The device also comes equipped with high current beeper drive and low battery flag indicator.

FEATURES

- Very Low Power Operation - Typ. 4mW
- Single Cell Operation
- Complete Radio Receiver in One Package
- Operation Optimised at 200MHz
- 200nV Typical Sensitivity
- Operates at 1200 BPS

APPLICATIONS

- Low Power Radio Data Receiver
- Radio Paging
- Ultrasonic Direction Indication
- Security Systems

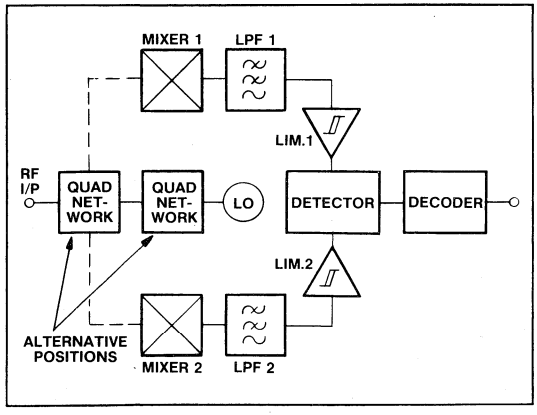
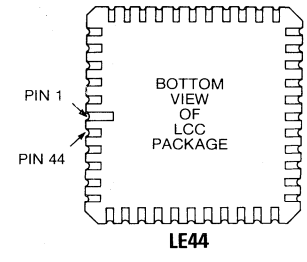


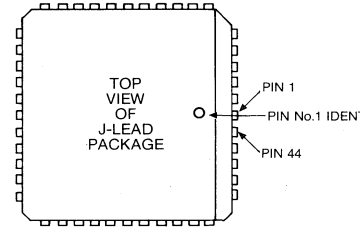
Fig.2 Block diagram (see Fig.5 for detailed schematic)

If waveform at limiter '1' input leads waveform on limiter '2' input by 90°, output at detector output will be a high level and low at decoder output.

If waveform at limiter '1' input lags waveform on limiter '2' input by 90°, output at detector output will be a low level and high at decoder output.



LE44



HP44

PIN	FUNCTION	PIN	FUNCTION
1	Detector O/P	23	Mixer 1 O/P
2	Decoder I/P	24	Power Down
3	Data Ground	25	Vcc2
4	LF Bias Decouple	26	Ground
5	Limiter '1' FB Decouple	27	Ground (Beep)
6	Limiter '1' I/P	28	Low Battery Control
7	Follower Filter O/P	29	Beep O/P
8	Follower Filter I/P	30	Beep Vcc1
9	Amplifier Filter O/P	31	Beep I/P
10	Amplifier Filter I/P	32	Mixer '2' RF I/P
11	Current Source Control (2)	33	Mixer '1' RF I/P
12	Current Source O/P (2)	34	Amplifier Filter I/P
13	Battery Flag	35	Amplifier Filter O/P
14	Osc.Current Source O/P(1)	36	Follower Filter I/P
15	Mixer '1' LO I/P	37	Follower Filter O/P
16	Mixer '2' LO I/P	38	RF Bias Decouple
17	Mixer Bias	39	RF Amplifier O/P
18	Inverter Control O/P	40	RF Ground
19	Reference O/P	41	RF I/P
20	Vcc1	42	Limiter '2' I/P
21	Inverter Control Threshold Adjust	43	Limiter '2' FB Decouple
22	Mixer 2 O/P	44	Decoder O/P

Fig.1 Pin connections

PRINCIPLE OF OPERATION

The incoming signal is split into two parts and frequency-converted to base band. The two paths are produced in phase quadrature (see Fig.2) and detected in a phase detector which provides a digital output. The quadrature network may be in either the signal path or the local oscillator path.

The input to the system is an FSK data modulated signal with a modulation index of 18. This gives a spectrum as in Fig.3. f_1 and f_0 represent the 'steady state' frequencies (i.e. modulated with continuous '1' and '0' respectively). The spectrum in Fig.3 is for reversals (a 0-1-0-1-0-1 etc. pattern) at the system bit rate; f_c is the nominal carrier frequency.

When the LO is at the nominal carrier frequency, then a continuous '0' or '1' will produce an audio frequency, at the output of the mixers corresponding to the difference between f_0 and f_c or f_1 and f_c. If the LO is precisely at f_c, then the resultant output signal will be at the same frequency regardless of the data state; nevertheless, the relative phases of the two paths will reverse between '0' and '1' states.

By applying the amplified outputs of the mixers to a phase discriminator, therefore, the digital data is reproduced.

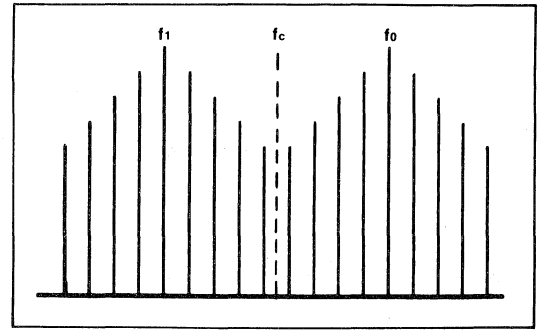


Fig.3 Spectrum diagram

ELECTRICAL CHARACTERISTICS (Use with test circuit Fig.4)

Test conditions: V_{CC1} = 1.3V V_{CC2} = 2.3V T_{amb} = -20°C to +60°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage V_{CC1}	20	0.9		3.5	V	
Supply voltage V_{CC2}	25	1.8		3.5	V	
Supply current I_{CC1}	12,14,15, 16,17,20, 39	0.6	0.8	1.0	mA	Beep off Pin 11 unconnected
Supply current I_{CC2}	25	0.82	1.23	1.64	mA	
Powered-down I_{CC2}	25	60	115	150	μA	
RF amplifier						
Supply current (I_{RF})	39	400	500	650	μA	Pin 40 at 0V
Noise figure			5.5		dB	R_S = 50Ω
Oscillator						
Current source value (I_{OSC1})	14	200	250	350	μA	
Current source value (I_{OSC2})	12	200	250	350	μA	Pin 11 at 0V
Mixers						
Conversion gain		17	21	25	dB	10mV rms signal 10mV rms local oscillator
Input impedance	32,33		500		Ω	
Active filter	10,9					
Inverting amplifiers	34,35					
Input noise			20		nV/√Hz	
Open loop gain			40		dB	Tested as active filters
Input impedance			1		MΩ	using applications CCT
Output impedance			800		Ω	
Active filter	8,7					
Buffer amplifiers	36,37					
Gain			1		v/v	
Input impedance			20		kΩ	
Output impedance			1		kΩ	
Limiting amplifier						
Input impedance	6,42		50		kΩ	
Sensitivity	6,42		20	40	μV	Bit error of 1 in 30 5kHz deviation 500 bps

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Detector						
Output current	1		±5		μA	
Decoder						
Output mark-space ratio	44	7:9		9:7		40μV at limiter input
Output logic high	44	85			% V_{CC2}	
Output logic low	44			15	% V_{CC2}	
Battery economy	24					
Input current				1	μA	
Input logic high		1.5			V	Powered down
Input logic low				0.7	V	Powered up
Beeper driver						
Output saturation voltage	29			300	mV	I load = 50mA
Input current	31			1	μA	
Input logic high	31	1.5			V	Beep on
Input logic low	31			0.7	V	Beep off
Band-gap reference						
Output voltage	19	1.00	1.10	1.25	V	
Battery flag	13					
Output high level		85			% V_{CC2}	Battery high
Output low level				15	% V_{CC2}	Battery low
Flag trigger level		0.9		1.1	V	
Inverter control	18					
V_{CC2} voltage control level		2		2.4	V	Pin 21 unadjusted
Inverter output current			200		μA	Sourced from pin 18
Low battery control	28					
Input logic high		1.5			V	Removes beep drive if battery low
Input logic low				0.7	V	Connects beep drive
Input current				1	μA	

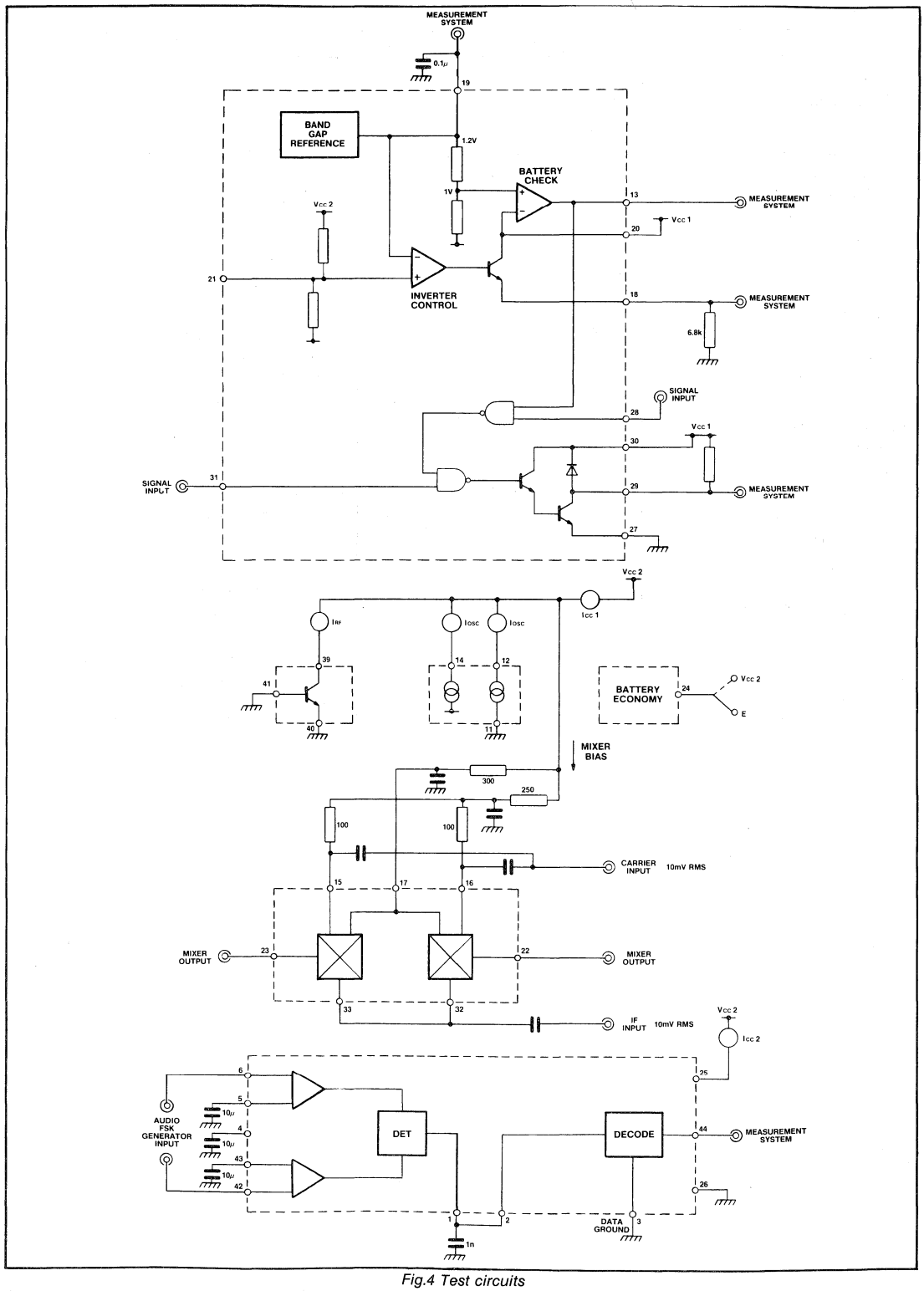


Fig.4 Test circuits

DETAILED DESCRIPTION

The schematic diagram of the SL6638 is shown in Fig.5. The various sub-sections will be described in more detail.

RF amplifier

The RF amplifier consists of a low noise transistor with a high f_t operating at a current of 500μA. It is arranged with a separate emitter connection to ensure stability, and to minimise noise introduction through common return impedances. The collector of this stage is uncommitted for maximum flexibility (transistor c, b, e on pins 39, 41 and 40 respectively) and is biased from a current mirror. The power-down circuitry removes bias from this stage in the standby condition. Typical parameters for this transistor are $\beta \simeq 100$, $rbb^1 \simeq 100\Omega$ and $f_t \simeq 1.2$GHz.

Mixers

The mixers are single balanced active mixers using a PNP current mirror as an active load. Inputs to the mixer are on pins 33 and 32 for the signal, and pins 15 and 16 for the LO. Pin 17 is the LO injection common point and may either be a common but 'live' point when the phase quadrature is used in the RF path or bypassed when quadrature LO drive to the mixers is employed. Emitter follower outputs on pins 23 and 22 ensure that mixer gain is unaffected by the load impedance. The mixers are also powered down on standby.

Local oscillator

A current source on pin 14 and a switchable current source on pin 12 are available for use in a local oscillator.

Inverting amplifiers

The inverting amplifiers have high gain (40dB open loop) and are for use in active low pass filters. The open loop gain is high and is not defined with any accuracy, as closed loop gain is defined by the external filter components.

Buffers

The buffer stages are x1 amplifiers for use in the active low pass filters.

Limiting amplifiers and detectors

These amplifiers provide the main gain block of the receiver system. An input of about 6μV provides limiting, and the inputs are to pins 6 and 42. Pins 4, 5 and 43 are bypass points for the amplifier bias points, while pin 1 is the digital output from the phase detector.

Decoder

The decoders function is to act as a low pass filter to the modulation frequency, and may be configured as an active LPF if desired. It should however, be designed as a very high impedance active LPF as the drive from the detectors is at a high impedance. Alternatively, the connection of a small capacitor to ground from the input is generally adequate for most applications.

Beeper drive

The beeper drive stage accepts an input from an external source and provides a high current drive to the beeper. This current drive can be as high as 200mA, and the arrangement is such that the output waveform may be modified when the battery is near end of life. This modified waveform is generated externally (and applied to pin 28). The internal band gap reference is 1.2V and this is divided down to a suitable voltage.

Inverter control

This output is available (on pin 18) to control an external inverter. It is derived from the ratio of the internal reference to the V_{CC2} line, and moves in phase with changes in the V_{CC2} line.

Pin 21 allows the value of the inverted voltage supply to be adjusted.

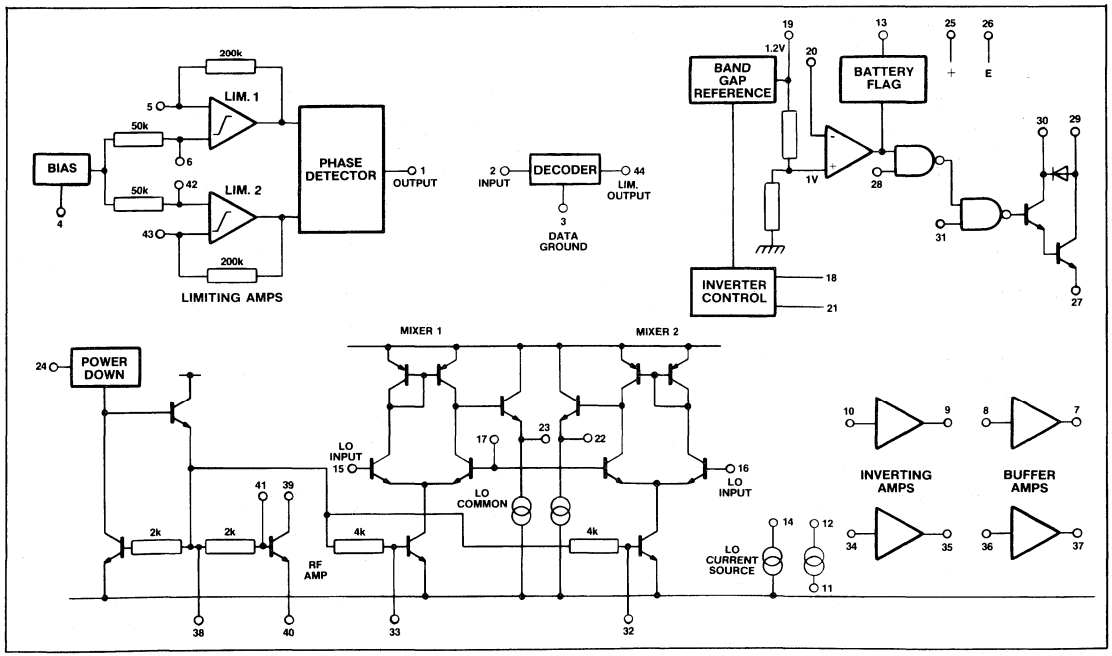


Fig.5 SL6638 schematic diagram

APPLICATIONS

The SL6638 is intended for applications at low data rates and high deviation (e.g. 512 and 1200 B.P.S. and ±4.5kHz deviation). Operation at a ratio of deviation to data rate of less than 6 is not recommended.

The choice of circuitry is dependent upon the system requirements. For example, operation from a single Leclanche or alkaline cell at a nominal 1.4V requires the use of an external inverter, while operation from a single 3 volt Lithium cell does not.

In the radio receiver application, a major decision is the positioning of the quadrature phase shift network. This network may be in the RF or the local oscillator paths, and each method has its advantages and disadvantages. Briefly, these are as follows:

1. **Local oscillator path.** This enables minimum RF loss to be attained. It requires a higher LO drive power to overcome the inevitable losses in the phasing network.
2. **RF signal path.** This method has the advantage that greater isolation may be achieved from the signal to the local oscillator - see Fig.6.

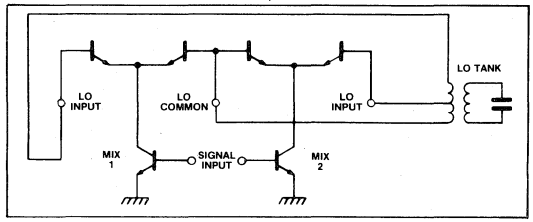


Fig.6 Local oscillator drive

The common mode rejection of the differential stages is used to its maximum advantage in this arrangement.

The form of the quadrature network is not critical. However, the use of an RC network as in Fig.7 has the disadvantage at VHF of being more subject to stray capacities than other methods.

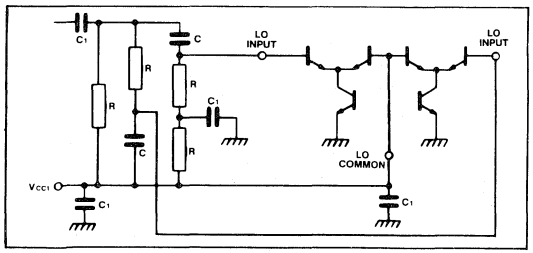


Fig.7 Quadrature LO drive

In the circuit of Fig.7, C_1 is a bypass capacitor, while $X_C = R$ at the operating frequency. Note that the resistances between the local oscillator inputs are equal to minimise DC offsets. The quadrature network can be achieved by coupled circuits (Fig.8) or a hybrid network (Fig.10).

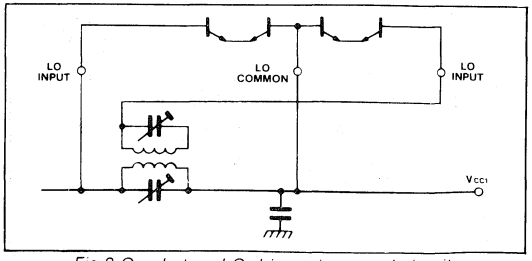


Fig.8 Quadrature LO drive using tuned circuits

In the method shown in Fig.8, the tuned circuits are adjusted to resonance, and are then detuned, one HF and the other LF, to achieve a 3dB drop in output from each one. This gives a +45° and -45° relative phase shift.

The quadrature hybrid network is well covered in the literature and is shown in Fig.9.

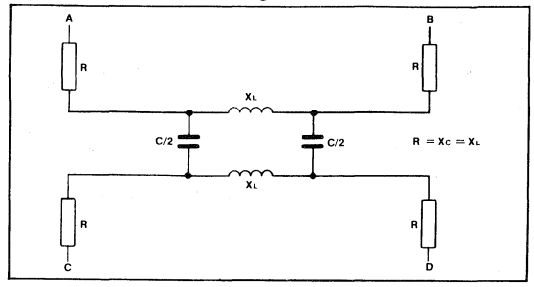


Fig.9 3dB quadrature coupler

The phase relationships are (A) input, (B) 90°, (C) 0° and (D) isolated. The circuit of Fig.10 may be used.

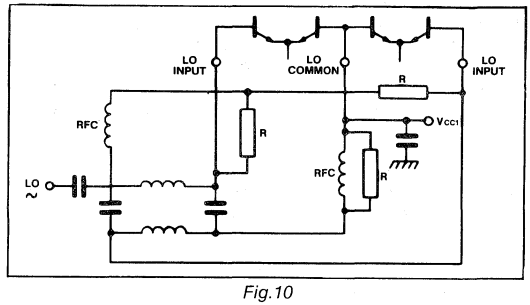


Fig.10

With a suitable local oscillator design some simplification occurs. In addition, it is possible to omit the resistors terminating the hybrid junction, although some mismatch then occurs.

Local oscillator

Because of the wide frequency range over which the SL6638 will operate, it is not possible to define which oscillator to use. Because of this, the oscillator provision is two uncommitted current sources which allows maximum flexibility. A typical overtone oscillator is shown in Fig.11.

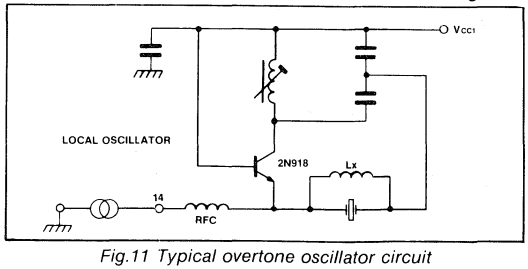


Fig.11 Typical overtone oscillator circuit

Lx is necessary with higher order overtone crystals to suppress oscillation at either the fundamental crystal frequency or as a form of Colpitts with no relation to the crystal frequency.

For lower frequencies, a simple oscillator may well be adequate as shown in Fig.12.

The choice of oscillator and quadrature network are dependent upon the application and no hard and fast rules can be formulated.

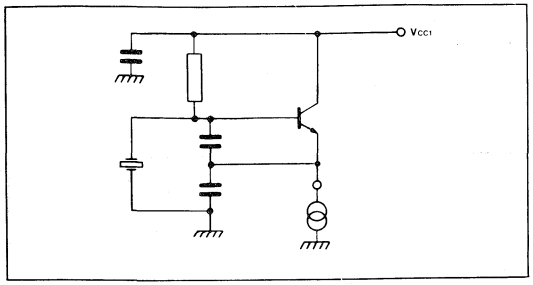


Fig.12 Fundamental LO circuit

Active filters

In any direct conversion receiver, the active filters provide the primary receiver selectively. The attenuation on the adjacent channel must be sufficient to prevent the limiting amplifiers from being driven into limiting by the unwanted signal; provided that this does not occur, then an adjacent channel signal has no effect.

The filter amplifiers consist of two stages for each channel, viz:

(a) An inverting amplifier with an open loop gain of about 40dB, and a gain-bandwidth product of 50kHz.

(b) A buffer stage with a x1 non-inverting gain.

Any of the standard variations of low pass filter can be used; however, design should ensure that differential group delay between the maximum possible error in mark and space frequencies is not excessive. The error in mark and space frequencies is caused by errors in the LO and received frequencies; an error in these frequencies leads to mark and space conditions producing different frequencies, and it is the differential group delay between these frequencies that must be minimised. This is especially important at data rates which are high in comparision with the deviation i.e. low values of modulation index m.

Decoder

The decoder may be connected as an active filter. It should however be a group delay equalised ('linear phase') filter, and the input capacitance should be minimised, as it is driven from a high impedance at the output of the detectors. It is perfectly satisfactory, however, to connect a 1000pF capacitor from the detector output to ground for bit rates up to 512 B.P.S.

Beeper drive

This output has a high current drive capability, suitable for driving beepers in pagers, or as a relay driver in other applications (Fig.13).

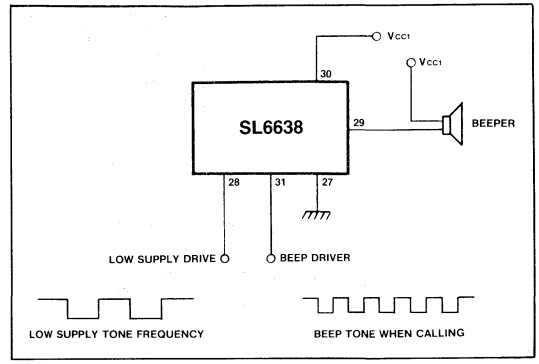


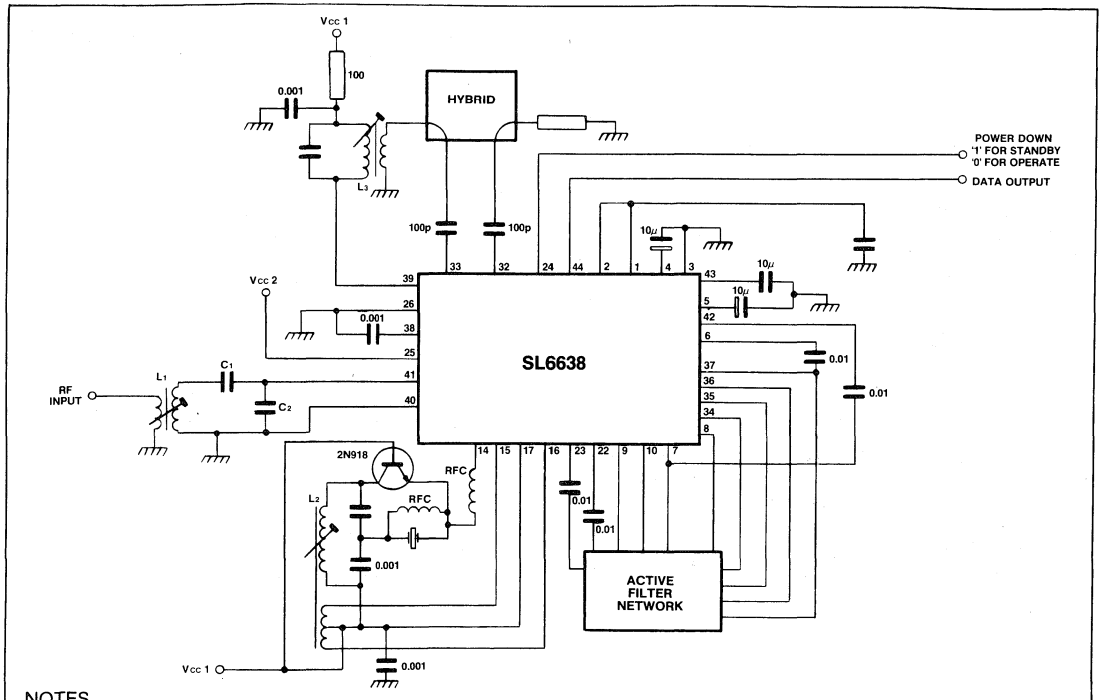
Fig.13 Beeper drive circuit

An internal diode connects pin 29 to pin 30 to protect the driver transistor when used with inductive loads.

The circuit allows for a modification of the beep output when the battery flag has operated. The low battery control pin 28 has no effect whilst the battery is high. When the battery is low pin 28 will override the beep input, a logic high will remove beep drive and a logic low will connect beep drive. Therefore wiring pin 28 high will stop the beeper when the battery is flat, while wiring a logic low on pin 28 will cause the beeper to ignore the battery flag. Putting a low frequency on pin 28 will modulate the beep tone giving a warbling effect when the battery is flat.

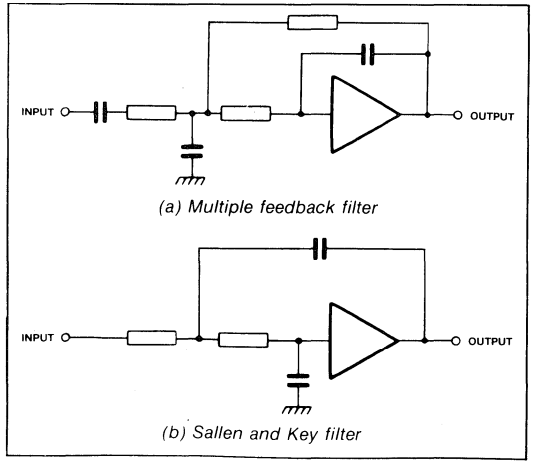
Typical application

Fig.14 shows a typical application as an FSK receiver for 512bps with a frequency deviation of ±4.5kHz. Typical sensitivity is of the order of 0.2μV for a 1 in 30 ber (bit error rate). The circuit as shown in Fig.13 uses a 9th overtone crystal and is usable to approximately 180MHz.



NOTES
Circuits L_1, C_1, C_2, L_2, L_3, resonate at the operating frequency. RFC1 suppresses oscillation at the crystal fundamental. RF level at pins 15 and 16 should be 10-20mV rms. For active filter network design, see Fig.15.

Fig.14 Typical application



(a) Multiple feedback filter

(b) Sallen and Key filter

Fig.15 Active filters. Component values may be determined from the standard books on active filter design.

The RF level at pins 15 and 16 can be increased which will increase the gain, but care must be taken with re-radiation from the input.

Operation at higher or lower frequencies is possible with appropriate external components.

USE OF SL6638 FROM ONE SUPPLY

For minimum power dissipation the SL6638 should be used with one cell (V_{CC1}) and an inverter (V_{CC2}). To operate from just one supply (V_C) certain precautions need to be taken.

Pin 25 will now be connected to Vc. Pins 12,14,39 can be returned to Vc through the same components as for two supply operation. Pins 15,16,17 are normally biased from V_{CC1} and cannot be connected directly to Vc. One diode volt drop down from the supply Vc is usually sufficient,see Fig.16.

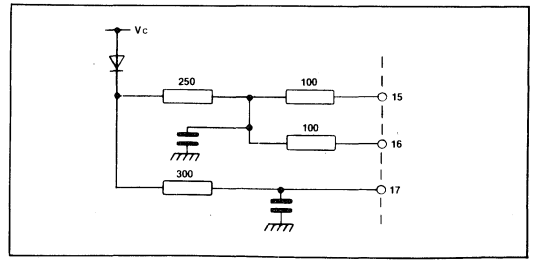


Fig.16

Pin 20 is usually connected to V_{CC1} when it is used to supply current to the inverter circuit and as an input to the battery check. For single voltage operation the inverter will not be required therefore pin 18 can be wired to Vc to disable the inverter. Pin 20 can still be used as a battery check by potting down the supply to pin 20, see Fig.17.

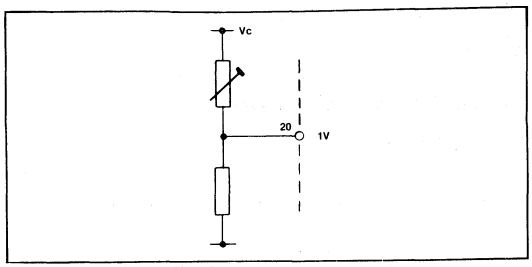


Fig.17

Pins 29,30 of the beeper driver are normally connected to V_{CC1}. These can be connected to Vc but the driver to the output transistor may then be excessive in any particular application. To reduce the drive a resistor may be included from pin 30 to Vc, see Fig.18.

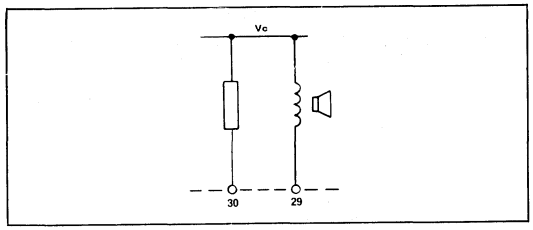


Fig.18

BATTERY ECONOMY

Function	Battery economised
RF amplifier	Yes
Osc current sources	Yes
Mixers	Yes
Active filters	Yes
Limiting amplifiers	No
Phase detector	Yes
Decoder	Yes
Band-gap reference	No
Battery check/flag	No
Inverter control	No
Low battery control	No
Beeper driver	No

Functions that are economised above will have their bias removed during power-down. Functions that are not economised will not be affected during power-down.

SL6639

200MHz DIRECT CONVERSION FSK DATA RECEIVER

(SUPERSEDES NOVEMBER 1989 EDITION)

The SL6639 is a low power direct conversion radio receiver for the reception of frequency shift keyed transmissions. It features the capability of 'power down' for battery conservation.

The device also includes high current beeper drive, high current LED driver and low battery flag indicator.

FEATURES

- Very Low Power Operation - typ. 5mW
- Single Cell Operation with External Inverter
- Complete Radio Receiver in one Package
- Operation up to 200MHz
- 200nV Typical Sensitivity
- Operates at 1200 BPS
- On-Chip Tunable Active Filters
- Minimum External Component Count
- Low Power Down Current - 3μA (Typ.)

APPLICATIONS

- Low Power Radio Data Receiver
- Wristwatch/Credit Card Pager
- Radio Paging
- Ultrasonic Direction Indication
- Security Systems

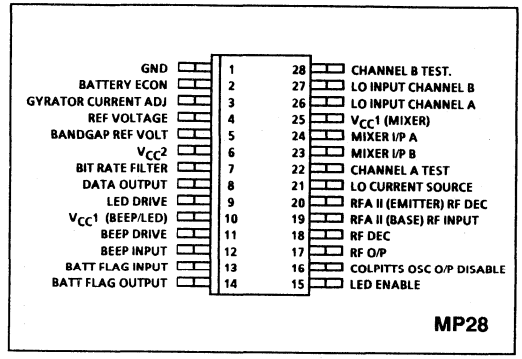


Fig.1 Pin connections (top view)

ABSOLUTE MAXIMUM RATINGS

Supply voltage 8V
Storage temperature -55°C to +150°C
Operating temperature -20°C to +60°C

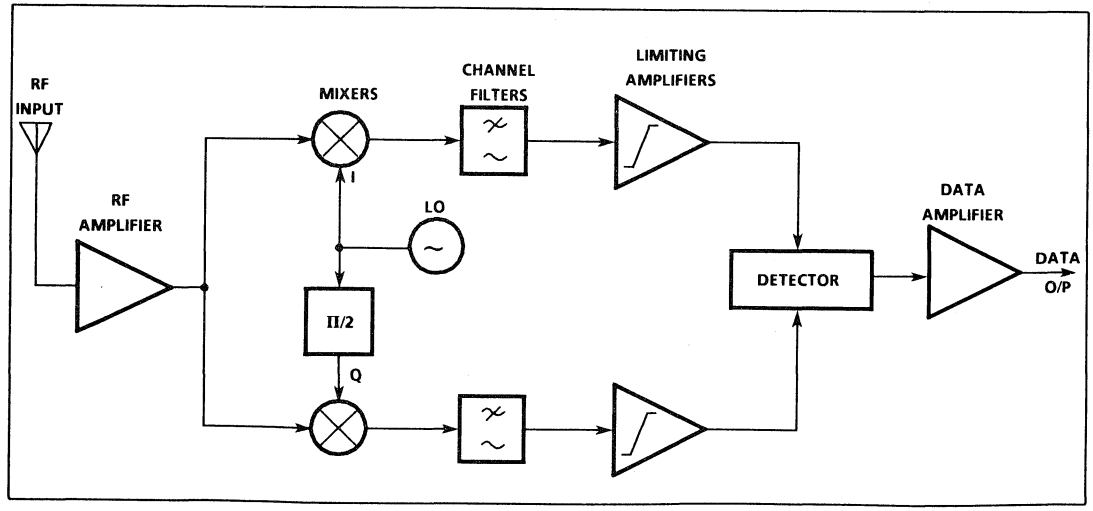


Fig. 2 Block diagram of SL6639 Direct Conversion Receiver

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
$T_{amb} = 25°C$, $V_{CC}1 = 1.3V$ $V_{CC}2 = 2.3V$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage V_{CC} 1	10, 25	0.9	1.3	3.5	V	
Supply voltage V_{CC} 2	6	1.8	2.3	3.5	V	
Supply current I_{CC} 1	10, 25		1.6		mA	(Beeper + LED) off
Supply current I_{CC} 2	6		0.5		mA	(Beeper + LED) off
Power down I_{CC} 1	10, 25		3		μA	Battery Economy I/P low
Power down I_{CC} 2	6		3		μA	Battery Economy I/P low
Bandgap reference	5		1.2		V	
Voltage reference	4		1.0		V	
RF Amplifier						
Supply current (I_{RF})	17		500		μA	
Noise figure			5.5		dB	
Voltage gain			14		dB	
Input impedance	19					See Fig.8
Mixers						
RF input impedance	23, 24					
LO input impedance	26, 27					
Oscillator						
Current source	21		250		μA	
Detector						
Output current	7		±4		μA	
Decoder						
Output mark/space ratio	8	7:9		9:7		
Output logic high	8	85			$\%V_{CC}2$	
Output logic low				15	$\%V_{CC}2$	
Battery Economy						
Input logic high	2	$V_{CC}2$ -0.3			V	Powered up
Input logic low	2			0.3	V	Powered down
Input current				1	μA	
Beeper Driver						
Beeper driver current	11			200	mA	Pin 12 high
Input logic high	12	1.5			V	Beeper on
Input logic low	12			0.5		Beeper off
Input current				1	μA	

ELECTRICAL CHARACTERISTICS (Continued)

Test conditions (unless otherwise stated)
T_{amb} = 25°C, V_{CC} 1 = 1.3V $V_{CC}2$ = 2.3V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Battery Flag						
Output high level	14	85			%$V_{CC}2$	Battery high
Output low level	14			15	%$V_{CC}2$	Battery low
Flag trigger level	13	0.9		1.1	V	
LED						
Oscillator frequency	9	32			kHz	Pin 15 high
Output current	9			50	mA	Pin 15 high
Input logic high	15	1.5			V	LED enable
Input logic low	15			0.5	V	LED disable
Input current	15			1	μA	

PRINCIPLE OF OPERATION

The incoming signal is split into two parts and frequency converted to baseband. The two paths are produced in phase quadrature (see Fig. 2) and detected in a phase detector which provides a digital output. The quadrature network may be in either the signal path or the local oscillator path.

The input to the system is an FSK data modulated signal with a modulation index of 18. This gives a spectrum as in Fig. 3, where f_1 and f_0 represent the 'steady state' frequencies (i.e. modulated with continuous '1' and '0' respectively). The spectrum in Fig. 3 is for reversals (a 0-1-0-1-0-1 etc. pattern) at the system bit rate; f_c is the nominal carrier frequency).

When the LO is at the nominal carrier frequency, then a continuous '0' or '1' will produce an audio frequency at the output of the mixers, corresponding to the difference between f_0 and f_c or f_1 and f_c. If the LO is precisely at f_c, then the resultant output signal will be at the same frequency regardless of the data state; nevertheless, the relative phases of the two paths will reverse between '0' and '1' states. By applying the amplified outputs of the mixers to a phase discriminator, therefore, the digital data is reproduced.

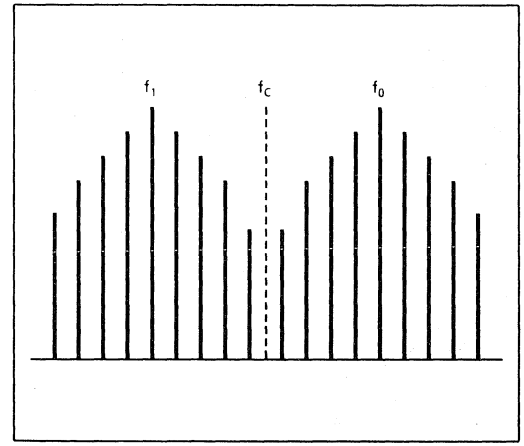


Fig.3 Spectrum diagram

RECEIVER CHARACTERISTICS

Test conditions (unless otherwise stated): Applications circuit diagram Fig.7; $V_{CC}1$ = 1.3V; $V_{CC}2$ = 2.3V; T_{amb} = 25°C; Colpitts oscillator frequency adjusted to 15kHz; mixer input A and B phase balance = 180°; local oscillator input A and B phase balance = 90°.Measurement methods as described by CEPT Res 2 specification.

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Terminal sensitivity tone only 4/5 call reception		-124		dBm	Δf = 4.5kHz
Deviation acceptance		±2.5		kHz	
Centre frequency acceptance		±4		kHz	Δf = 4.5kHz fm = 256Hz
Adjacent channel rejection		70		dB	Δf = 4.5kHz Channel Spacing 25kHz
Adjacent +1 channel rejection		70		dB	Δf = 4.5kHz Channel Spacing 25kHz
Third order intermod adj-1 + adj-2		55		dB	Δf = 4.5kHz Channel Spacing 25kHz

TUNING THE CHANNEL FILTERS

The adjacent channel rejection performance of the SL6639 receiver is determined by the gyrator channel filters. To obtain optimum adjacent channel rejection, the channel filters' cut-off frequency should be set to 8kHz. The process tolerances are such that the cut-off frequency cannot be defined accurately in manufacture, hence the channel filters must be tuned externally.

Tuning is performed by adjusting the current in the gyrator circuits. This changes the values of the gyrators' equivalent inductance. To define the cut-off frequency of the channel filters accurately, a gyrator-based Colpitts oscillator circuit has been included on the SL6639. The oscillator and channel filters use the same type of architecture, hence there is a direct correlation between the Colpitts oscillator frequency and filter cut-off frequency. By knowing the oscillator frequency the channel filter cut-off frequency can be estimated from the oscillator/filter characteristic, Fig. 4.

Once the channel filters have been tuned it is necessary to disable the oscillator by connecting the Colpitts Oscillator output/disable pin (CO, pin 16) to $V_{CC}2$. This is required since continuous oscillation could impair the performance of the receiver.

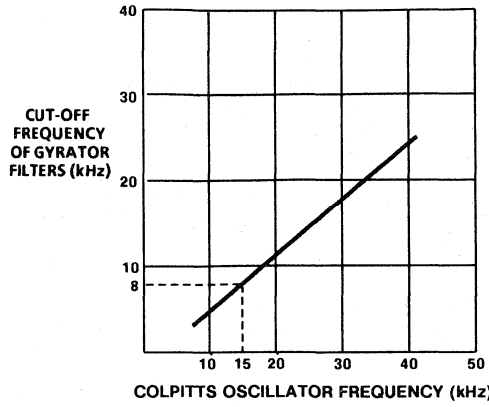


Fig.4 Oscillator frequency v. gyrator filter cut-off frequency

RF TUNING PROCEDURE

There are two tuned circuits which require adjustment fo maximum sensitivity. These are the LO tuned load (T1, C18 and C19) and the RF amplifier tuned load (T2 andC4).

The adjustable core of T1 is tuned to give maximum LO signal at the nominal crystal frequency. This may be measured using a high-Z probe at the junction of C17 and R4.

The RF amplifier load is initially tuned by injecting at the RF input a signal of about 50μV, unmodulated and offset from the nominal crystal frequency by 2-3 kHz.

The output at pin 22 or pin 28 is monitored on an oscilloscope and the core of T2 adjusted for maximum p-p sinewave. It is then necessary to monitor the data output on pin 8 and inject at the RF input a normally modulated signal at the nominal crystal frequency, at a level close to the sensitivity threshold (about -124dBm). The core of T2 is slightly detuned to produce the best bit error rate.

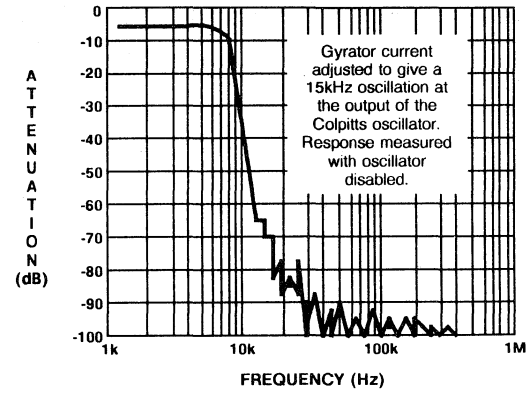


Fig.5 Channel filter response

COMPONENT LIST FOR FIG.6

Capacitors				Resistors		Inductors		Transformers	
C1	1nF	C11	1nF	R1	2.2kΩ	L1	10μH	T1	1:1 transformer
C2	1nF	C12	1nF	R2	200kΩ variable	L2	220nH	T2	Primary/secondary inductance = 200nH
C3	1nF	C13	10pF	R3	12kΩ	L3	150nH		
C4	5.6pF	C14	1nF	R4	100Ω	L4	470μH (optional)	T3	Primary 3T, secondary 4T
C5	1nF	C15	10pF	R5	100Ω	L5	10μH (optional)	**Miscellaneous**	
C6	2.2μF	C16	1nF	R6	100Ω				
C7	2.2μF	C17	5.6pF	R7	100Ω			IC1	SL6639
C8	1nF	C18	4.7pF					TR1	SOT-23 transistor with $f_t \geq 1.3$GHz
C9	2.2μF	C19	10pF					X1	153MHz 7th overtone crystal
C10	2.2μF	C20	1nF						

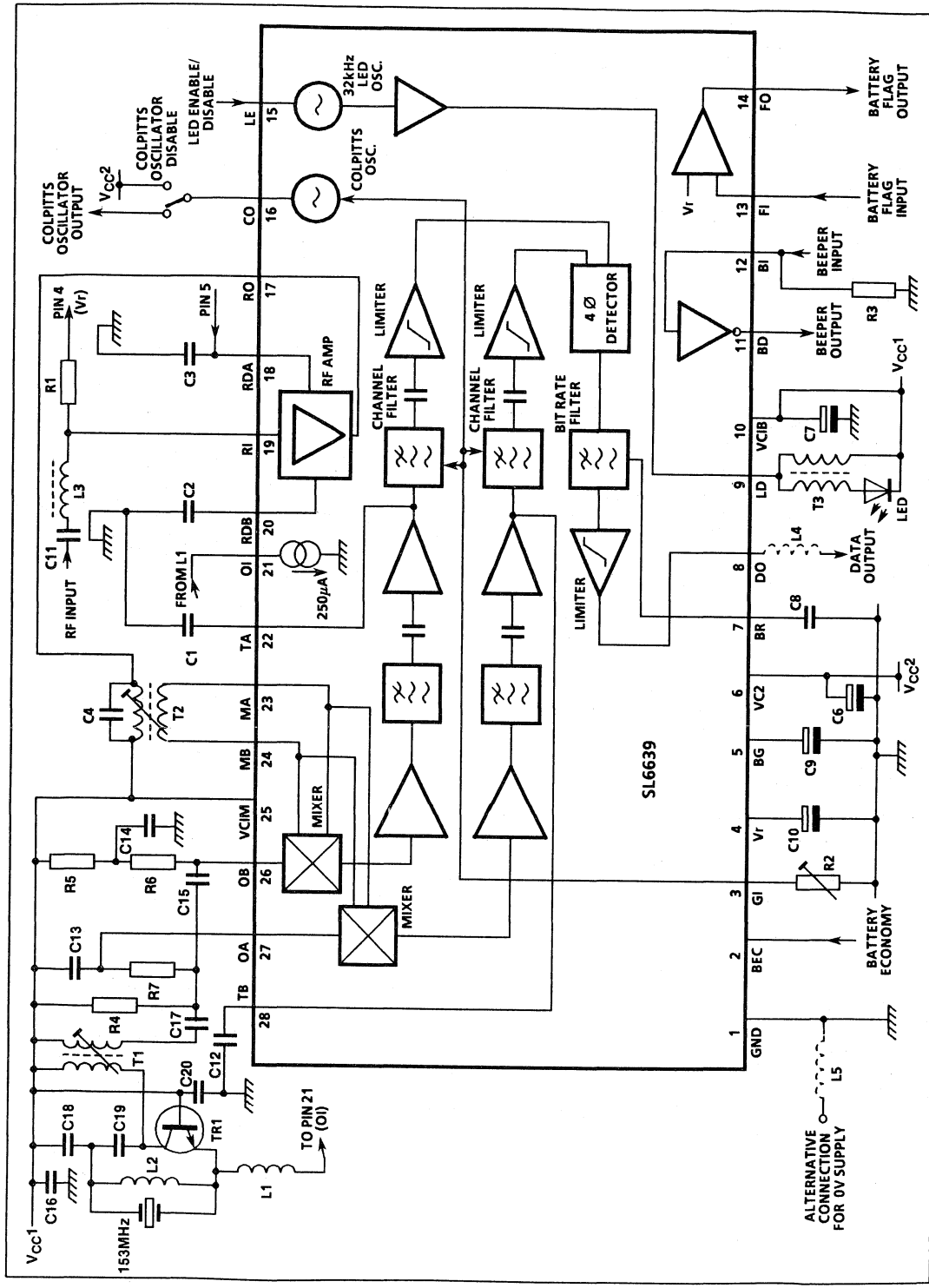


Fig.6 SL6639 block diagram and application circuit

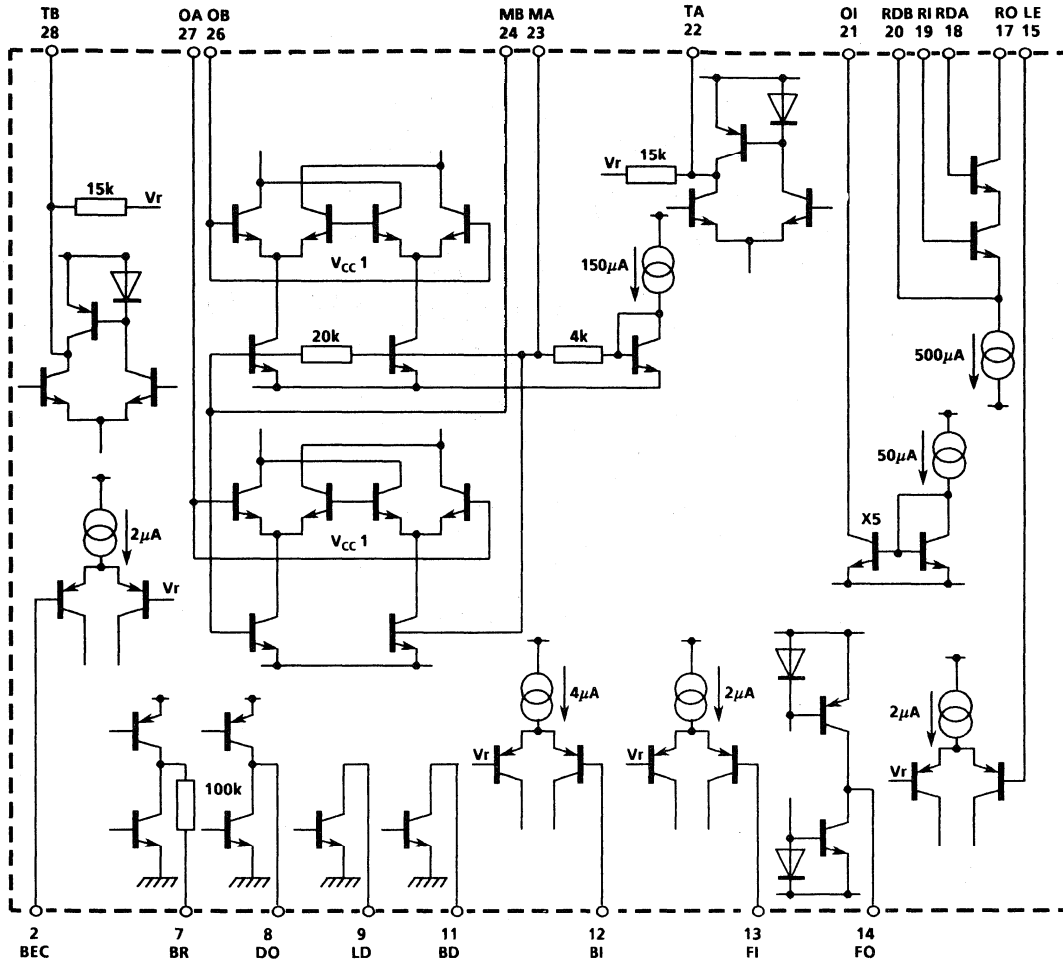


Fig.7 Pinning diagram of the SL6639

PIN	MNEMONIC	FUNCTION
1	GND	Ground
2	BEC	Battery Economy
3	GI	Gyrator Current Adjust
4	Vr	Reference Voltage
5	BG	Bandgap Reference Voltage
6	Vc2	V_{cc} 2
7	BR	Bit rate Filter
8	DO	Data Output
9	LD	LED Driver
10	Vc1B	V_{cc} 1 (Beep/LED)
11	BD	Beep Driver
12	BI	Beep Input
13	FI	Battery Flag Input
14	FO	Battery Flag Output

PIN	MNEMONIC	FUNCTION
15	LE	LED Enable
16	CO	Colpitts Oscillator Output/Disable
17	RO	RFA I (collector) RF Output
18	RDA	RFA I (base) RF Decouple
19	RI	RFA II (base) RF Input
20	RDB	RFAII (emitter) RF Decouple
21	OI	LO Current Source
22	TA	Channel A Test
23	MA	Mixer I/P A
24	MB	Mixer I/P B
25	VCIM	V_{cc}1 (mixer)
26	OB	LO Input Channel B
27	OA	LO Input Channel A
28	TB	Channel B Test

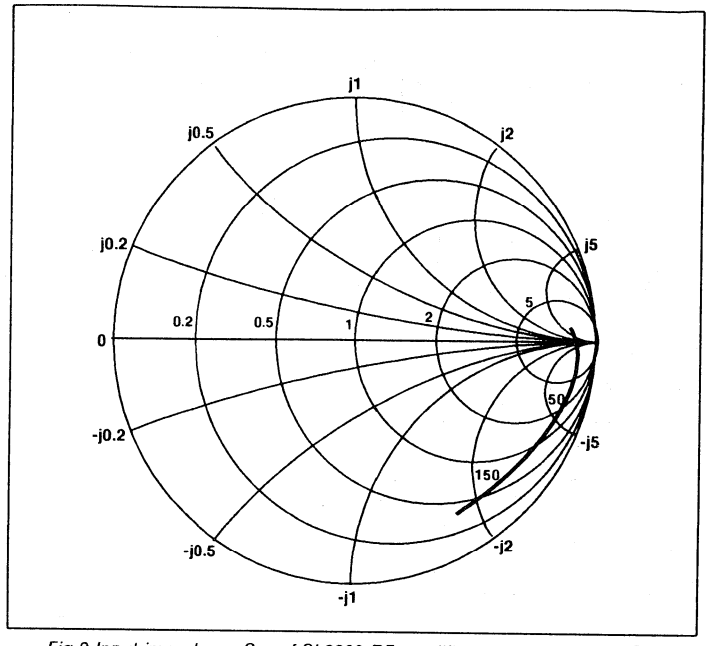


Fig.8 Input impedance S_{11} of SL6639 RF amplifier (normalised to 50Ω)

PLESSEY
Semiconductors

SL6652

LOWER POWER IF (AF CIRCUIT (WITH RSSI) FOR FM CELLULAR RADIO

The SL6652 is a complete single chip mixer/oscillator, IF amplifier and detector for FM cellular radio, cordless telephones and low power radio applications. It features an exceptionally stable RSSI (Received Signal Strength Indicator) output using a unique system of detection. Supply current is less than 2mA from a supply voltage in the range 2.5V to 7.5V.

FEATURES

- Low Power Consumption (1.5mA)
- Single Chip Solution
- Guaranteed 100MHz Operation
- Exceptionally Stable RSSI

APPLICATIONS

- Cellular Radio Telephones
- Cordless Telephones

QUICK REFERENCE DATA

- Supply Voltage 2.5V to 7.5V
- Sensitivity 3μV
- Co-Channel Rejection 7dB

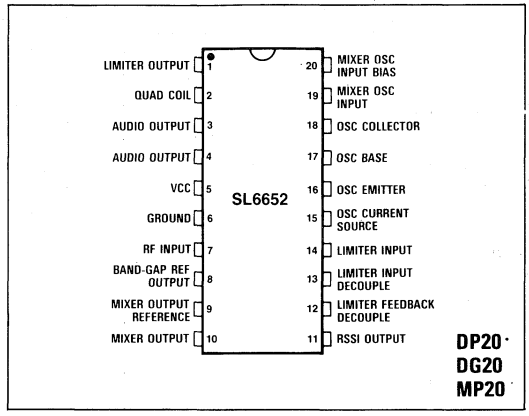


Fig.1 Pin connections (top view)

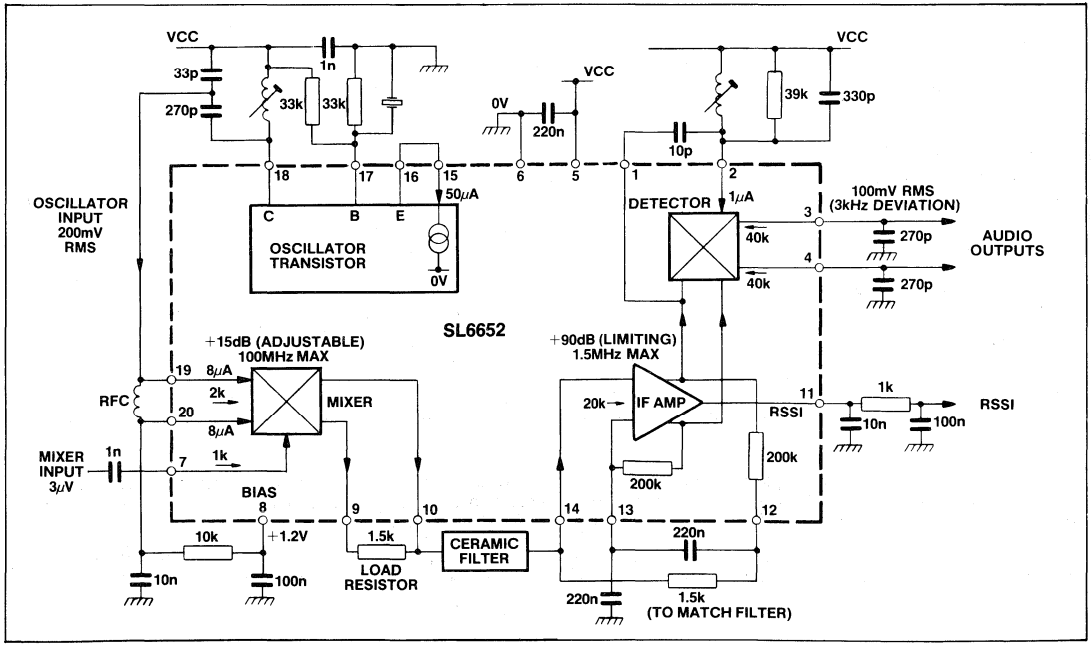


Fig.2 Block diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Storage temperature	-55° C to +150° C
Operating temperature	-55° C to +125° C
Mixer input	1V rms

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = 2.5V to 7.5V, T_{amb} = -30° C to +85° C, IF = 455kHz, RF = 50MHz, Quad Coil Working Q = 30

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Overall					
Supply current		1.5	2.0	mA	
Sensitivity		5	10	μV	20dB SINAD
		3		μV	12dB SINAD
AM rejection		40		dB	RF input <500μV
V_{bias}	1.0	1.2	1.4	V	T_{amb} = 25° C
Co-channel rejection		7		dB	See Note 2
Mixer					
RF input impedance		1		kohm	
OSC input impedance		2		kohm	
OSC input bias		5		μA	At V_{bias}
Mixer gain		15		dB	Rload = 1.5k
3rd order input intercept		-10		dBm	
OSC input level	180		300	mV	
OSC frequency	100			MHz	
Oscillator					
Current sink	40		70	μA	T_{amb} = 25° C
H_{fe}	30				40 ... 70μA
f_T		500		MHz	40 ... 70μA
IF Amplifier					
Gain		90		dB	
Frequency	455	1500		kHz	
Diff. input impedance		20		kohm	
Detector					
Audio output level	75		125	mV	5mV into pin 14
Ultimate S/N ratio		60		dB	5mV into pin 14
THD		0.5	5	%	5mV into pin 14
Output impedance		40		kohm	
Inter-output isolation		65		dB	1kHz
RSSI Output(T_{amb} = +25° C)					
Output current			20	μA	No input pin 14
Output current	50		80	μA	Pin 14 = 2.5mV
Current change	0.9	1.22	1.5	μA/dB	See Note 1
Linear dynamic range	70			dB	See Note 1

NOTES

1. The RSSI output is 100% dynamically tested at 5V and +20° C over a 70dB range. First the input to pin 14 is set to 2.5mV and the RSSI current recorded. Then for each step of 10dB from -40 to +30dB the current is measured again. The current change in each step must meet the specified figure for current change. The RSSI output is guaranteed monotonic and free from discontinuities over this range.

2. Co-channel rejection is measured by applying a 3kHz deviation, 1kHz modulated signal at an input level to give a 20dB SINAD ratio. Then a 3kHz deviation, 400Hz modulated signal on the same frequency is also applied and its level increased to degrade the SINAD to 14dB.

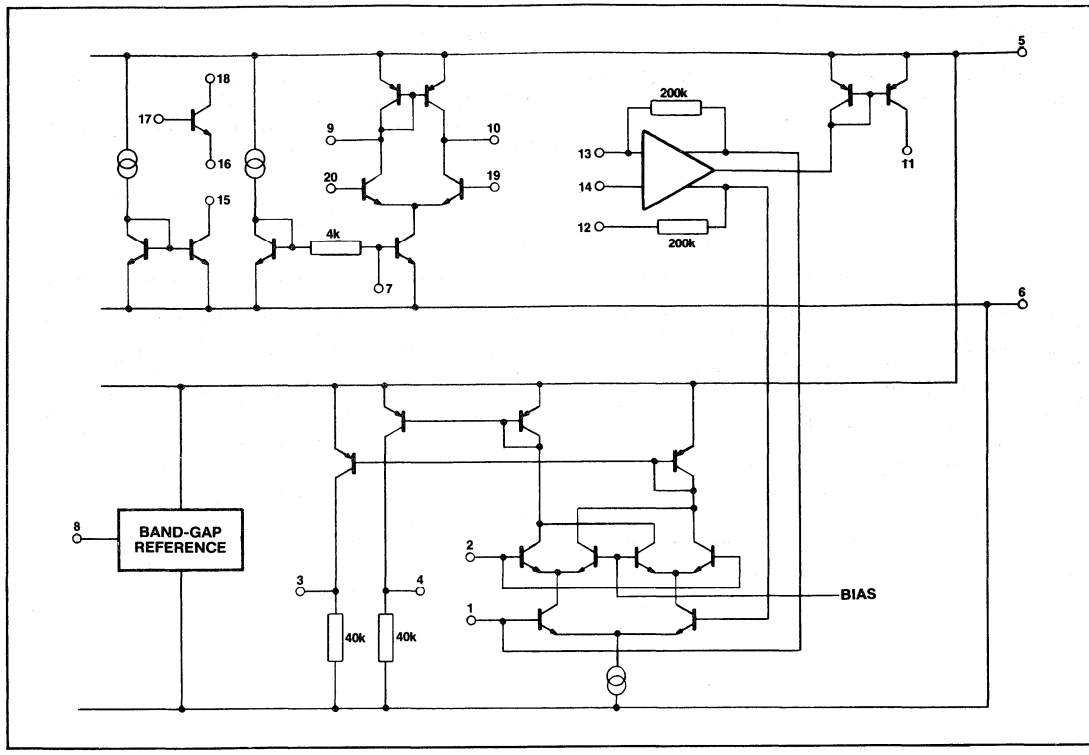


Fig.3 Internal schematic

GENERAL DESCRIPTION

The SL6652 is a very low power, high performance integrated circuit intended for IF amplification and demodulation in FM radio receivers. It comprises:

- A mixer stage for use up to 100MHz
- An uncommitted transistor for use as an oscillator
- A current sink for biasing this transistor
- A limiting amplifier operating up to 1.5MHz
- A quadrature detector with differential AF output
- An RSSI (Received Signal Strength Indicator) output

Mixer

The mixer is single balanced with an active load. Gain is set externally by the load resistor although the value is normally determined by that required for matching into the ceramic filter. It is possible to use a tuned circuit but an increase in mixer gain will result in a corresponding reduction of the mixer input intercept point.

The RF input is a diode-biased transistor with a bias current of typically 300μA. The oscillator input is differential but would normally be driven single-ended. Special care should be taken to avoid accidental overload of the oscillator input.

Oscillator

The oscillator consists of an uncommitted transistor and a separate current sink. The user should ensure that the design of oscillator is suitable for the type of crystal and frequency required; it may not always be adequate to duplicate the design shown in this data sheet.

IF amplifier

The limiting amplifier is capable of operation to at least 1MHz and the input impedance is set by an external resistor to match the ceramic filter. Because of the high gain, pins 12 and 13 must be adequately bypassed.

Detector

A conventional quadrature detector is fed internally from the IF amplifier; the quadrature input is fed externally using an appropriate capacitor and phase shift network. A differential output is provided to feed a comparator for digital use, although it can also be used to provide AFC.

RSSI output

The RSSI output is a current source with value proportional to the logarithm of the IF input signal amplitude. There is a small residual current due to noise within the amplifier (and mixer) but beyond this point there is a measured and guaranteed 70dB dynamic range. The typical range extends to 92dB, independent of frequency, and with exceptionally good temperature and supply voltage stability.

Supply voltage

The SL6652 will operate reliably from 2.5V to 7.5V The supply line must be decoupled with 470nF using short leads.

Internal bias voltage

The internal band gap reference must be externally decoupled. It can be used as an external reference but must not be loaded heavily; the output impedance is typically 14 ohms.

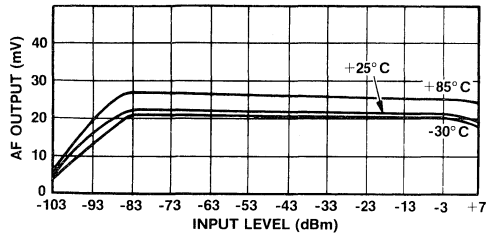


Fig.4 Audio output vs input and temperature at 2.5V

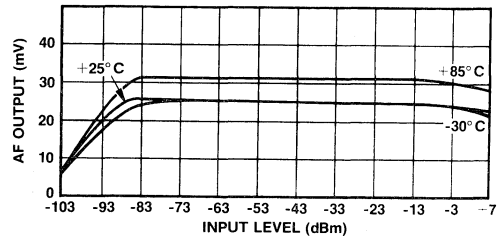


Fig.5 Audio output vs input and temperature at 5.0V

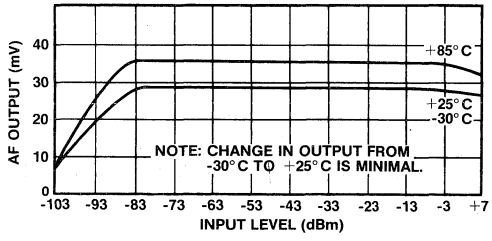


Fig.6 Audio output vs input and temperature at +7.5V

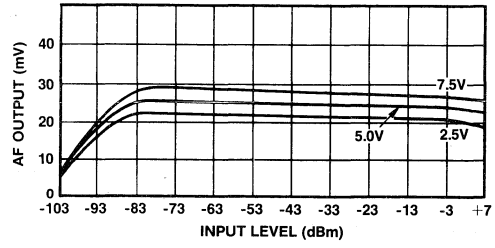


Fig.7 Audio output vs input and supply voltage at +25°C

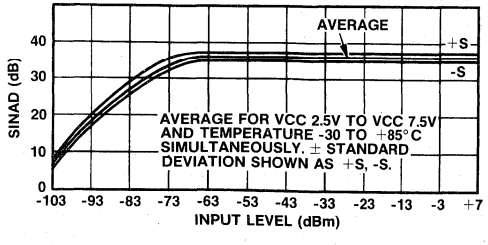


Fig.8 SINAD and input level

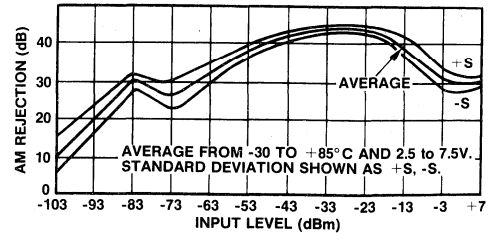


Fig.9 AM rejection and input level

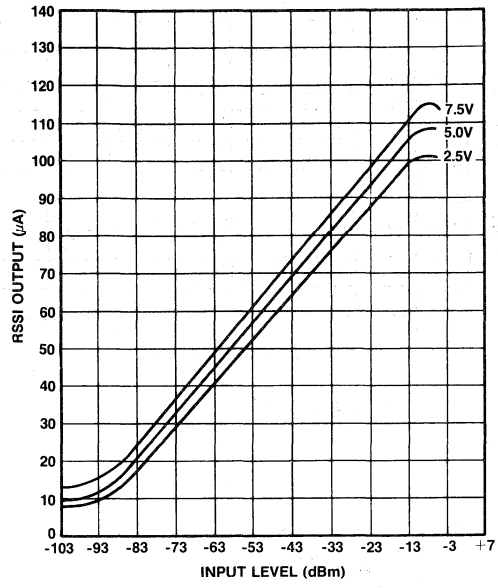


Fig.10 RSSI output vs input and supply voltage (T_{amb} = 20° C)

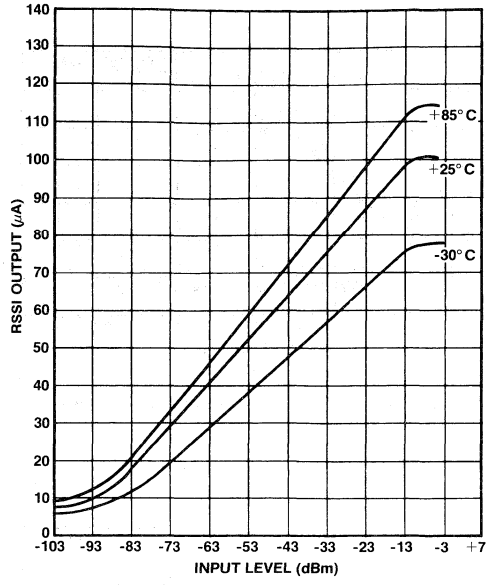


Fig.11 RSSI output vs input level and temperature (V_{CC} = 2.5V)

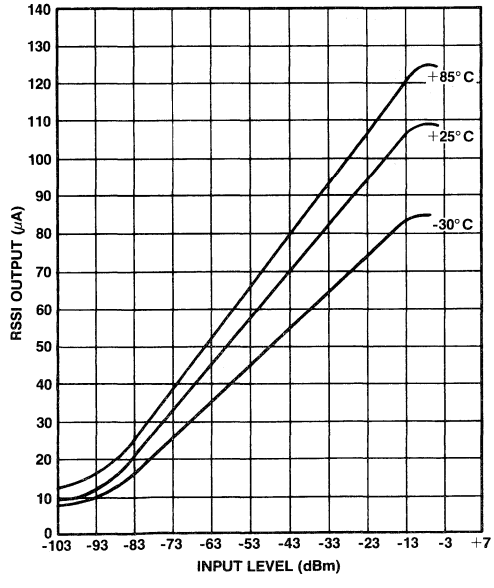


Fig.12 RSSI output vs input level and temperature (V_{CC} = 5V)

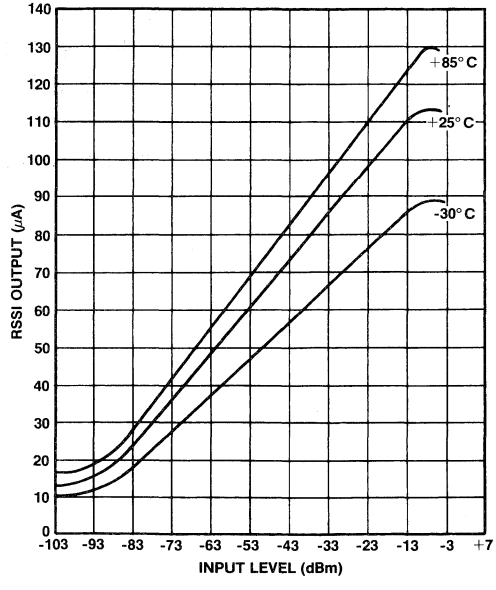


Fig.13 RSSI output vs input level and temperature (V_{CC} = 7.5V)

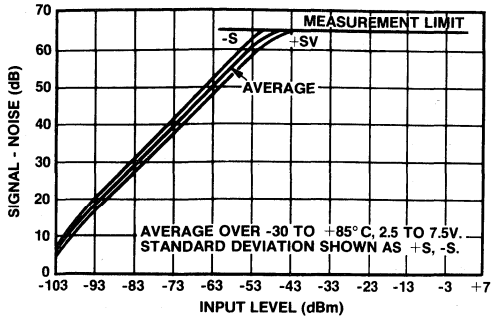


Fig.14 Signal + noise to noise ratio vs input level

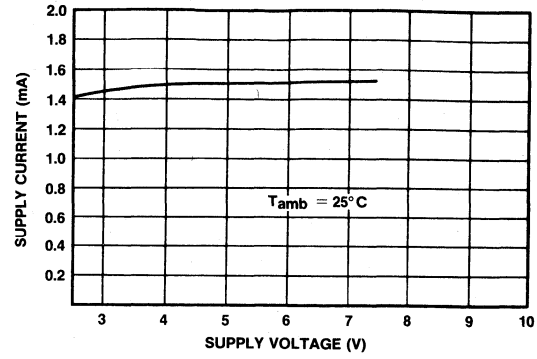


Fig.15 Supply current vs supply voltage

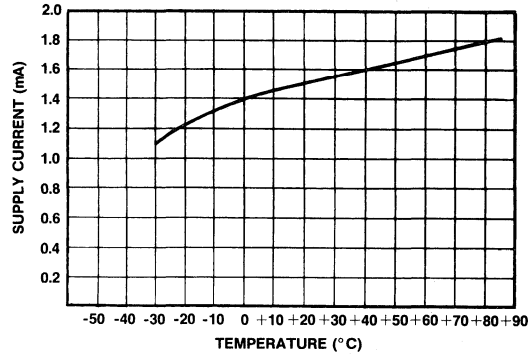


Fig.16 Supply current vs temperature (V_{CC} = 5V)

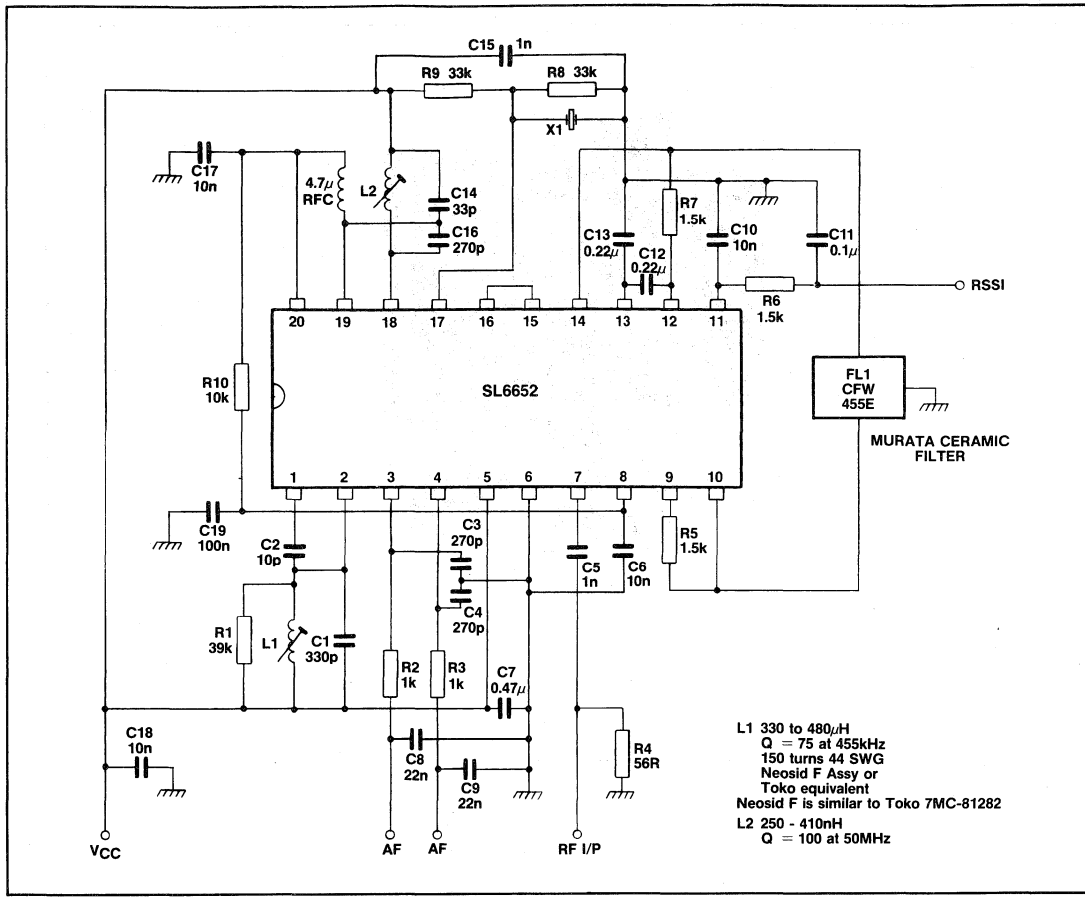


Fig.17 Circuit diagram of SL6652 demonstration board

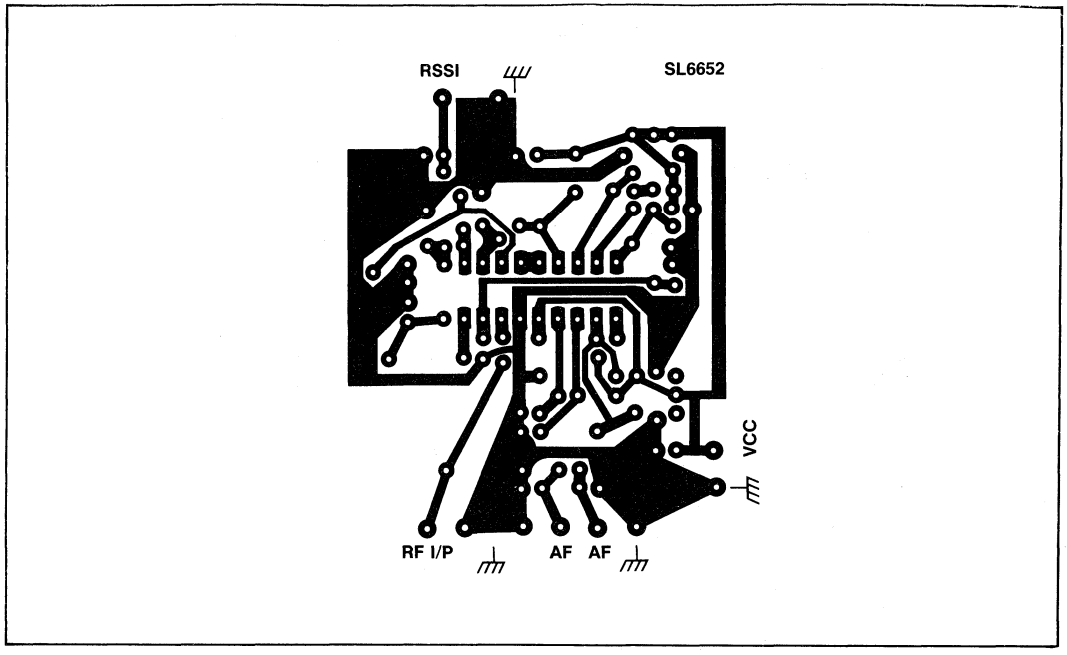


Fig.18 PCB mask of demonstration board (1:1)

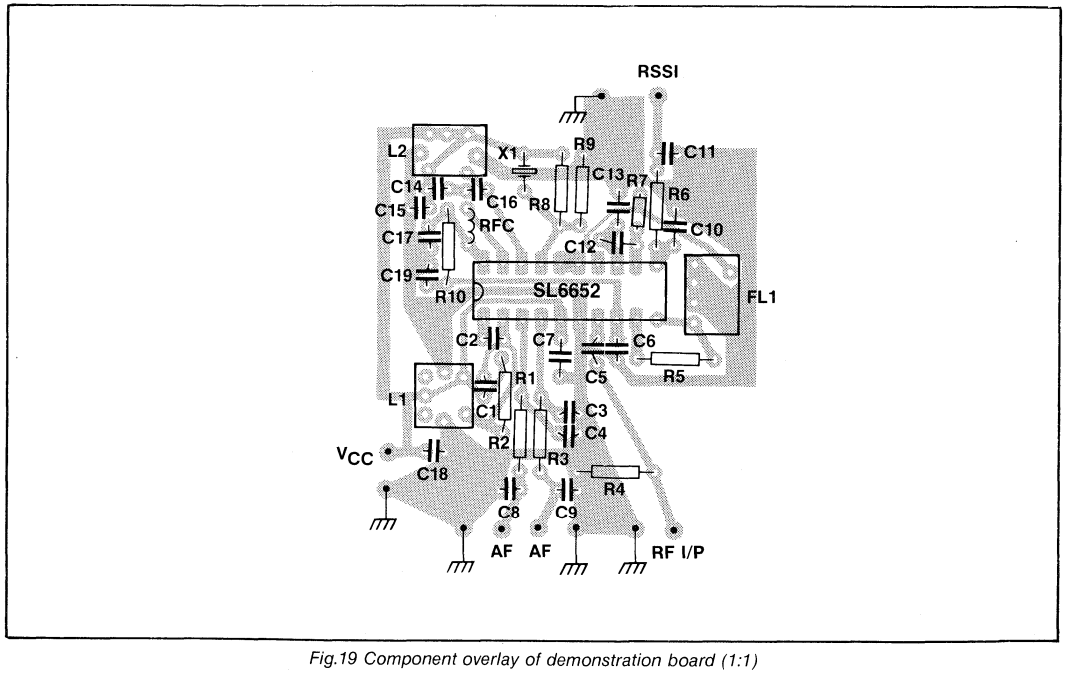


Fig.19 Component overlay of demonstration board (1:1)

PLESSEY
Semiconductors

SL6653

LOW POWER IF/AF CIRCUIT FOR FM RECEIVERS

The SL6653 is a complete single chip mixer/oscillator, IF amplifier and detector for FM cellular radio, cordless telephones and low power radio applications. Supply current is less than 2mA from a supply voltage in the range 2.5V to 7.5V

The SL6653 affords maximum flexibility in design and use. It is supplied in a dual-in-line plastic package.

FEATURES

- Low Power Consumption (1.5mA)
- Single Chip Solution
- Guaranteed 100MHz Operation

APPLICATIONS

- Mobile Radio Telephones
- Cordless Telephones

QUICK REFERENCE DATA

- Supply voltage 2.5V to 7.5V
- Sensitivity 3μV

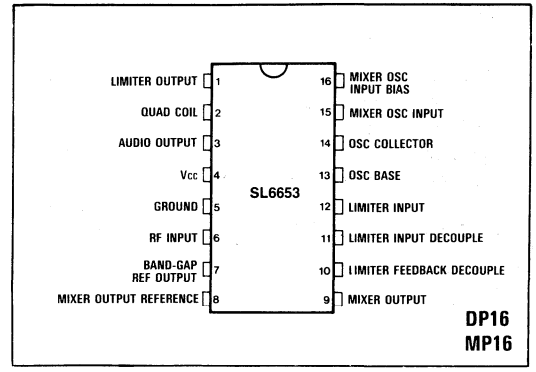


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Storage temperature	-55° C to +150° C
Operating temperature	-55° C to +125° C
Mixer input	1V rms

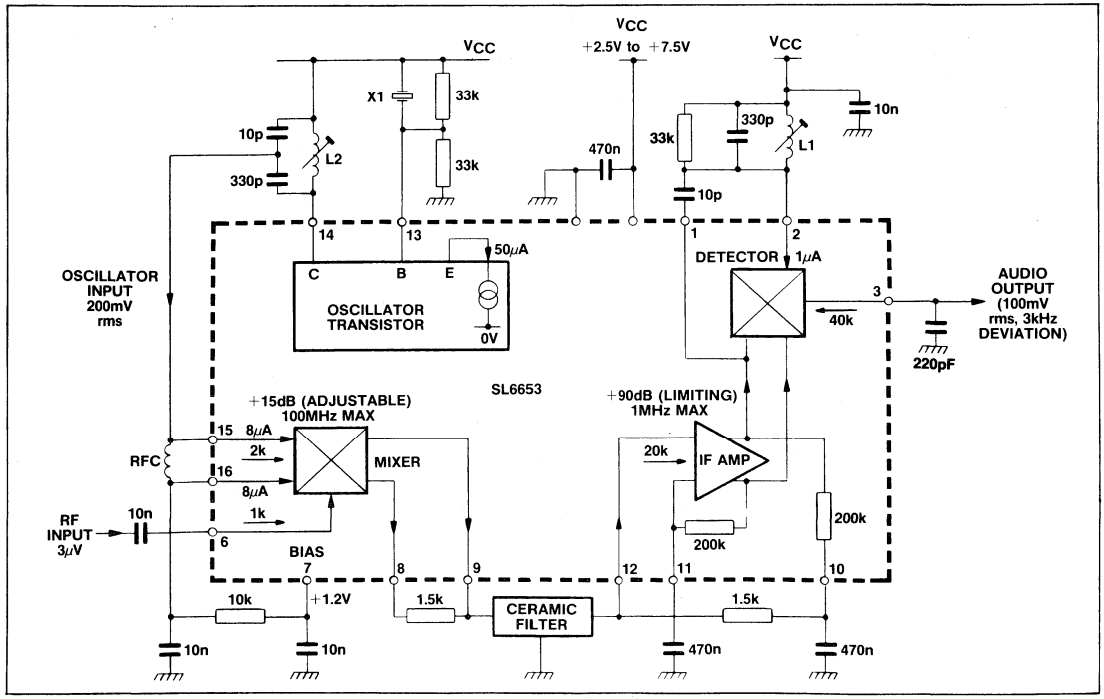


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = 2.5V to 7.5V, T_{amb} = -30° C to +85° C, Mod.Freq. = 1kHz, Deviation = 2.5kHz, Quadrature Circuit Working Q = 30

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Overall					
Supply current		1.5	2.0	mA	
Sensitivity		5	10	μV	20dB SINAD
		3		μV	12dB SINAD
AM rejection		30		dB	RF input < 500μV
V_{bias}	1.0	1.2	1.4	V	T_{amb} = 25° C
Mixer					
RF input impedance		1		kohm	
OSC input impedance		2		kohm	
OSC input bias		5		μA	At V_{bias}
Mixer gain		15		dB	Rload = 1.5k
3rd order input intercept		-10		dBm	
OSC input level	180		300	mV	
OSC frequency	100			MHz	
Oscillator					
Current sink	40		70	μA	T_{amb} = 25° C
H_{fe}	30				40 ... 70μA
f_T		500		MHz	40 ... 70μA
IF Amplifier					
Gain		90		dB	
Frequency	455	1500		kHz	
Diff. input impedance		20		kohm	
Detector					
Audio output level	75		125	mV	
Ultimate S/N ratio		60		dB	10mV into pin 12
THD		0.5	5	%	
Output impedance		40		kohm	

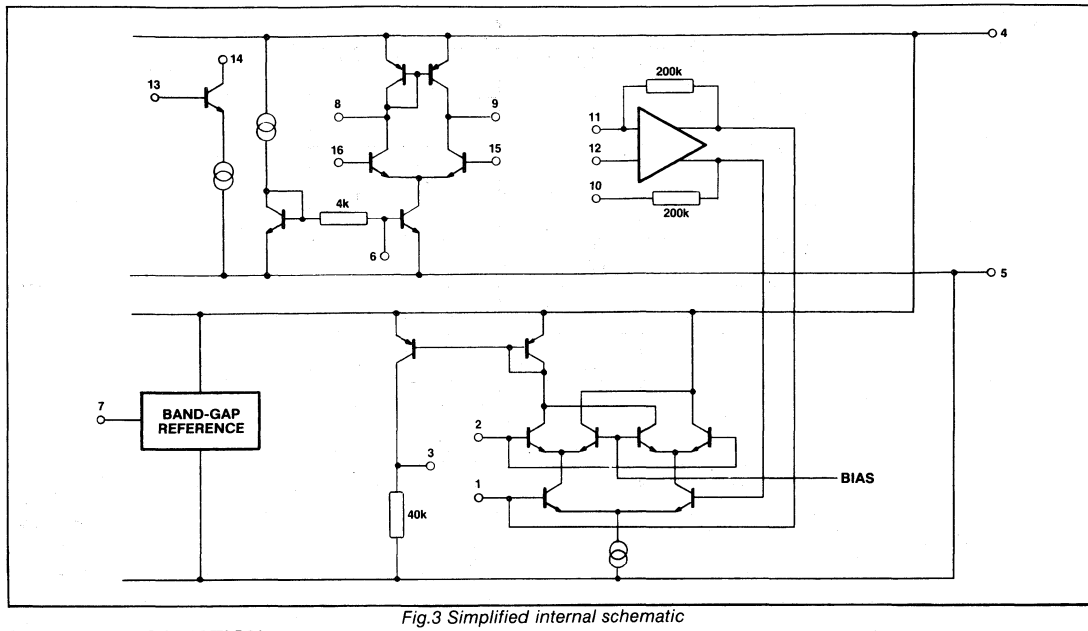


Fig.3 Simplified internal schematic

GENERAL DESCRIPTION

The SL6653 is a very low power, high performance integrated circuit intended for IF amplification and demodulation in FM radio receivers. It comprises:

- A mixer stage for use up to 100MHz
- A transistor for use as an oscillator
- A limiting amplifier operating up to 1.5MHz
- A quadrature detector with AF output

Mixer

The mixer is single balanced with an active load. Gain is set externally by the load resistor although the value is normally determined by that required for matching into the ceramic filter. It is possible to use a tuned circuit but an increase in mixer gain will result in a corresponding reduction of the mixer input intercept point.

The RF input is a diode-biased transistor with a bias current of typically 300μA. The oscillator input is differential but would normally be driven single-ended. Special care should be taken to avoid accidental overload of the oscillator input.

Oscillator

The oscillator consists of a transistor and a current sink. The user should ensure that the design of oscillator is suitable for the type of crystal and frequency required; it may not always be adequate to duplicate the design shown in this data sheet.

IF amplifier

The limiting amplifier is capable of operation to at least 1MHz and the input impedance is set by an external resistor to match the ceramic filter.

Detector

A conventional quadrature detector is fed internally from the IF amplifier; the quadrature input is fed externally using an appropriate capacitor and phase shift network.

Supply voltage

The SL6653 will operate reliably from 2.5V to 7.5V. The supply line must be decoupled with 470nF using short leads.

Internal bias voltage

The internal band gap reference must be externally decoupled. It can be used as an external reference but must not be loaded heavily; the output impedance is typically 14 ohms.

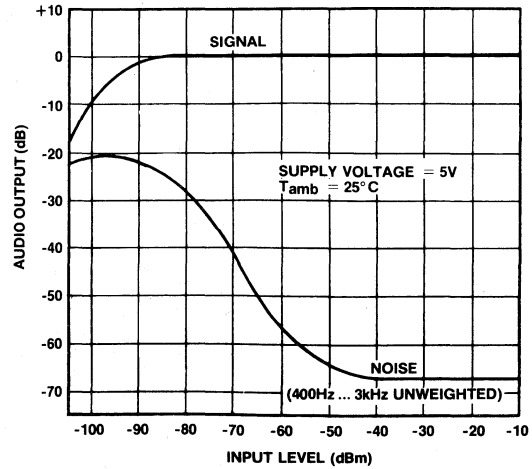


Fig.4 Audio and noise outputs vs input level

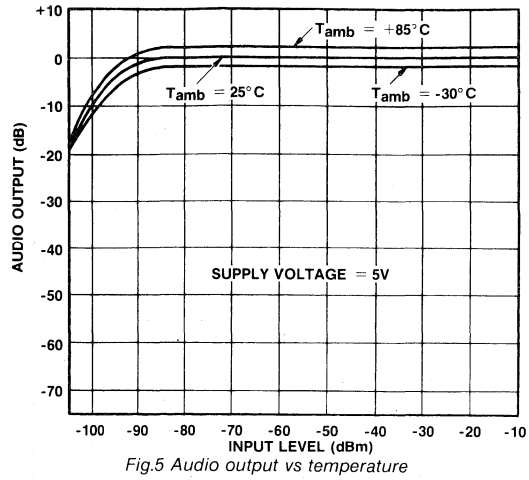


Fig.5 Audio output vs temperature

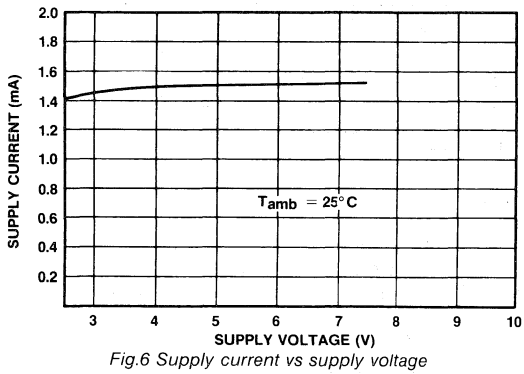


Fig.6 Supply current vs supply voltage

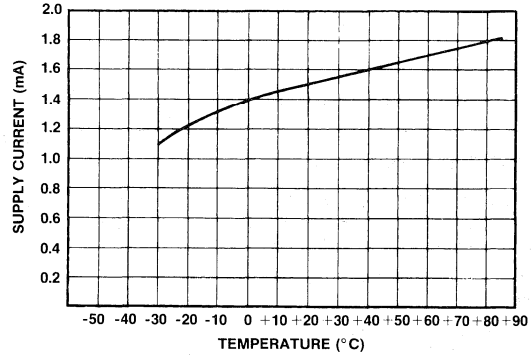


Fig.7 Supply current vs temperature

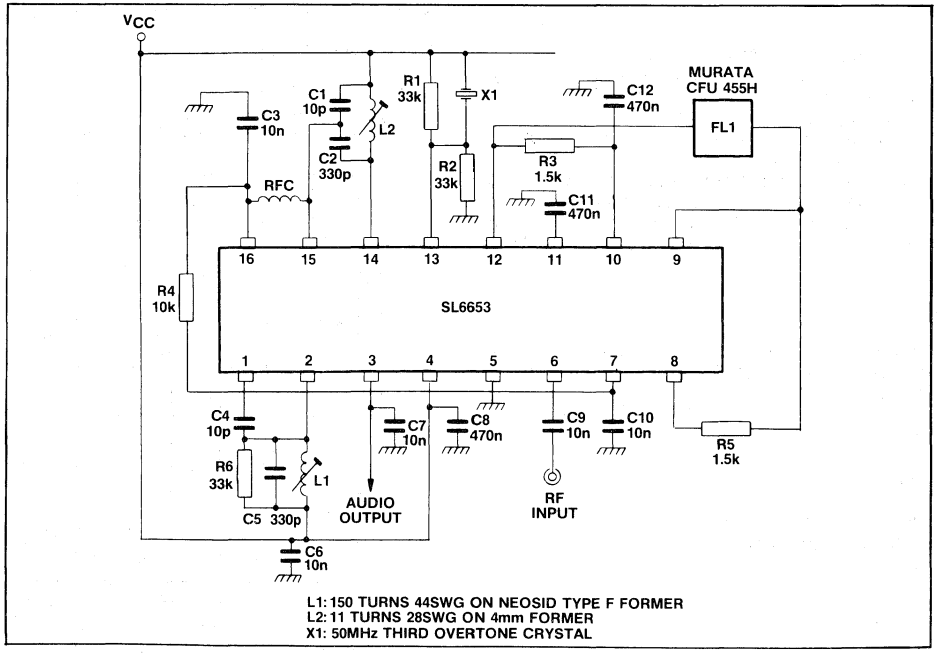


Fig.8 Circuit diagram of SL6653 demonstration board

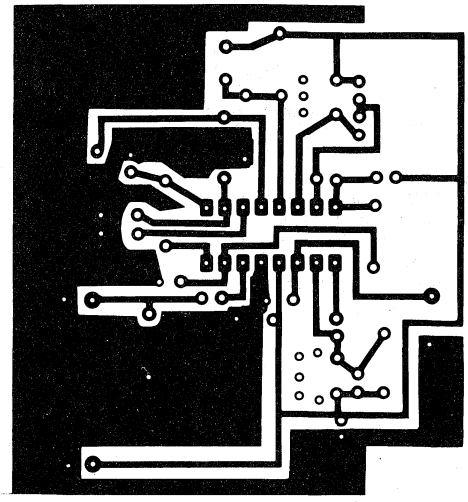


Fig.9 PCB mask of demonstration board (1:1)

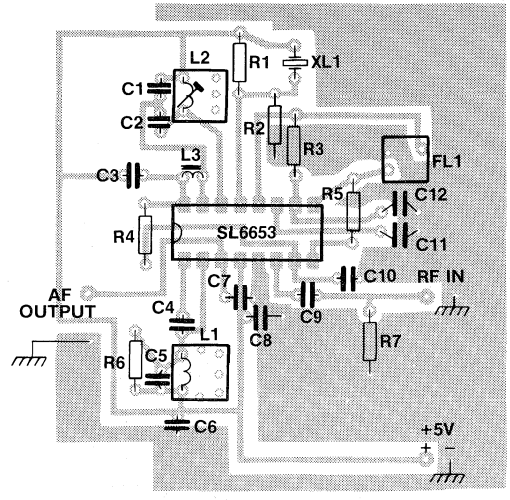


Fig.10 Component overlay of demonstration board (1:1)

PLESSEY
Semiconductors

SL6654

LOWER POWER IF (AF CIRCUIT (WITH RSSI) FOR FM CELLULAR RADIO

The SL6654 is a complete single chip mixer/oscillator, IF amplifier and detector for FM cellular radio, cordless telephones and low power radio applications. It features an exceptionally stable RSSI (Received Signal Strength Indicator) output using a unique system of detection. Supply current is less than 2mA from a supply voltage in the range 2.5V to 7.5V.

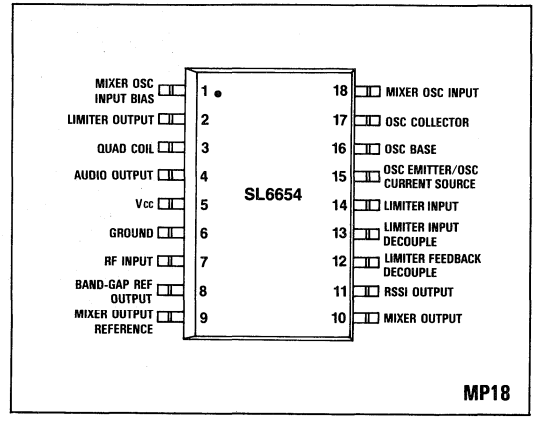


Fig.1 Pin connections (top view)

FEATURES

- Low Power Consumption (1.5mA)
- Single Chip Solution
- Guaranteed 100MHz Operation
- Exceptionally Stable RSSI

APPLICATIONS

- Cellular Radio Telephones
- Cordless Telephones

QUICK REFERENCE DATA

- Supply Voltage 2.5V to 7.5V
- Sensitivity 3μV
- Co-Channel Rejection 7dB

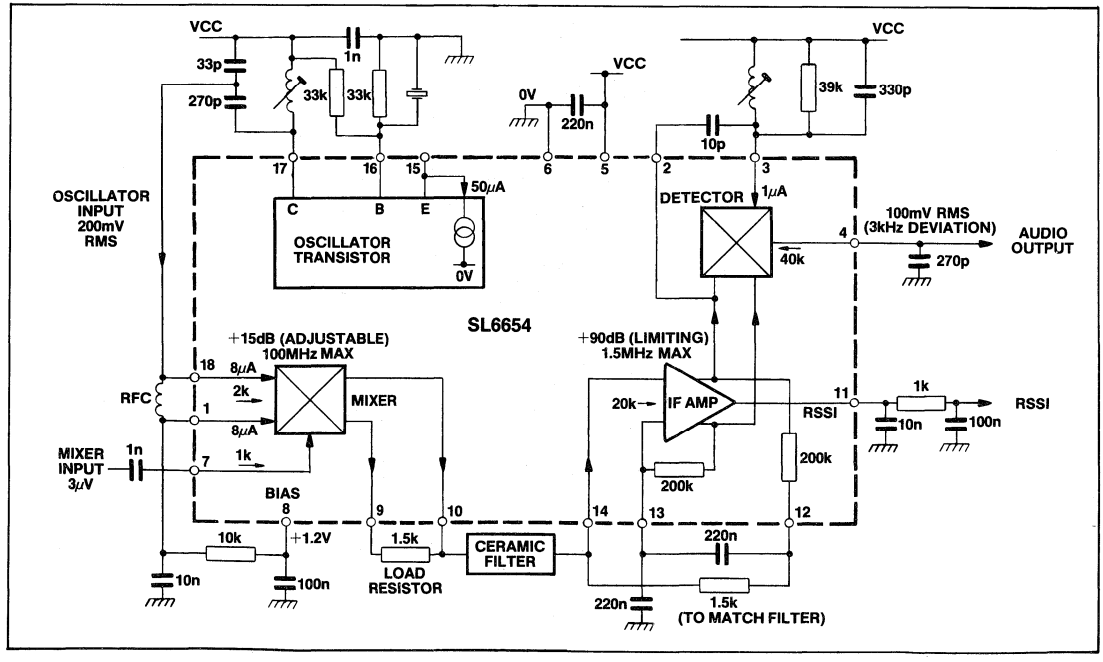


Fig.2 Block diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Storage temperature	-55° C to +150° C
Operating temperature	-55° C to +125° C
Mixer input	1V rms

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = 2.5V to 7.5V, T_{amb} = -30° C to +85° C, IF = 455kHz, RF = 50MHz, Quad Coil Working Q = 30

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Overall					
Supply current		1.5	2.0	mA	
Sensitivity		5	10	μV	20dB SINAD
		3		μV	12dB SINAD
AM rejection		40		dB	RF input <500μV
V_{bias}	1.0	1.2	1.4	V	T_{amb} = 25° C
Co-channel rejection		7		dB	See Note 2
Mixer					
RF input impedance		1		kohm	
OSC input impedance		2		kohm	
OSC input bias		5		μA	At V_{bias}
Mixer gain		15		dB	Rload = 1.5k
3rd order input intercept		-10		dBm	
OSC input level	180		300	mV	
OSC frequency	100			MHz	
Oscillator					
Current sink	40		70	μA	T_{amb} = 25° C
H_{fe}	30				40 ... 70μA
f_T		500		MHz	40 ... 70μA
IF Amplifier					
Gain		90		dB	
Frequency	455	1500		kHz	
Diff. input impedance		20		kohm	
Detector					
Audio output level	75		125	mV	5mV into pin 14
Ultimate S/N ratio		60		dB	
THD		0.5	5	%	
Output impedance		40		kohm	
RSSI Output(T_{amb} = +25° C)					
Output current			25	μA	No input pin 14
Output current	50		80	μA	Pin 14 = 2.5mV
Current change	0.9	1.22	1.5	μA/dB	See Note 1
Linear dynamic range	70			dB	See Note 1

NOTES

1. The RSSI output is 100% dynamically tested at 5V and +20° C over a 70dB range. First the input to pin 14 is set to 2.5mV and the RSSI current recorded. Then for each step of 10dB from -40 to +30dB the current is measured again. The current change in each step must meet the specified figure for current change. The RSSI output is guaranteed monotonic and free from discontinuities over this range.

2. Co-channel rejection is measured by applying a 3kHz deviation, 1kHz modulated signal at an input level to give a 20dB SINAD ratio. Then a 3kHz deviation, 400Hz modulated signal on the same frequency is also applied and its level increased to degrade the SINAD to 14dB.

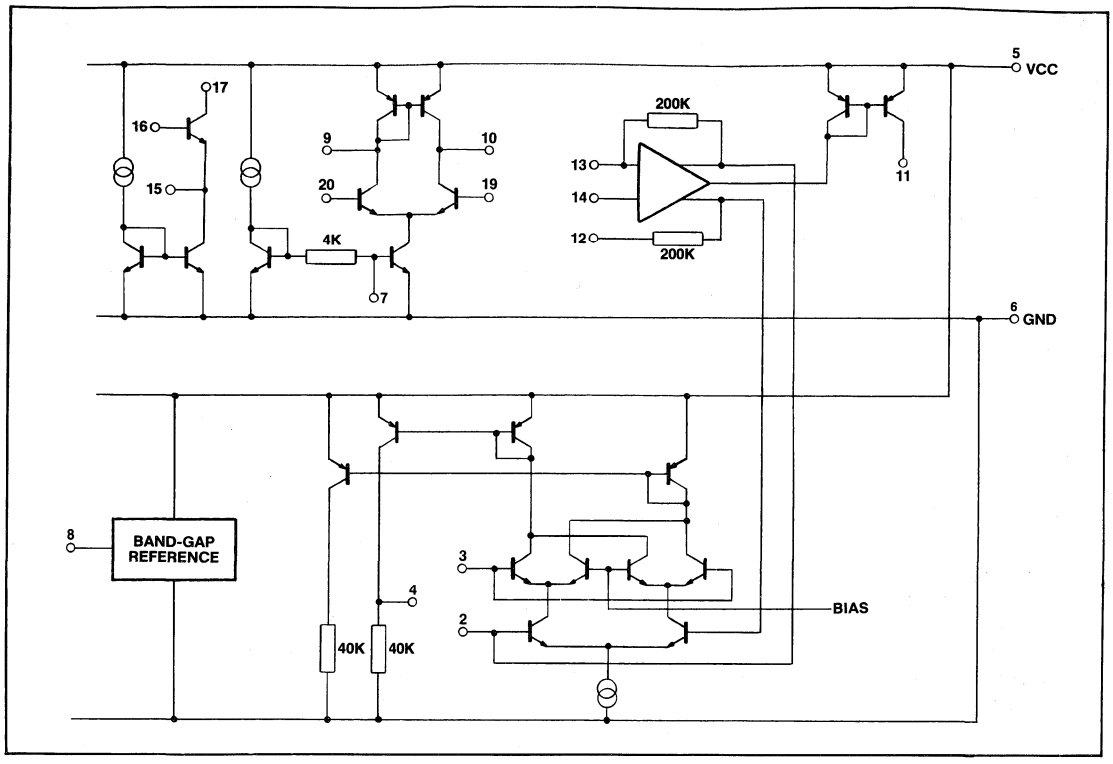


Fig.3 Internal schematic

GENERAL DESCRIPTION

The SL6654 is a very low power, high performance integrated circuit intended for IF amplification and demodulation in FM radio receivers. It comprises:

- A mixer stage for use up to 100MHz
- An uncommitted transistor for use as an oscillator
- A current sink for biasing this transistor
- A limiting amplifier operating up to 1.5MHz
- A quadrature detector with AF output
- An RSSI (Received Signal Strength Indicator) output

Mixer

The mixer is single balanced with an active load. Gain is set externally by the load resistor although the value is normally determined by that required for matching into the ceramic filter. It is possible to use a tuned circuit but an increase in mixer gain will result in a corresponding reduction of the mixer input intercept point.

The RF input is a diode-biased transistor with a bias current of typically 300μA. The oscillator input is differential but would normally be driven single-ended. Special care should be taken to avoid accidental overload of the oscillator input.

Oscillator

The oscillator consists of an uncommitted transistor with a current sink. The user should ensure that the design of oscillator is suitable for the type of crystal and frequency required; it may not always be adequate to duplicate the design shown in this data sheet.

IF amplifier

The limiting amplifier is capable of operation to at least 1MHz and the input impedance is set by an external resistor to match the ceramic filter. Because of the high gain, pins 12 and 13 must be adequately bypassed.

Detector

A conventional quadrature detector providing audio output is fed internally from the IF amplifier; the quadrature input is fed externally using an appropriate capacitor and phase shift network.

RSSI output

The RSSI output is a current source with value proportional to the logarithm of the IF input signal amplitude. There is a small residual current due to noise within the amplifier (and mixer) but beyond this point there is a measured and guaranteed 70dB dynamic range. The typical range extends to 92dB, independent of frequency, and with exceptionally good temperature and supply voltage stability.

Supply voltage

The SL6654 will operate reliably from 2.5V to 7.5V. The supply line must be decoupled with 470nF using short leads.

Internal bias voltage

The internal band gap reference must be externally decoupled. It can be used as an external reference but must not be loaded heavily; the output impedance is typically 14 ohms.

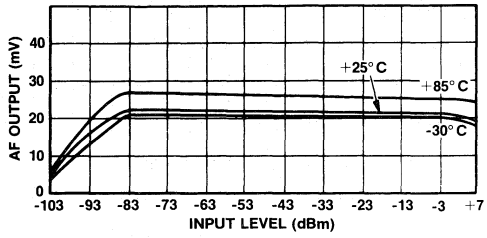


Fig.4 Audio output vs input and temperature at 2.5V

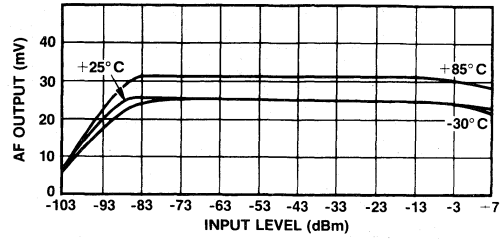


Fig.5 Audio output vs input and temperature at 5.0V

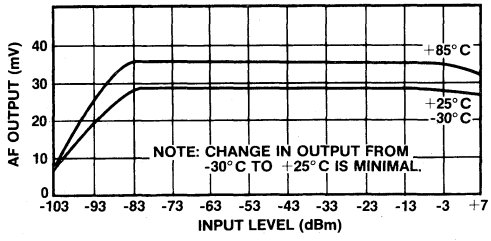


Fig.6 Audio output vs input and temperature at +7.5V

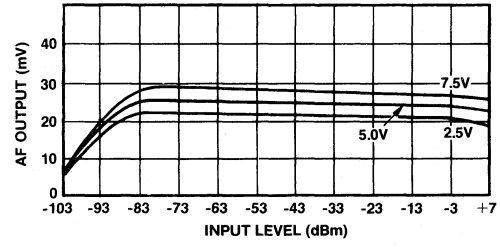


Fig.7 Audio output vs input and supply voltage at +25°C

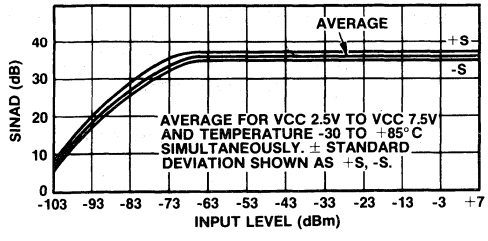


Fig.8 SINAD and input level

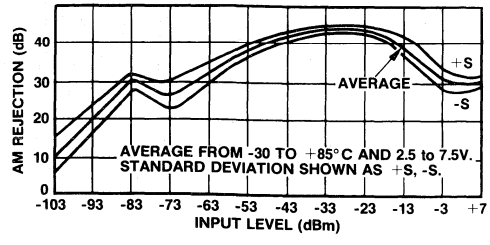


Fig.9 AM rejection and input level

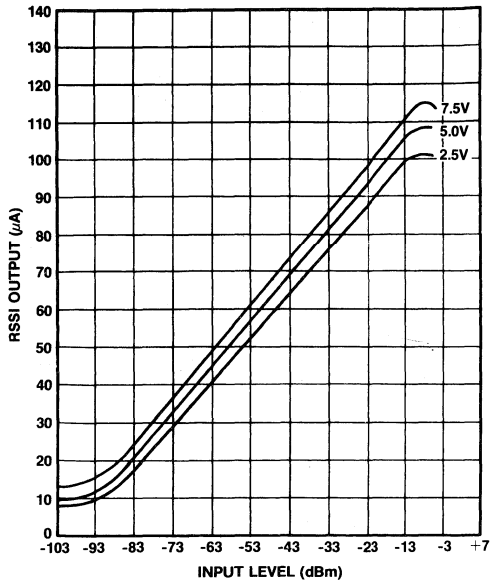


Fig.10 RSSI output vs input and supply voltage (T_{amb} = 20° C)

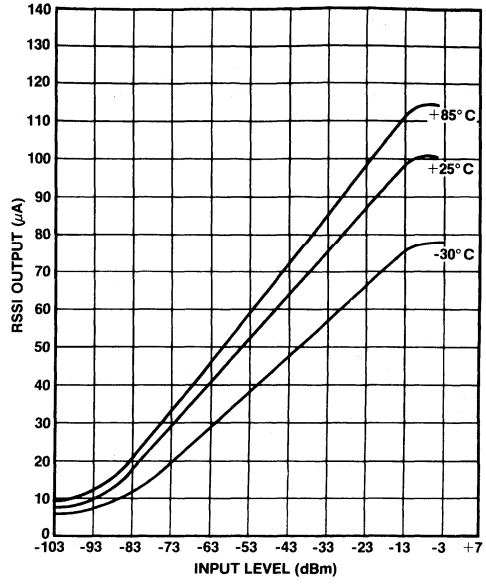


Fig.11 RSSI output vs input level and temperature (V_{CC} = 2.5V)

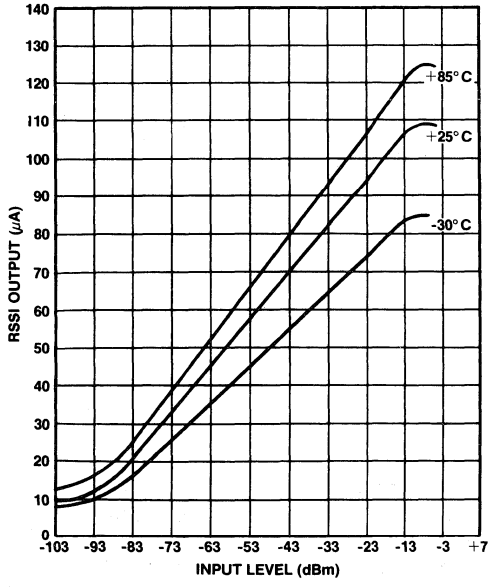


Fig.12 RSSI output vs input level and temperature (V_{CC} = 5V)

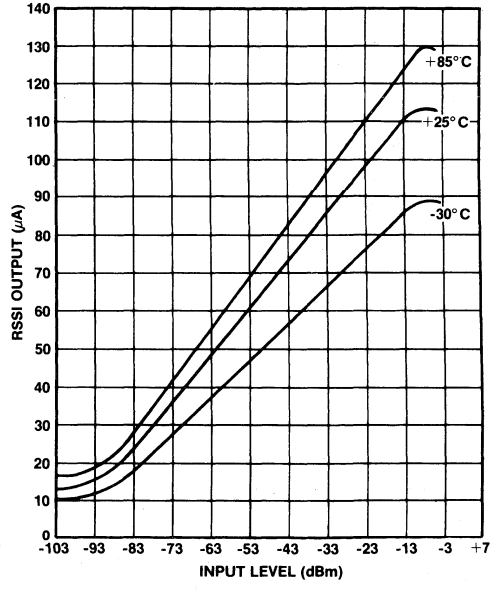


Fig.13 RSSI output vs input level and temperature (V_{CC} = 7.5V)

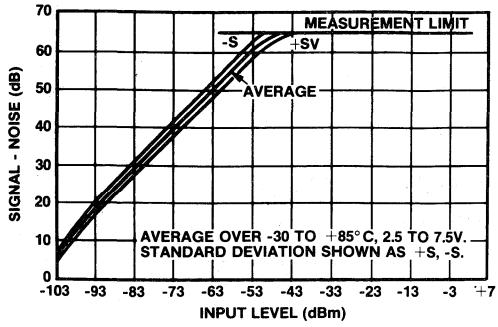


Fig.14 Signal + noise to noise ratio vs input level

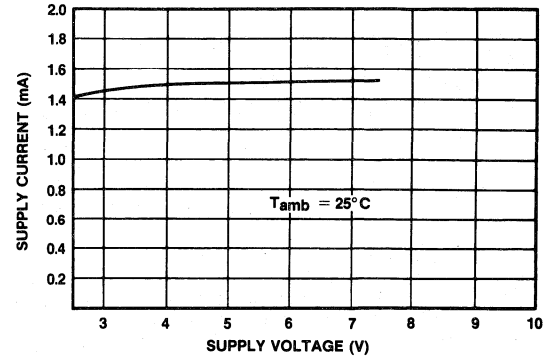


Fig.15 Supply current vs supply voltage

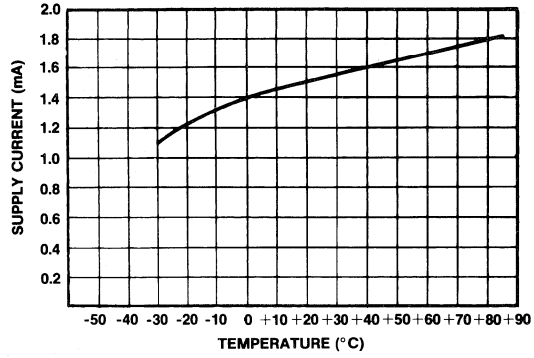


Fig.16 Supply current vs temperature (V_{CC} = 5V)

PLESSEY
Semiconductors

SL6655

ULTRA LOW POWER FM RADIO RECEIVER

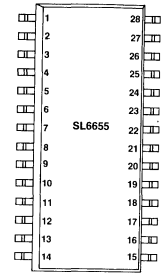
The SL6655 is a single conversion receiver complete with RF amplifier/mixer/oscillator/IF amplifier and detector. It features very low power consumption and operation from 0.95V to 5V supply. The device can be powered-down to currents os 1μA and offers sensitivities of typically 250nV.

FEATURES

- Very Low Voltage Operation (0.95V)
- Very Low Current Consumption:
  - 1mA Powered-up (typ.)
  - 1μA Powered-down (typ.)
- Wide Supply Range: 0.95V to 5V
- 250nV Sensitivity (12dB Sinad)
- Guaranteed 100MHz Operation
- Miniature Plastic Surface Mount Package

APPLICATIONS

- Low Power Radio Receivers
- Radio Paging
- Cordless Telephones



MP28

Pin	Function	Pin	Function
1	N/C	15	RF Vcc +
2	Mixer output	16	LF Vcc +
3	Battery economy	17	Audio output
4	Oscillator current source & emitter	18	Audio output(Differential)
5	Oscillator base	19	Quad coil drive
6	Oscillator collector	20	Quad coil
7	Mixer osc input	21	N/C
8	Mixer osc I/P bias	22	2nd limiter F/B decouple
9	Mixer RF input	23	2nd limiter input
10	RF amp output	24	2nd limiter I/P decouple
11	Regulator output	25	1st limiter output
12	RF amp input	26	1st limiter I/P decouple
13	RF ground	27	1st limiter input
14	LF ground	28	1st limiter F/B decouple

Fig.1 Pin connections - top view

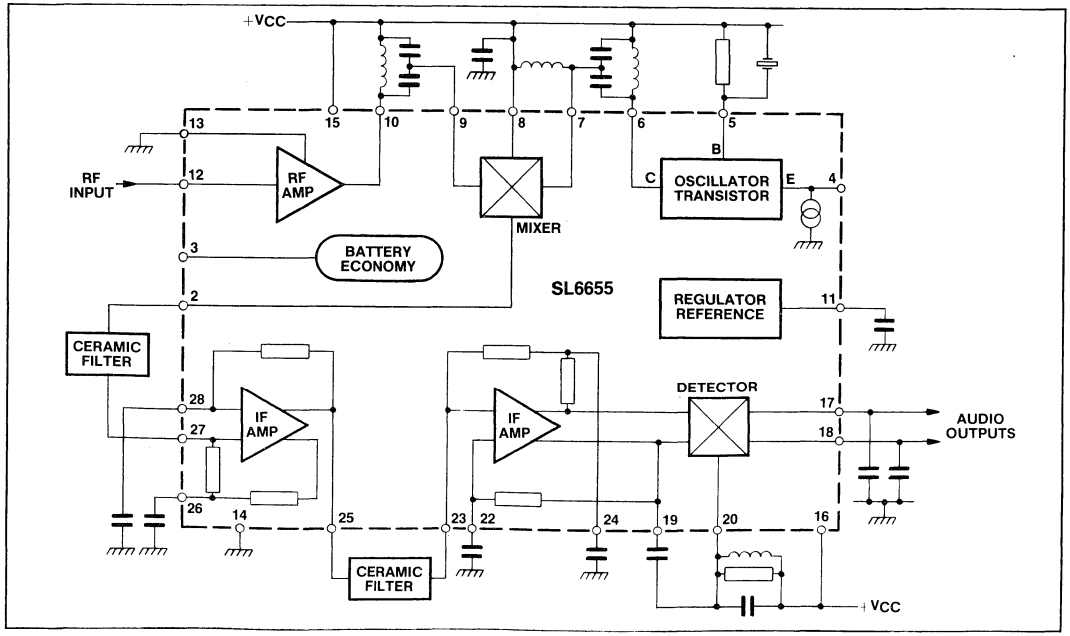


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Input signal = 50MHz, Frequency modulated with 1kHz with ± 3kHz deviation, T_{amb} = 0° C to +50° C, V_{CC} = 1.3V

Characteristic	Pin Number	Value			Units	Conditions
		Min.	Typ.	Max.		
Overall						
Supply voltage		0.95		5.0	V	25° C
Supply voltage		1.05		5.0	V	-30° C to +85° C
Supply current						
Powered up			1.0	1.3	mA	Pin 3 High
Powered down			1.0		μA	Pin 3 Low
Battery economy response			0.5		ms	
Sensitivity			250		nV	12dB Sinad
AM rejection			37		dB	
RF amplifier						
Supply current			50		μA	
Noise figure			6		dB	
H_{FE}			100			
f_T			500		MHz	
Oscillator						
Supply current			50		μA	
H_{FE}			100			
f_T			500		MHz	
IF amplifier cascade						
Sensitivity	27		3		μV	12dB Sinad
Input impedance	27, 23		1.5		kΩ	
Output impedance	25		1.5		kΩ	
Gain			100		dB	
Upper cut-off frequency			1.5		MHz	
Detector						
Audio output level			12		mV(rms)	Open circuit (Quad Coil Q ≃ 30)
Inter-output isolation			65		dB	
Output impedance			50		kΩ	
Mixer						
Conversion gain			6		dB	
Input impedance			4		kΩ	
Output impedance			1.5		kΩ	
Regulator						
Output level		0.9	0.95	1	V	
Output temperature coefficient			1.3		mV/° C	
Output current		6			mA	
Battery economy						
Input current			0.5		μA	
Input logic high		80			% V_{CC}	
Input logic low				20	% V_{CC}	

GENERAL DESCRIPTION

The RF amplifier is a diode biased input with a bias current of typically 50μA. The output is left open circuit so that the gain can be selected externally.

The RF input to the Mixer is diode biased with a bias current of typically 250μA. The oscillator input is differential, but would normally be driven single ended with the remaining input biased at V_{CC}.

The Mixer has a single output with resistance of 1.5kΩ. A single transistor is used for the oscillator which has its base and collector floating, and the emitter connected to a current source of 50μA nominal value.

The IF amplifiers have input impedances of 1.5kΩ and are thus ideally suited for use with 455kHz ceramic filters.

The detector is fed internally from the IF limiting amplifier and the quadrature input is fed externally using a capacitor and appropriate phase shift networks. A differential audio output is provided to feed a comparator for digital use. The regulated output is a supply independent and partially temperature compensated capable of sourcing 6mA.

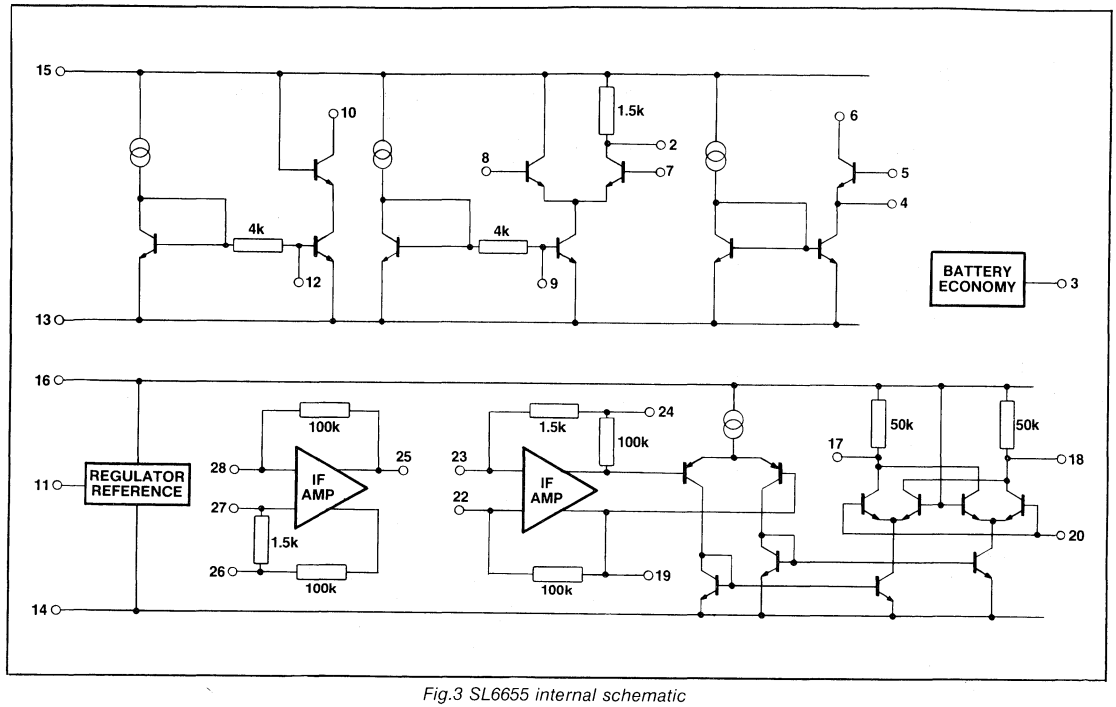


Fig.3 SL6655 internal schematic

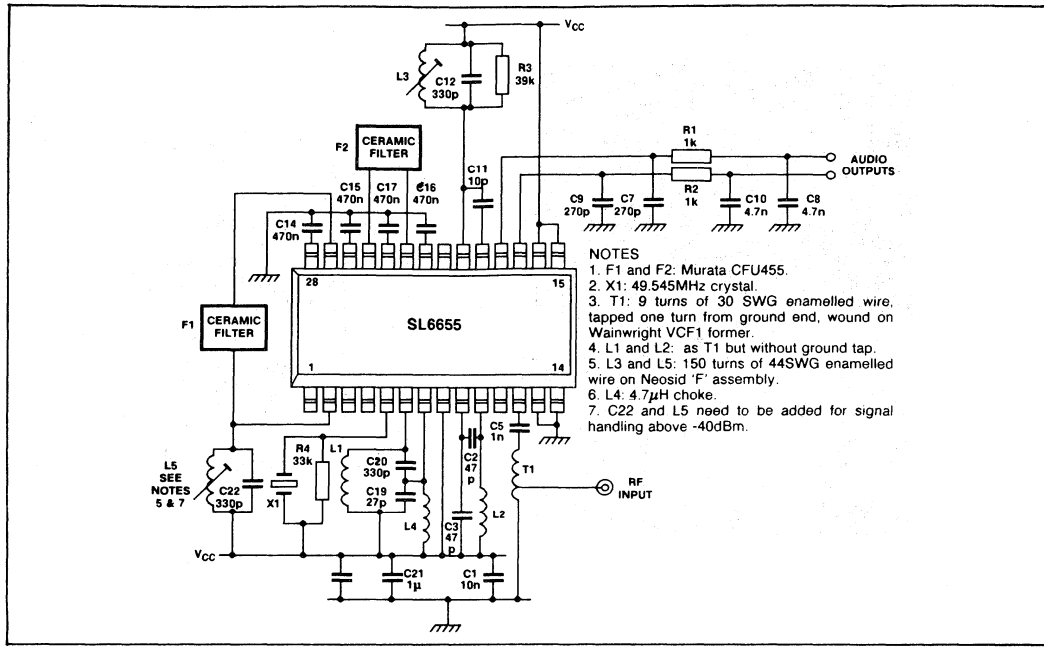


Fig.4 Circuit diagram of SL6655 demonstration board

PERFORMANCE OF SL6655 DEMONSTRATION BOARD

Input signal = 50MHz, Frequency modulated with 1kHz with ± 3kHz deviation, T_{amb} = 0° C to +50° C, V_{CC} = 1.3V

Sensitivity	-119dBm for 12dB sinad at 1.3V -113dBm for 12dB sinad at 0.95V
Adjacent channel rejection	50dB at 1.3V 68dB at 0.95V
Co-channel rejection	10dB at 1.3V 9dB at 0.95V
RF amplifier 2nd order intercept **RF amplifier 3rd order intercept**	0dB -14dBm
Noise figure of RF amplifier	6dB

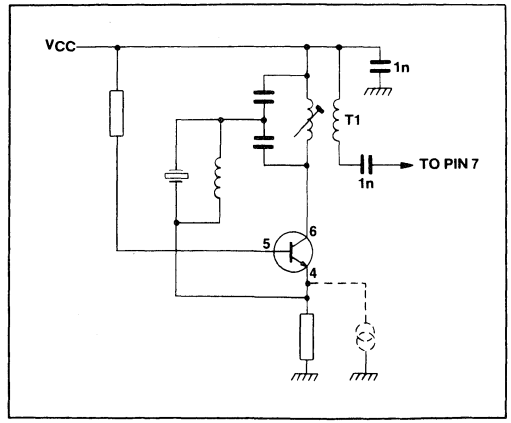


Fig.5 Alternative local oscillator

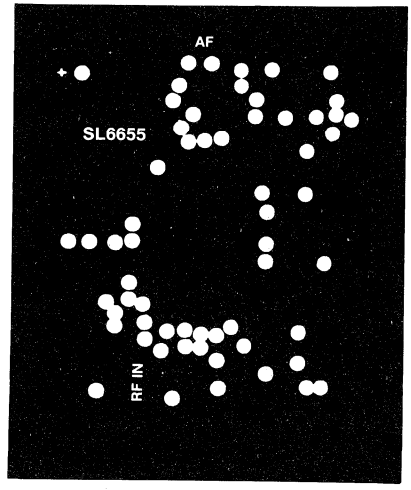


Fig.6a Ground plane (1:1)

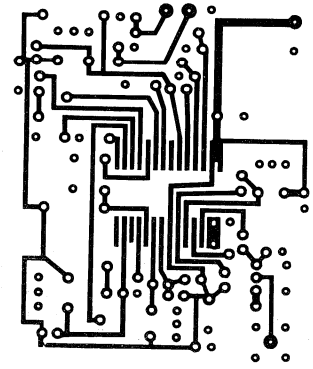


Fig.6b Copper track (1:1)

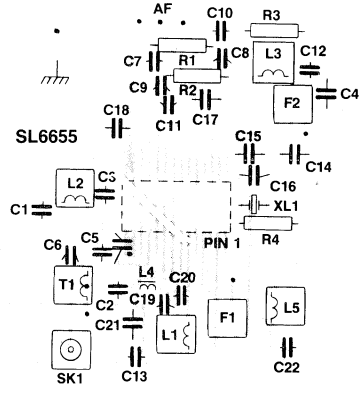


Fig.6c Component overlay (SL6655 surface mounted on track side of board (1:1)

PLESSEY
Semiconductors

PRELIMINARY INFORMATION

SL6670

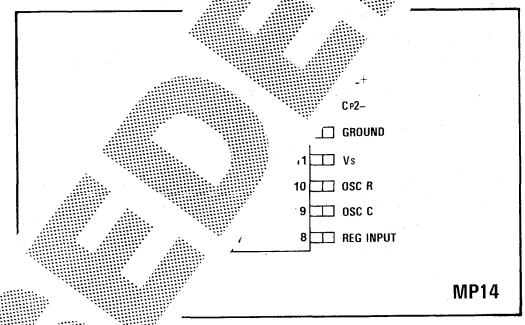
0.95V DC/DC VOLTAGE CONVERTER

The SL6670 is a novel Bipolar monolithic voltage multiplier designed to operate from supply voltages as low as **0.95V**

Voltage tripling uses a capacitor pump technique and no external coil is required.

Full load regulation is provided and the output can be pre-set to the desired voltage.

A programmable oscillator allows for optimisation of efficiency for any particular load. This can be switched into a very high efficiency 'standby' mode when very small load currents are required. The device also comes equipped with a battery flag monitor.



.1 Pin connections - top view

FEATURES

- High Power Efficiency
- 0.95V to 3V Supply
- 0.9V to 5V Output
- No Inductors Required
- Low Radiation
- Miniature Plastic Surface M

,ONS

- , Pager Power Supplies
- ,mory Back-up Supplies
- ,igh Efficiency Battery Powered DC/DC Converters

ORDERING INFORMATION

SL6670 MP

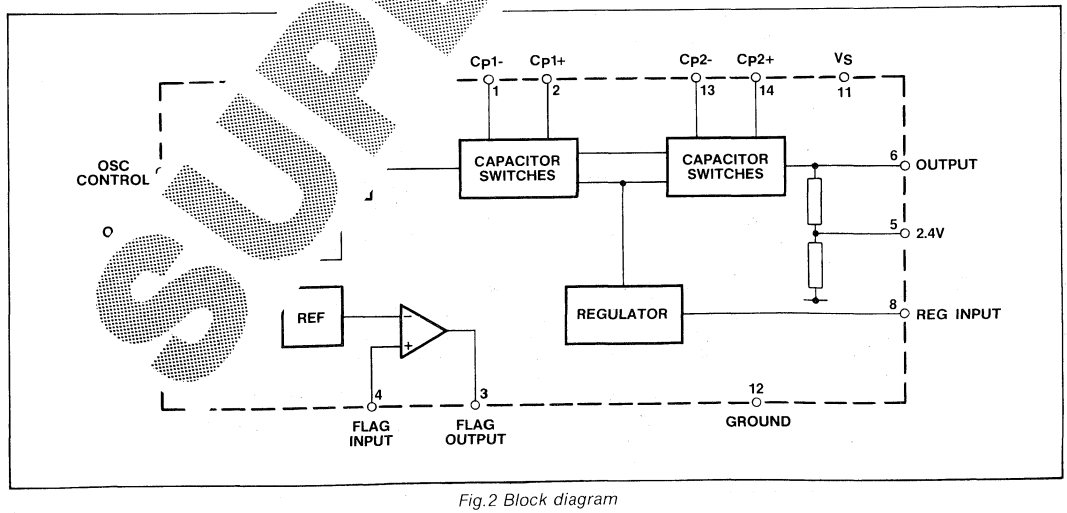


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = -30°C to +85°C, V_S = 1.05V to 8V Oscillator control high.

Characteristics	Pin No.	Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply voltage V_S	11	0.95V		3	V	T_{amb} = 25°C
Supply current I_S	11		180	250	μA	I_O = 0
Output current I_O	6	1.5			mA	V_S = 2.5V, [illegible] °C
		1			mA	V_S = 1V, [illegible]
Output voltage V_O	6	0.9		5	V	
Operating frequency range f_O	9,10			50	kHz	
Output source impedance Z_O	6		67		Ω	V_S [illegible] mA
Power conversion efficiency (See Note 1)			85		%	
Voltage tripling conversion efficiency (See Note 2)			99		%	
Oscillator control bias current	7			2		
Oscillator control high voltage	7	70				
Oscillator control low voltage	7			[illegible]		
Flag input impedance	4	1.5				
Flag output high voltage	3	70				[illegible] 10μA
Flag output low voltage	3					[illegible] 1μA
Flag threshold voltage						
Regulator input reference voltage	8					
Regulator input bias current	8					
Fixed output voltage option		[illegible]				T_{amb} = 25°C, I_O = 0

NOTES

1. Power conversion efficiency = $\frac{\text{Load curr}}{\text{[Input current - [illegible]}}$ x 100%

2. Voltage conversion efficiency = $\frac{\text{Output vol}}{\text{[3 x Input [illegible]}}$

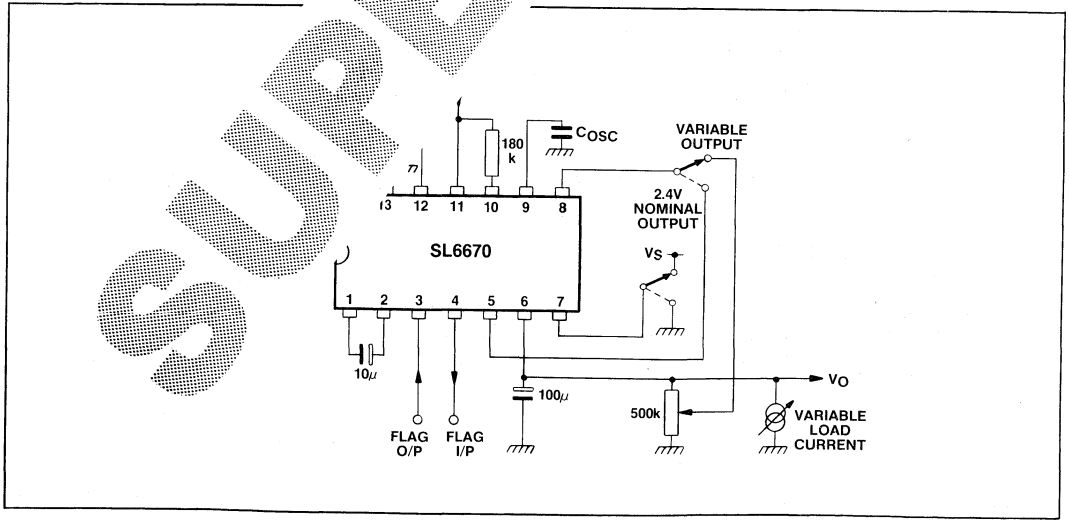


Fig.3 Test circuit

PIN DESIGNATIONS

Pin	Function
1	Capacitor between this pin and pin 2 to store pumping current.
2	Capacitor between this pin and pin 1 to store pumping current.
3	**Flag output.** This output is low when pin 4 is lower than the flag reference.
4	**Flag input.** Pin 3 output will be low when this pin is below the flag reference.
5	**2.4V nominal.** Tying this pin to pin 8, Regulator input, will set the output to nomi
6	**Output.** This pin drives the Tank capacitor and can be adjusted to any voltage
7	**Oscillator control pin.** When this pin is taken high the oscillator runs at a freque components on pins 9 and 10. When taken low the oscillator will run at 6⁰
8	**Regulator input.** The output voltage pin 6 is set by an external resistive divi pin 8 and ground. The regulator will keep this pin at 0.7V. Tying this pin to pir ɔ 2.4V.
9	**Oscillator capacitor.** A capacitor is connected from this pin to grour ılator frequency.
10	**Oscillator resistor.** A 180kΩ resistor connected from this pin to
11	**Battery voltage.** From 0.95V to 3V.
12	**Ground.**
13	Capacitor between this pin and pin 14 to store pumping
14	Capacitor between this pin and pin 13 to store pumping c equired on this pin if Vs is greater than 1.7V.

PRINCIPLE OF OPERATION

Because of the low input voltage the SL6670 uses a tw stage pump circuit, using external pump capacitors, wh will provide up to three times the input voltage at the o tank capacitor. A regulator is provided to enable the o be set at any voltage below this tripled output.

The operation of the device can best be de considering Fig.4, which shows an idealised vc Switches S1 are closed for half the clock cycl S2 open. The next half clock cycle, switch and switches S1 open. With switche capacitors charge up, towards Vs. Whe the charged capacitor are stacked one Vs, giving a maximum output of 3V

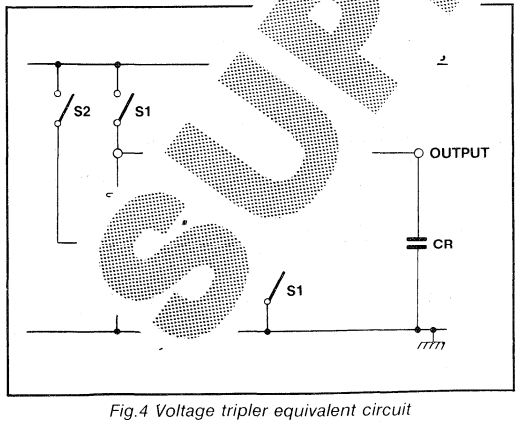


Fig.4 Voltage tripler equivalent circuit

PTION

uses a charge control method to charge the ɔrs sufficiently to keep the reservoir capacitor ı voltage regardless of load, thus achieving ı voltage regulation. The regulated output voltage ɔd by providing a feedback voltage to the regulator ın using an external resistive divider. Alternatively, a ɹt 2.4V nominal output pin is provided to minimise ɐrnal components.

Oscillator

The clock is provided by the on-chip oscillator, the frequency of which can be selected by choosing appropriate R and C values. The control pin will, when taken low, reduce the oscillator frequency to approximately 6% of its nominal value. This is useful where the load is variable, e.g. radio pagers with battery economy. Linking the oscillator control input to the battery economy signal will optimise the converter efficiency for the different load requirement.

Flag Circuit

A flag circuit is included which can be used to signal that the output has dropped below a preset level. Hysteresis can be provided with a feedback resistor. The flag circuit can also be used to check the battery supply if desired. Another use of the flag circuit is to lower the oscillator frequency when either the battery voltage or output drops below a preset limit.

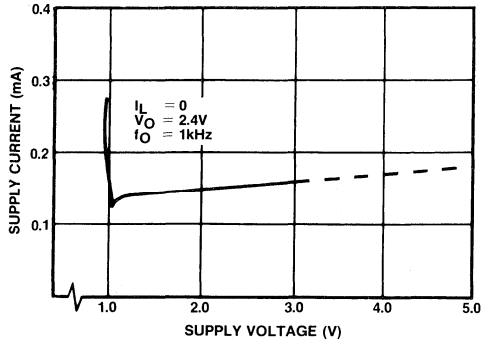
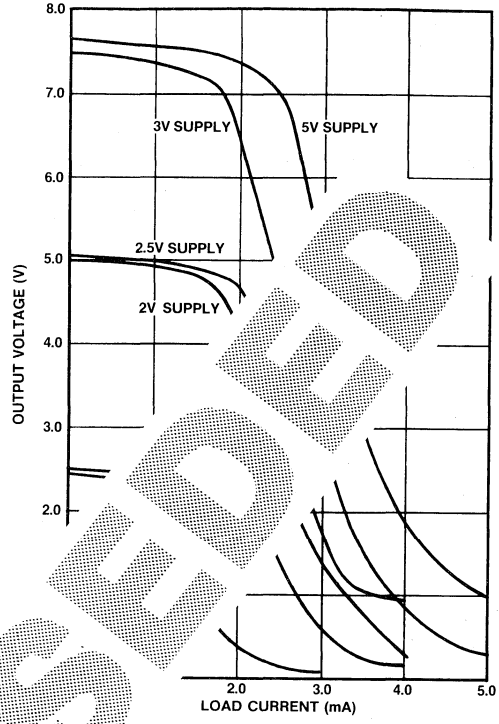


Fig.5 Supply current as a function of supply voltage



utput voltage as a function of load current

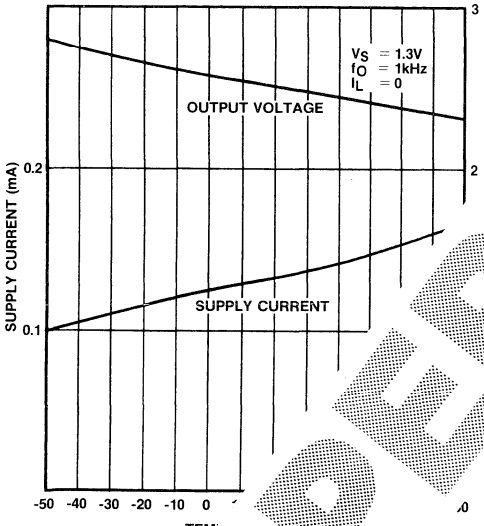


Fig.6 Output voltage *ction of*

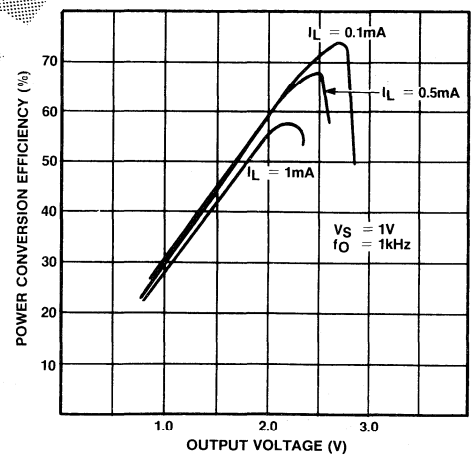


Fig.8 Power conversion efficiency as a function of regulated output voltage

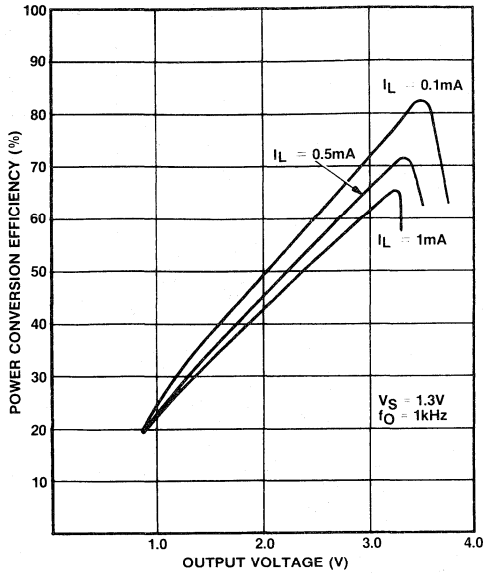


Fig.9 Power conversion efficiency as a function of regulated output voltage

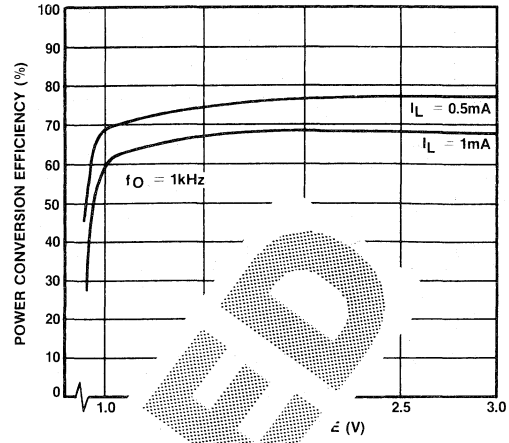


Fig.12 Op' ...fficiency as a function of ...ge

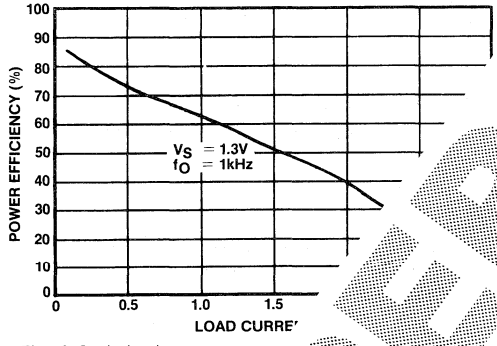


Fig.10 Optimised power conver ...n of load

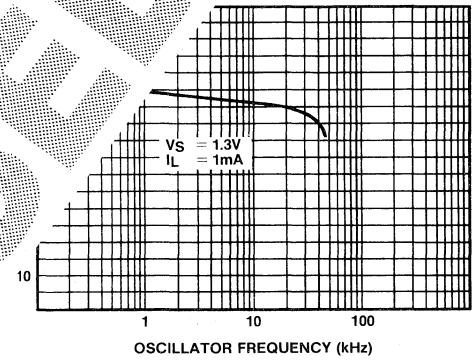


Fig.13 Power conversion efficiency as a function of oscillator frequency

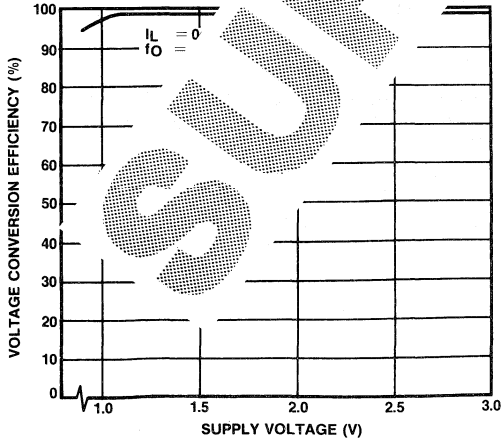


Fig.11 Optimised voltage conversion efficiency as a function of supply voltage

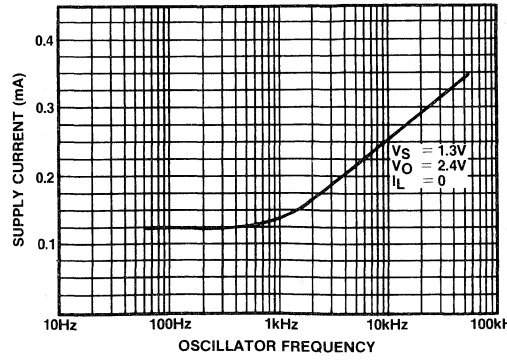


Fig.14 Supply current as a function of oscillator frequency

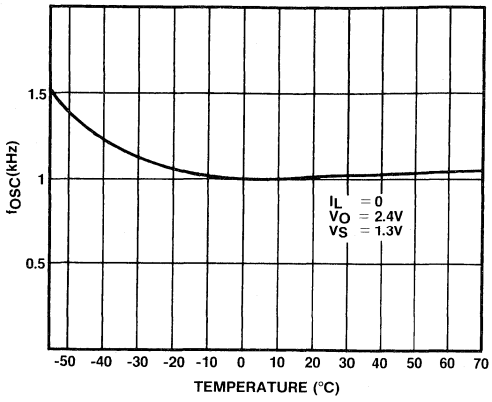


Fig.15 Oscillator frequency as a function of temperature

Fig.18 ...uency with load current

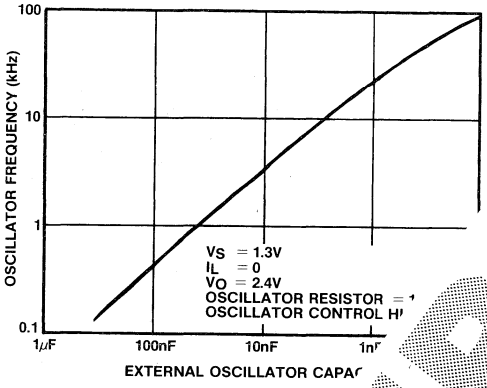


Fig.16 Oscillator frequency as a functio... capacitor

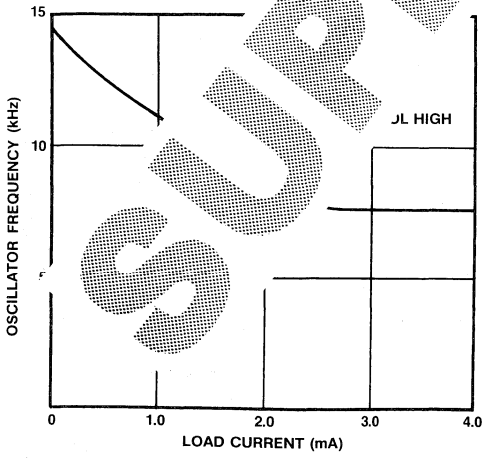


Fig.17 Variation of oscillator frequency with load current

EXT... S
C... apacitor

...rmines the amount of hysteresis in ...d be 180kΩ for correct operation. The ...ch will depend on the frequency of ..., can be calculated as follows:

$$C_{OSC} \approx \frac{26}{f}$$

...ator control pin is high.
..., is in μF and f is in Hz, or obtained from the ...iate graph.

...np Capacitors

The pump capacitors C_P store the pumping charge before it is transferred to the tank capacitor. For the regulator to maintain optimum efficiency the pump capacitors must be equal in value. The pump capacitor value is chosen to ensure the droop voltage ΔV_P is acceptable.

$$\Delta V_P = \frac{I_{LOAD}}{fC_P}$$

The magnitude of ΔV_P is chosen considering the worst case input-output voltage expected.

$$\Delta V_P < \frac{[3V_S - V_O]}{2}$$

where ΔV_P is droop voltage on each pump capacitor.
If this consideration is not met the output will fall out of regulation.

Reservoir Capacitors

The reservoir capacitor integrates the ripple at the output. To reduce the ripple ΔV_O the reservoir capacitor C_R must be of the correct value.

$$\Delta V_O = \frac{I_{LOAD}}{2C_R f}$$

where f is clock frequency in Hz.

Schottky Diode

A Schottky diode is required from pin 14 to ground if V_S exceeds 1.7V. This protects the chip should the output be short circuited. If the diode is not present the device will remain in a non-destructive latched state; removing the supply will ensure normal operation. The inclusion of the diode will not affect the device operation and no change in device specification is required; the diode only acts as a catching diode under fault conditions and carries no current under normal operation.

CONSIDERATIONS FOR HIGH EFFICIENCY

Frequency

The efficiency of the SL6670 is dependent on the oscillator frequency. As the oscillator frequency is increased the switching losses increase, so lowering the efficiency.

Pump Capacitors

The regulator controls the amount of charge transfer assuming that both pump capacitors have the same charge characteristic. Therefore, for optimum efficiency, the pump capacitors should be the same value. To obtain optimum efficiency the value of pump capacitors must be chosen so that the regulator is always in regulation.

Reservoir Capacitor

The reservoir capacitor must be chosen to reduce the output ripple. For optimum efficiency the regulator must see a signal at its inputs which has no large ripple compone

Regulator

The regulator will control the output voltage to r between 0.9V and 5V, depending on the value r control range in any application is set by Vs but t not necessarily be efficient at all settings of r When the output voltage is set close to Vs, the amount of charge that can be transfer capacitors to the reservoir capacitor, a fall. When the output is set close to 3\ may be insufficient, due to internal achieve the required output. The drive the output higher than is currents into the switches, ev will reduce the efficiency nea

ıis

ıtor.

DESIGN EXAMPLE

2.4V Supply from Si ,e in Radio Pager

A major use of ' g a high voltage supply to enab' ıte from battery voltages dowr ıy from 1.7V when new to 0.9V ' ıery voltage of 0.95V, the maxim ıL6670 will be 2.85V. A good ch ıld be 2.4V because this allows ər to be used.

The requireme dependent on the ripple sizes. In the case of direct conversion rge amounts of gain at low frequencies, a hi or frequency will ease the supply decoupling require A frequency of about 18kHz is acceptable, which gives a value of oscillator capacitor of 1.5nF.

The maximum droop voltage that can be allowed is:

$$\frac{3V_S - V_O}{2} = 225mV$$

Using a load of 1mA and a 1µF capacitor for C_P:

$$\frac{I_{LOAD}}{fC_P} = 56mV \text{ droop voltage}$$

This is well below 225mV and is an ' eptable value.

Using a 100µF capacitor for the re acitor will give:

$$\frac{I_{LOAD}}{2C_Rf} = 0.3mV$$

If the oscillator control cillator frequency when the r sed', the performance at this n ked. When 'battery economised' om 1mA to, say, 50µA. The dr

$$\frac{50\mu}{18kHz \times 6}$$

eptable value

Output '

$$\times \frac{6}{100} = 0.23mV$$

ly voltage is 1.7V the extra Schottky t be required.

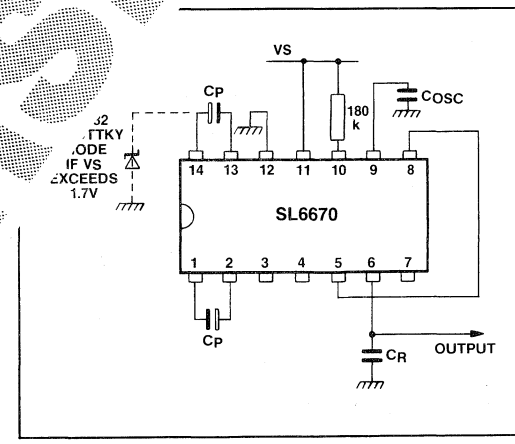


Fig.19 Simple positive converter with fixed 2.4V output

TYPICAL APPLICATIONS

Simple Positive Voltage Converter

A major application of the SL6670 is the conversion of a single cell battery to a higher voltage suitable for the supply of CMOS circuits. A typical application would be in radio pagers and Fig.19 shows a typical application. The use of 2.4V output will allow the use of the on-chip resistors and so reduce the external component count. The Schottky diode will be required if V_S exceeds 1.7V.

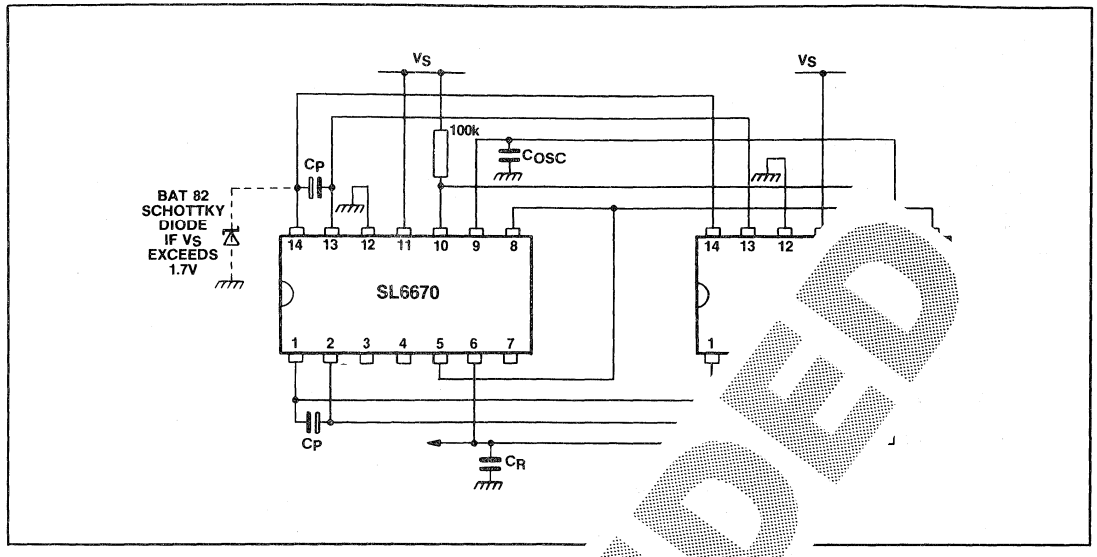


Fig.20 Paralleling devices

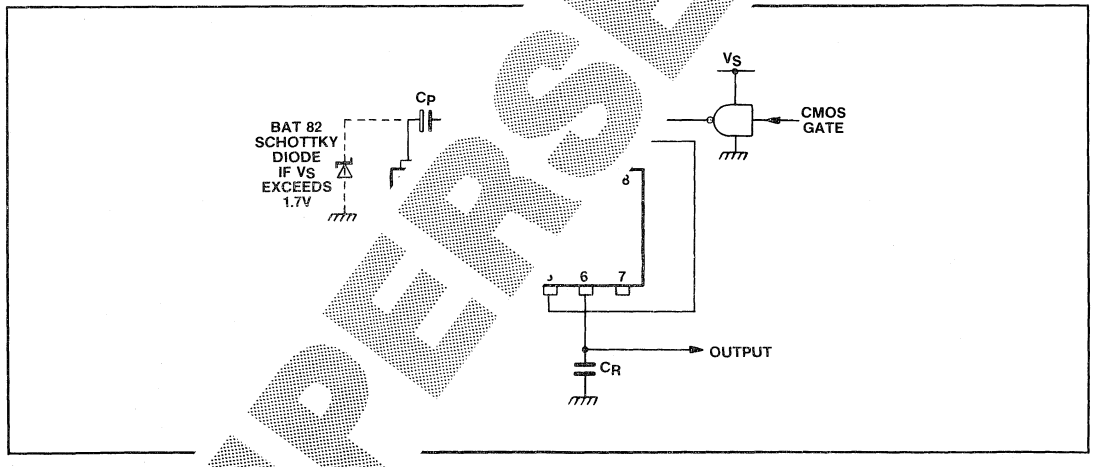


Fig.21 External clocking of SL6670

Paralle'

An ,oltage converters may be paralle .put current capability. The reservoir ıp capacitors and oscillator components devices, see Fig.20. Individual components cou used for the oscillator and pump capacitors on each ıı.dividual device if required.

Cosc should be doubled when paralleling devices for the same operating frequency.

External Clocking of SL6670

In some applications it may be advantageous to externally control the internal oscillator. This can be achieved as shown in Fig.21.

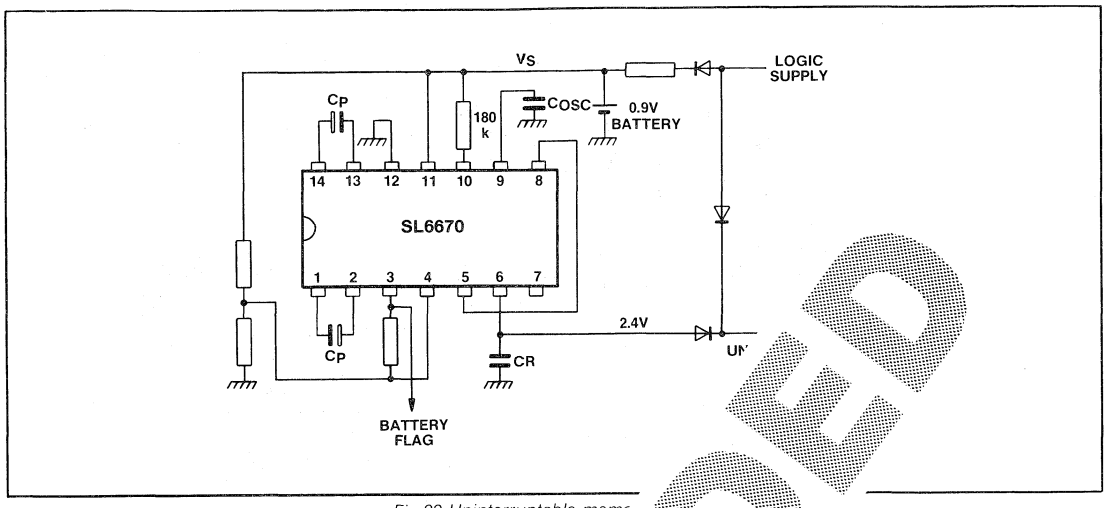
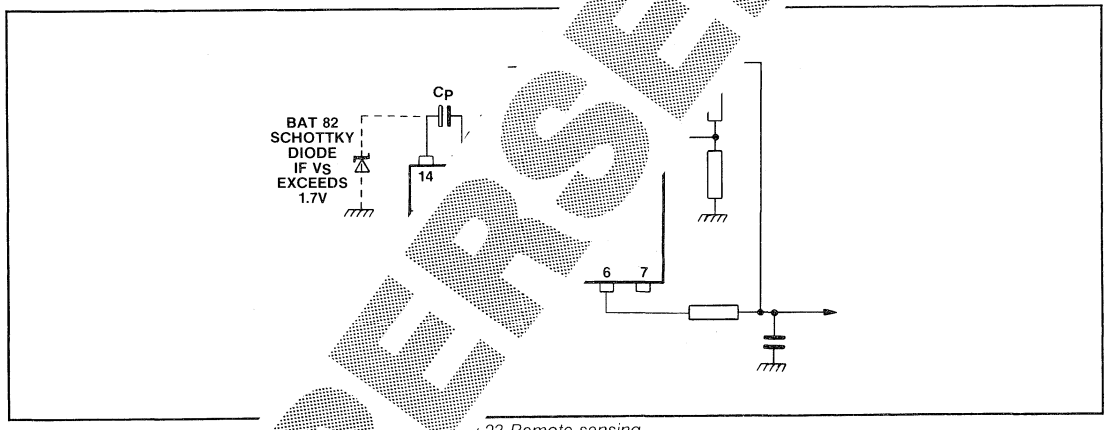


Fig.22 Uninterruptable memc



g.23 Remote sensing

Uninterruptable

Fig.22 shows a standby memory supply. The h .ne battery supply is nearly disch

Remote

Th .1 be used for remote sensing applica. .-ig.23.

Separate Re. coupling

In applications . .re the high output ripple can be tolerated the regulator can be separately decoupled with a small capacitor on Pin 8 as shown in Fig.24. In applications where large load glitches appear on the output a more complex smoothing network can be incorporated between the output, pin 6, and pin 8 or, for fixed 2.4V output, between pin 5 and pin 8.

3V Battery to 5V Logic Supply

Fig.25 shows the SL6670 used to provide a 5V supply from a 3V battery. The circuit continues to work even when the battery is exhausted at 1.8V. The battery flag will sense when the battery is exhausted.

R1 and R2 set the voltage where the flag is required to switch and R_F sets the value of hysteresis required.

R3 and R4 set the regulated output voltage. In normal operation 0.7V will appear across R4 and V_O-0.7V will appear across R3.

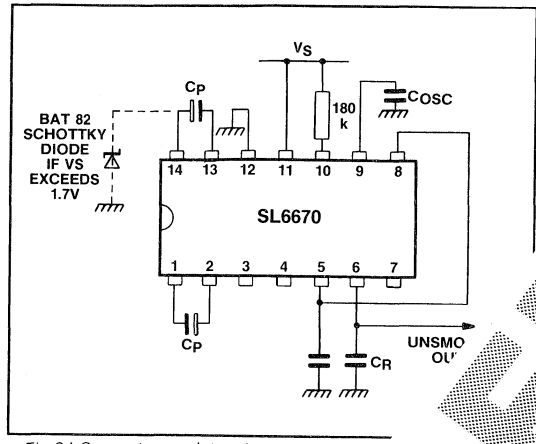
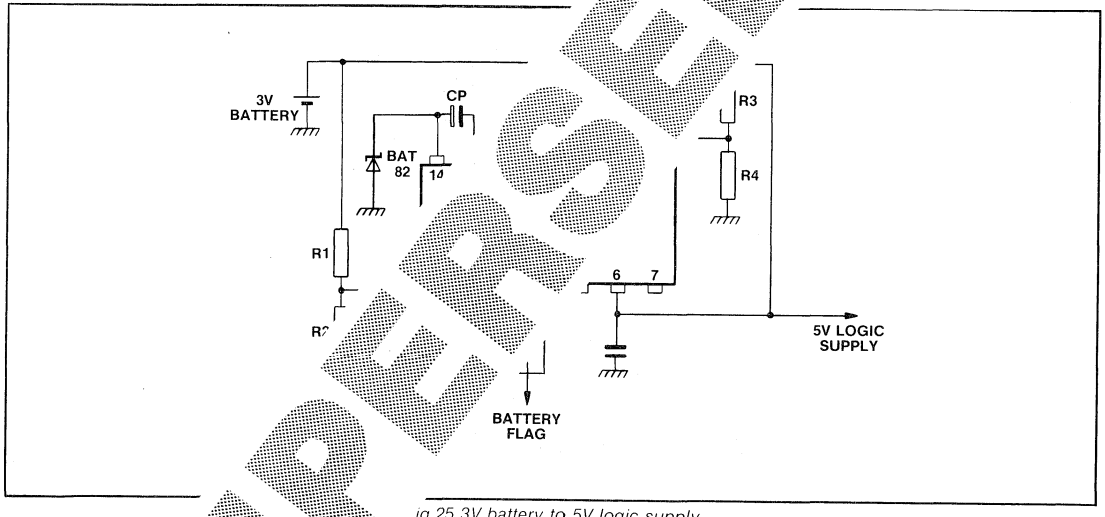


Fig.24 Separate regulator decoupling with f



ig.25 3V battery to 5V logic supply

SL6691C

IF SYSTEM FOR PAGING RECEIVERS

The SL6691C is an IF system for paging receivers, consisting of a limiting IF amplifier, quadrature demodulator, voltage regulator and audio tone amplifier with Schmitt trigger.

The voltage regulator requires an external PNP transistor as the series pass transistor. The frequency response of the tone audio amplifier is externally defined.

The SL6691C operates over the temperature range -30° C to +85° C.

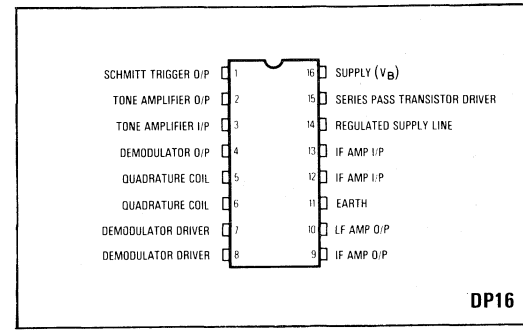


Fig.1 Pin connections (top view)

FEATURES

- Very Low Standby Current
- Fast Turn-on
- Wide Dynamic Range
- Minimum External Components

APPLICATIONS

- Pagers
- Portable FM Broadcast Receivers

ABSOLUTE MAXIMUM RATINGS

Storage temperature – 65°C to + 150°C
Supply voltage 6V

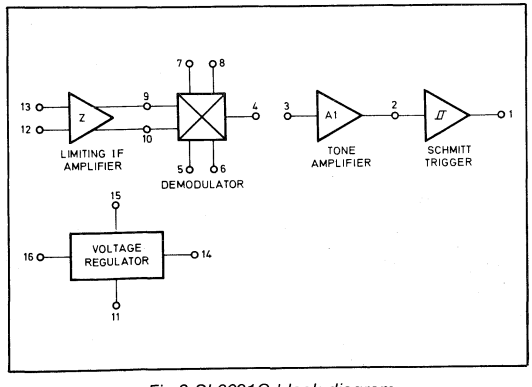


Fig.2 SL6691C block diagram

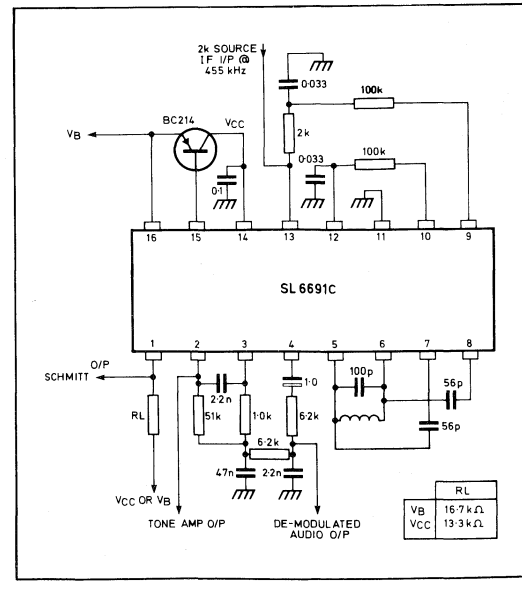


Fig.3 SL6691C test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Temperature	-30°C to +85°C
Supply voltage (V_C)	2.5V
IF frequency	455kHz (nominal)
Modulation frequency	500Hz
Deviation	±4.5kHz

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Quiescent current		1.0	1.4	mA	V_B = 3V Pins 2 and 3 S/C Pins 1 and 4 O/C
Switch on time		12	18	ms	Note 1
Voltage regulator					
Regulated voltage	1.9		2.1	V	V_B > 2.2V
Supply line rejection		40		dB	V_B > 2.2V 200mV p-p square wave @ 500 Hz injected
Current sink capability pin 15	100			µA	
IF amplifier					
Input impedance		20//2		kΩ//pF	
Output impedance		2		kΩ	
Dynamic range		100		dB	
Output voltage swing		600		mV p-p	
Amplifier gain		90		dB	
Sensitivity	20	16		µV rms	Audio 20dB S+N/N ratio
AM rejection		40		dB	100µV rms I/P @ 30% AM modulation
Amplifier 3dB bandwidth		1.5		MHz	
Demodulator					
Audio output	8	15		mV rms	Quadrature element L-C tuned circuit: Q = 30
Distortion, THD		1.5	3	%	
Output impedance		1	3	kΩ	
Signal-to-noise ratio		40		dB	100µV rms I/P 3kHz audio bandwidth
Tone amplifier					
Open loop gain		54		dB	
Peak output current		20		µA	
Schmitt trigger					
Mark space ratio		45/55	38/62		20µV rms I/P
Output current				µA	

NOTES

1. The 'Switch On' time is the time to the zero crossing point of the centre of the first occurrence of a 30/70 or 70/30 mark space wave on the output of the Schmitt trigger after the supply voltage has been switched on. Conditions: V_B = 2V, Tone filter connected (See Fig.3), IF input = 100µV rms, Modulation 500Hz @ 2kHz deviation.

CIRCUIT DESCRIPTION

IF Amplifier and Detector

The IF amplifier consists of five identical differential amplifier/emitter follower stages with outputs at the fourth (pins 9 and 10) and fifth (pins 7 and 8) stages. The outputs from the fourth stage are used when the lowest turn-on time is required. Coupling to the quadrature network of the detector is via external capacitors; otherwise the design is conventional. The audio output is taken from pin 4 and filtered externally.

Tone (Audio) Amplifier

The tone amplifier is a simple inverting audio amplifier with voltage gain determined by the ratio of feedback resistor to input resistor. The frequency response can readily be controlled by suitable selection of feedback components.

Schmitt Trigger

The Schmitt trigger has an open collector output stage which saturates when the input at pin 2 is high. A 20µV rms input is sufficient.

NOMINAL DC PIN VOLTAGES(DP16)

Function	Pin	Voltage
Supply	16	Battery voltage
Series pass transistor driver	15	Battery voltage –0.7V
Regulated supply line	14	2V
Earth	11	0V
IF amp I/P	13	1V
IF amp I/P	12	1V
IF amp O/P	10	1V
IF amp O/P	9	1V
Demodulator O/P	4	1V
Quadrature coil	6	1V
Quadrature coil	5	1V
Tone amplifier I/P	3	1.4V
Schmitt trigger O/P	1	0V or pin 16 or pin 14
Tone amplifier O/P	2	1.4V
Demodulator driver	7	1V
Demodulator driver	8	1V

PLESSEY
Semiconductors

SP8703

1GHz LOW CURRENT TWO-MODULUS DIVIDER

The SP8703 is a divide by 128/9 programmable divider with a maximum specified operating frequency of 1GHz.

The signal (clock) inputs are biased internally and require to be capacitor coupled.

The output stage is CMOS compatible only, the 0 to 1 output edge giving best loop delay performance.

A unique 'power-down' feature is included to minimise power consumption.

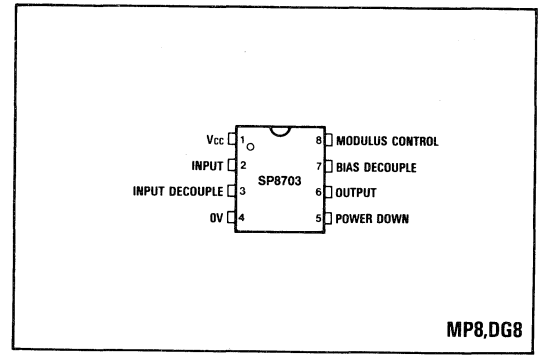


Fig.1 Pin connections - top view

FEATURES

- DC to 1GHz Operation
- -30° to +70°C Temperature Range
- Unique Power-Down Feature
- CMOS Compatible

QUICK REFERENCE DATA

- Supply Voltage 5.0V ± 0.25V
- Supply Current 30mA Typical

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6V
Storage temperature range	-30°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

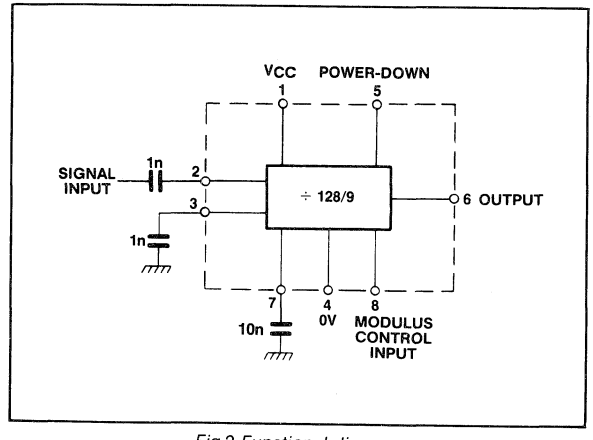


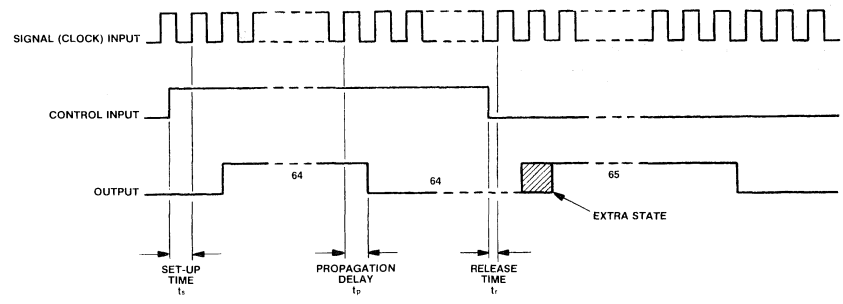
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = +4.75V to 5.25V, T_{amb} = -30°C to +70°C

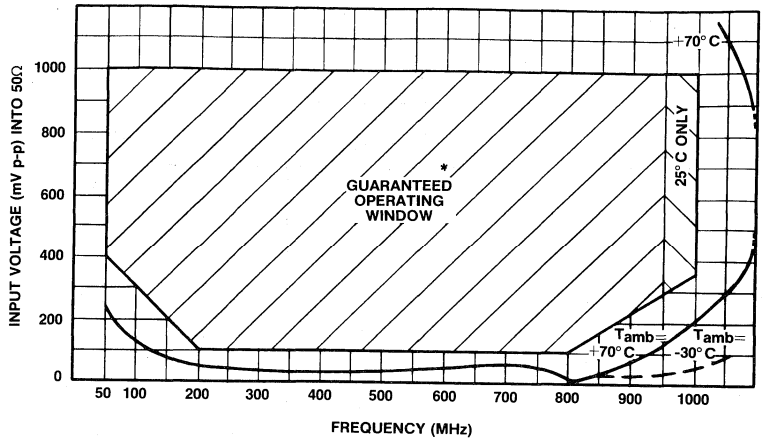
Characteristics	Value		Units	Conditions	Notes
	Min.	Max.			
Maximum frequency	1000		MHz	T_{amb} = 25°C	Note 1,2,4
Maximum frequency	950		MHz		Note 1,2,3
Minimum frequency (sinewave)		50	MHz		Note 1,2,3
Power supply current		40	mA	Power-up	Note 3
Power supply current		3	mA	Power-down	Note 3
Output high voltage	3.2	V_{CC}	V	IL = -0.2mA	Note 3
Output low voltage	0	1.7	V	IL = 0.2mA	Note 3
Control input high voltage	3.2	V_{CC}	V	Divide by 128	Note 3
Control input low voltage	0	1.7	V	Divide by 129	Note 3
Control input high current		50	μA	Input = V_{CC}	Note 3
Control input low current	-10		μA	Input = 0V	Note 3
Power-down high voltage	3.2	V_{CC}	V	Power-down	Note 3
Power-down low voltage	0	1.7	V	Power-up	Note 3
Power-down high current		10	μA	Input = V_{CC}	Note 3
Power-down low current	-2		μA	Input = 0V	Note 3
Clock to output delay		30	ns	CL = 10pF	Note 5
Set-up time		15	ns	CL = 10pF	Note 5
Release time		15	ns	CL = 10pF	Note 5

NOTES
1. See Fig.4 for guaranteed operating window.
2. See Fig.5 for input voltage measurement method.
3. Tested at 25°C and +70°C only.
4. Tested at 25°C only.
5. Guaranteed but not tested.



NOTE
The set-up time t_s is defined as the minimum time that can elapse between a L→H transition of the control input and the next L→H clock pulse transition to ensure that the ÷128 mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H→L transition of the control input and the next L→H clock pulse transition to ensure that the ÷129 mode is obtained.

Fig.3 Timing diagram



*Tested as specified in table of Electrical Characteristics

Fig.4 Typical input characteristics

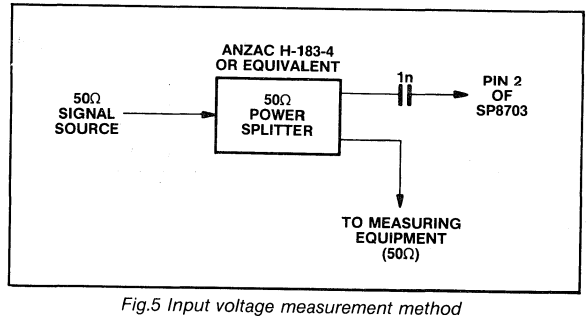


Fig.5 Input voltage measurement method

OPERATING NOTES

1. The inputs are biased internally and coupled to a signal source with suitable capacitors.
2. If no signal is present the devices will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from one input to pin 4 (ground). This will reduce the sensitivity.
3. The circuits will operate down to DC but slew rate must be better than 100V/μs.
4. The output stage is of an unusual design and is intended to interface with CMOS. External pull-up resistors or circuits must not be used.

SP8704

950MHz VERY LOW CURRENT MULTI-MODULUS DIVIDER

The SP8704 is a switchable divide by 128/129, 64/65 programmable divider with a maximum specified operating frequency of 950MHz.

The signal (clock) inputs are biased internally and require to be capacitor coupled.

The SP8704 will operate from any supply from 3V to 5V and features full electrostatic discharge protection.

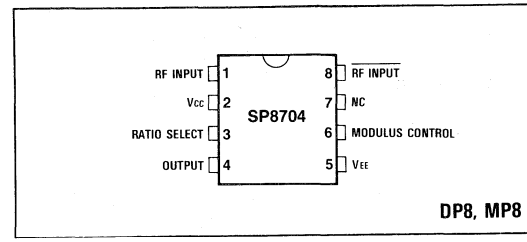


Fig.1 Pin connections - top view

FEATURES

- DC to 950MHz Operation
- -40°C to +85°C Temperature Range
- Operation from 3V to 5V Supply
- ESD Protection on all Pins

QUICK REFERENCE DATA

- Supply Voltage 3V to 5V
- Supply Current 10mA - Including Output Emitter Follower

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7V
Storage temperature range	-55°C to +125°C
Junction temperature	+175°C
Input voltage	2.5V p-p

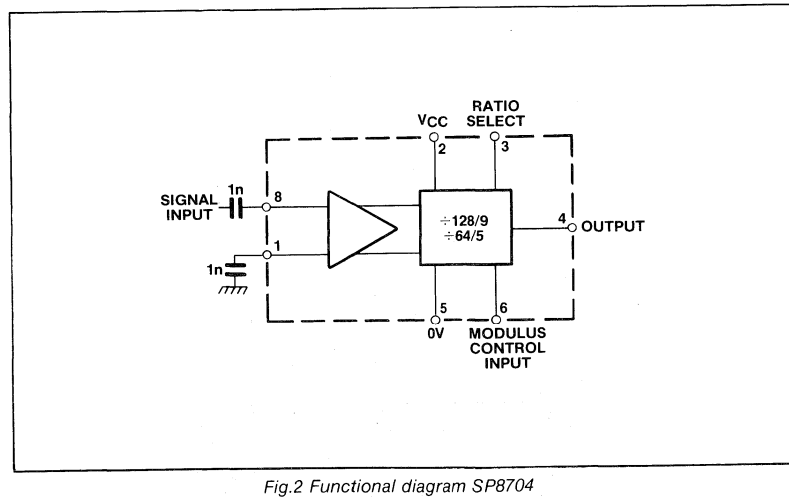


Fig.2 Functional diagram SP8704

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -40°C to 85°C, V_{CC} = +2.75V to +5.5V

Characteristic		Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current			10		mA	Including output emitter follower
Input sensitivity	10MHz			150	mV rms	Sinewave input into 50Ω
	80MHz			25		
	150MHz			15		
	850MHz			15		
	950MHz			50		
Input impedance			50		Ω	
			2		pF	
Output			1		V pk-pk	Emitter follower output current source = 0.75mA
Ratio select (pin 3)	LO			1	V	128/129 selected
	HI	V_{CC}			V	64/65 selected
Modulus control (pin 6)	LO			1	V	65 or 129 selected
	HI	2			V	64 or 128 selected
Clock to output delay			8		ns	
Set up time			16		ns	
Release time			16		ns	

TRUTH TABLE

Pin 3	Pin 6	Division ratio
L	L	129
L	H	128
H	L	65
H	H	64

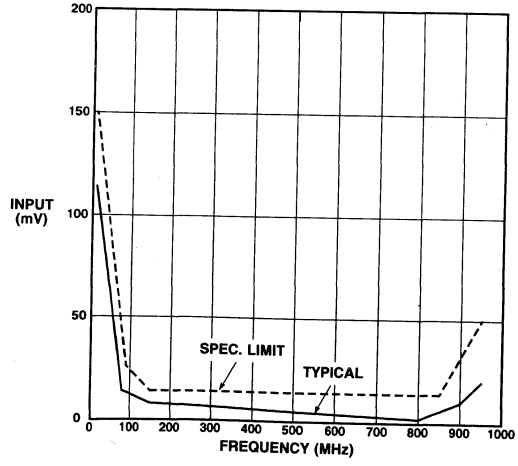


Fig.3 Typical input sensitivity at 85°C

SP8705

1100MHz VERY LOW CURRENT MULTI-MODULUS DIVIDER

The SP8705 is a switchable divide by 128/129, 64/65 programmable divider with a maximum specified operating frequency of 1100MHz.

The signal (clock) inputs are biased internally and require to be capacitor coupled.

The SP8705 will operate from any supply from 3V to 5V and features full electrostatic discharge protection.

FEATURES

- DC to 1100MHz Operation
- -40°C to +85°C Temperature Range
- Operation from 3V to 5V Supply
- ESD Protection on all Pins

QUICK REFERENCE DATA

- Supply Voltage 3V to 5V
- Supply Current 5mA - Including Output Emitter Follower

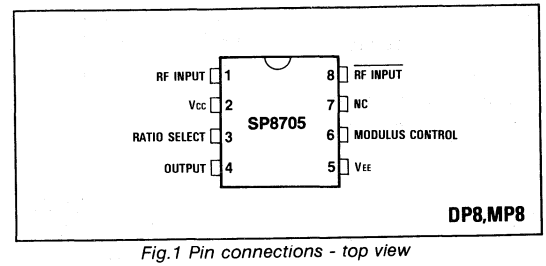


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage:	7V
Storage temperature range:	-55°C to +125°C
Junction temperature:	+175°C
Input voltage:	2.5V p-p

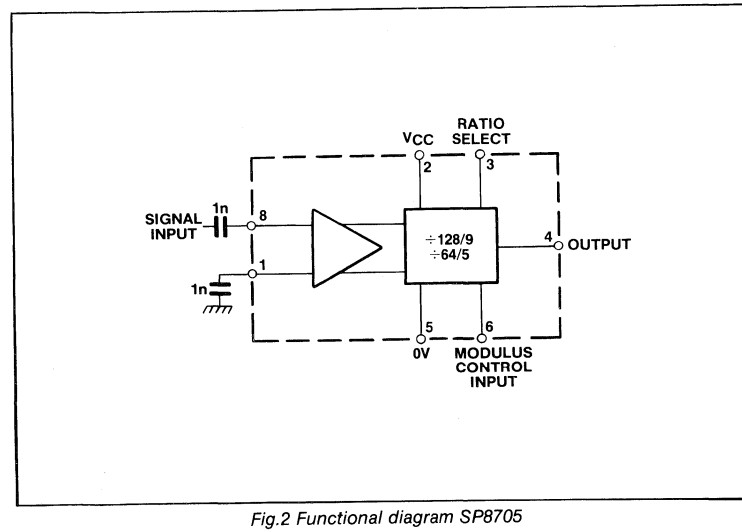


Fig.2 Functional diagram SP8705

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -40° C to 85° C, V_{CC} = +2.75V to +5.5V

Characteristic		Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current				5	mA	Including output emitter follower
Input impedance			50		Ω	
			2		pF	
Ratio select (pin 3)	LO			1	V	128/129 selected
	HI	V_{CC}			V	64/65 selected
Modulus select (pin 6)	LO			1	V	64 or 129 selected
	HI	2			V	64 or 128 selected
Clock to output delay			8		ns	

TRUTH TABLE

Pin 3	Pin 6	Division ratio
L	L	129
L	H	128
H	L	65
H	H	64

SP8706

950MHz VERY LOW CURRENT TWO-MODULUS DIVIDER

The SP8706 is a divide by 80/81 programmable divider with a maximum specified operating frequency of 950MHz.

The signal (clock) inputs are biased internally and require to be capacitor coupled.

The SP8706 will operate from any supply from 3V to 5V and features full electrostatic discharge protection.

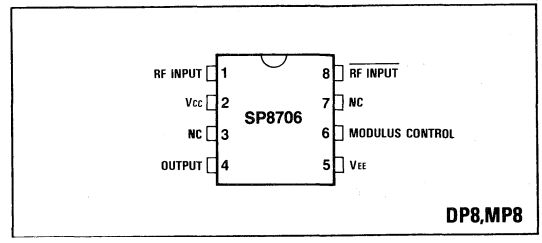


Fig.1 Pin connections - top view

FEATURES

- DC to 950MHz Operation
- -40°C to +85°C Temperature Range
- Operation from 3V to 5V Supply
- ESD Protection on all Pins

QUICK REFERENCE DATA

- Supply Voltage 3V to 5V
- Supply Current 10mA - Including Output Emitter Follower

ABSOLUTE MAXIMUM RATINGS

Supply voltage:	7V
Storage temperature range:	-55°C to +125°C
Junction temperature:	+175°C
Input voltage:	2.5V p-p

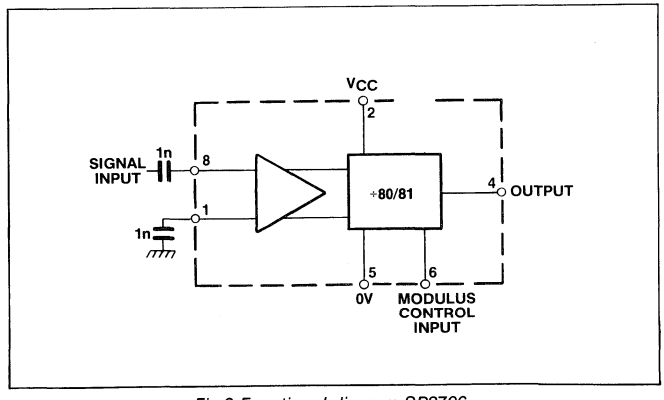


Fig.2 Functional diagram SP8706

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -40° C to 85° C, V_{CC} = +2.75V to +5.5V

Characteristic		Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current			12		mA	Including output emitter follower
Input sensitivity	10MHz			150	mV rms	Sinewave input into 50Ω
	80MHz			25		
	150MHz			15		
	850MHz			15		
	950MHz			50		
Input overload		150			mV rms	
Input impedance			50		Ω	
			2		pF	
Output			1		V p - p	Emitter follower output current source = 0.75mA
Modulus control (pin 6)	LO			1	V	81 selected
	HI	2			V	80 selected
Clock to output delay			8		ns	

PLESSEY
Semiconductors

PRELIMINARY INFORMATION

SP8710B

225MHz LOW POWER TWO MODULUS DIVIDER ÷ 100/101

The SP8710 is a Low Power Two Modulus Divider with a divide by 100 ratio when the modulus control input is high and 101 when the input is low. The device also features a power down mode and will operate with a 3V power supply.

FEATURES

- Low Power High Speed
- Power Down Mode
- CMOS Compatible Output Capability
- Ideal for Decade Synthesisers
- 3V Supply Operation

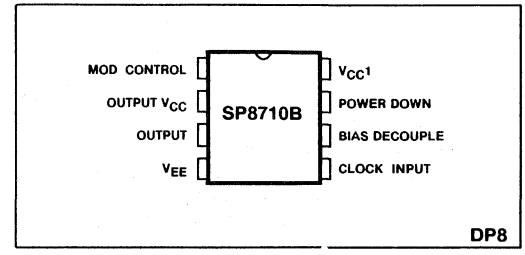


Fig.1 Pin connections - top view

QUICK REFERENCE DATA

- Supply Voltage Range 3V to 10V
- Industrial Temperature Range: -40°C to 85°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	12V
Clock input level	2.5V p-p
Junction temperature	+175°C
Storage temperature range	-55°C to +125°C

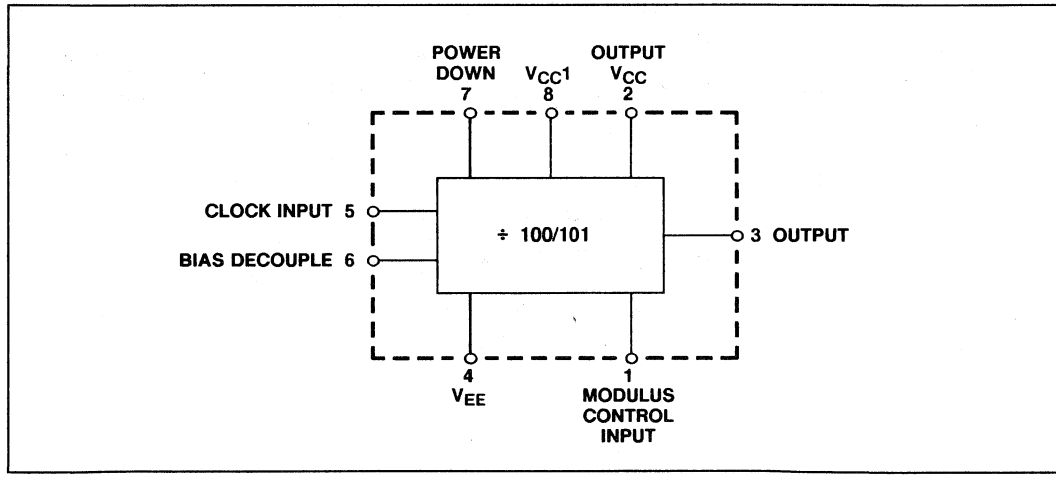


Fig.2 SP8710 functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = SP8710A -55°C to +125°C, SP8710B -40°C to +85°C, V_{CC} = +3V to +10V

Characteristic	Pin	Value		Units	Conditions
		Min.	Max.		
Max. sinewave input frequency	5	225		MHz	Input = 200mV - 1200mV p-p
Min. sinewave input frequency	5		20	MHz	Input = 400mV - 950mV p-p
Min. slew rate for LF operation	5		100	V/µs	
Power supply current I_{EE}	8		8	mA	Power up V_{CC} = 5V
			8.5	mA	Power up V_{CC} = 10V
			1	mA	Power down
Output low voltage	3	0	0.5	V	Load = 10pF//100k
Output high voltage		V_{CC}-0.9	V_{CC}	V	Load = 10pF//100k, V_{CC} = 5V
		V_{CC}-0.95	V_{CC}	V	Load = 10pF//100k,V_{CC} = 10V
Modulus control input high voltage	1	0.6V_{CC}	V_{CC}	V	
Modulus control input low voltage	1	0	0.4V_{CC}	V	
Modulus control input high current	1		20	µA	Input = V_{CC}
Modulus control input low current	1		-10	µA	Input = 0V
Clock to output propagation delay	5,6,7		80	ns	
Set up time	1		10	ns	
Release time	1		10	ns	
Power down input high voltage	7	0.6V_{CC}	V_{CC}	V	
Power down input low voltage	7	0	0.4V_{CC}	V	
Power down input high current	7		1	µA	
Power down input low current	7		-1	µA	

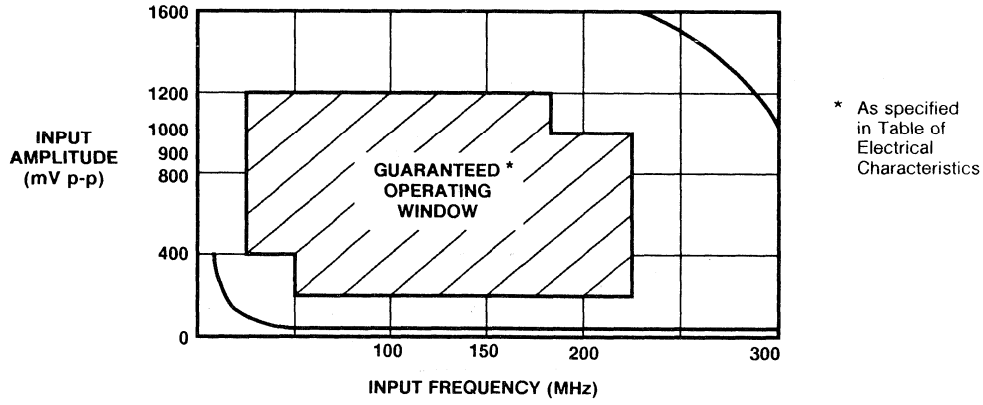


Fig.3 Typical input characteristics SP8710

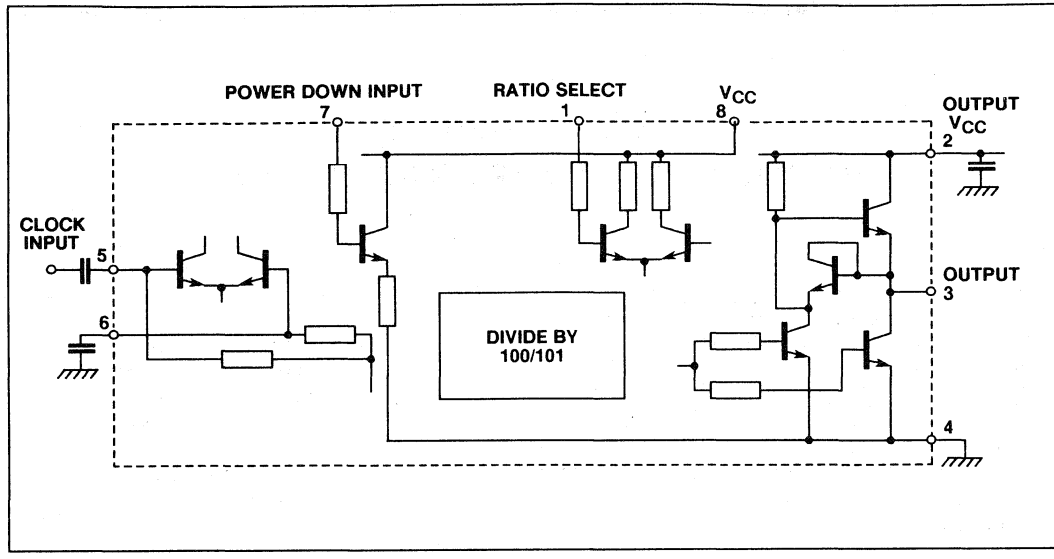


Fig.4 Typical application showing interfacing

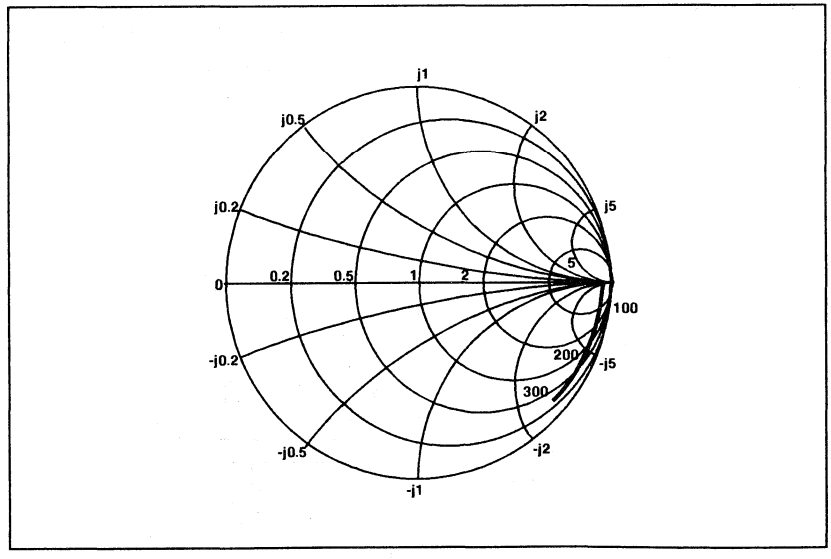


Fig.5 Typical Input Impedance. Test conditions:supply voltage 5V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 Ohms

PLESSEY
Semiconductors

SP8716/8/9

520MHz LOW CURRENT TWO MODULUS DIVIDERS

SP8716 ÷ 40/41, SP8718 ÷ 64/65, SP8719 ÷ 80/81 are 50mW programmable dividers with a maximum specified operating frequency of 520MHz over the temperature range -40 °C to +85 °C.

The signal (clock) inputs are biased internally and require to be capacitor coupled. The output stage is of an unusual low power design featuring dynamic pull-up, and optimised for driving CMOS. The 0 to 1 output edge should be used to give the best loop delay performance.

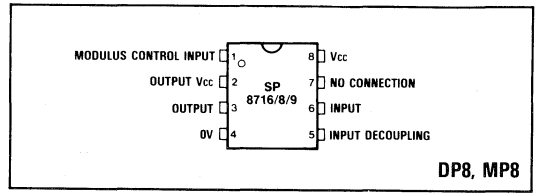


Fig.1 Pin connections - top view

FEATURES

- DC to 520MHz Operation
- -40°C to +85°C Temperature Range
- Control Inputs and Outputs are CMOS Compatible

QUICK REFERENCE DATA

- Supply Voltage 5.2V ± 0.25V
- Supply Current 10.5mA typ.

ABSOLUTE MAXIMUM RATING

Supply voltage (pin 2 or 8):	8V
Storage temperature range:	-55 °C to +150 °C
Max. junction temperature:	+175 °C
Max. clock input voltage:	2.5V p-p

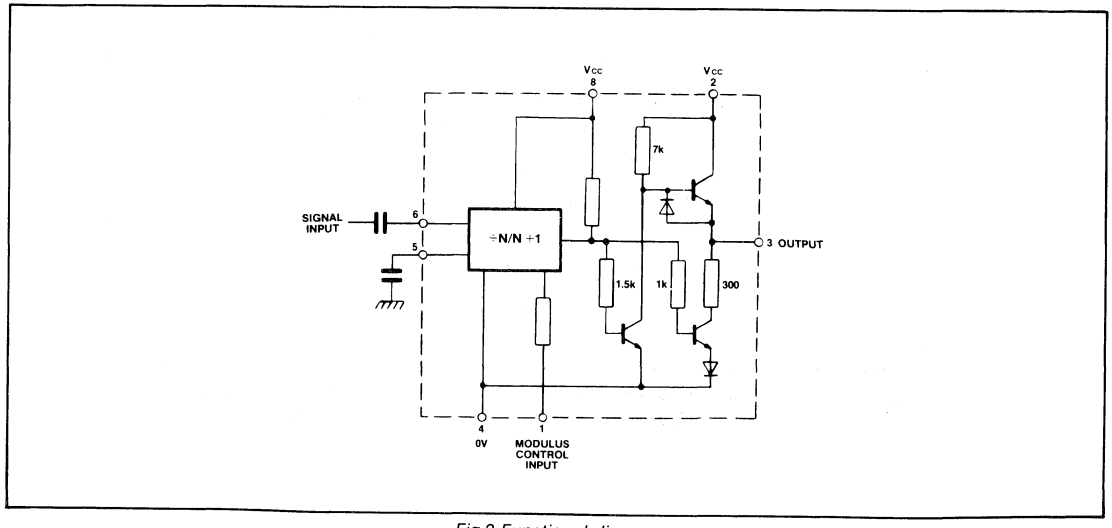


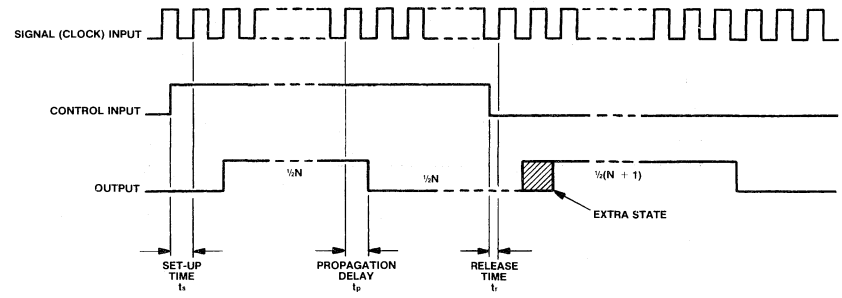
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage: V_{CC} = +4.95 to 5.45V, Temperature: T_{amb} = -40°C to +85°C

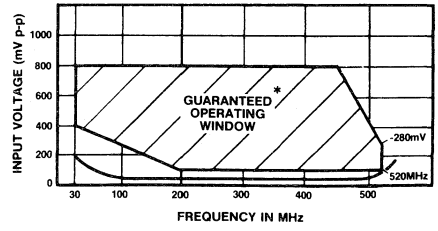
Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Max. frequency	f_{max}	520		MHz	Input 100-280mV p-p	1
Min. frequency (sinewave input)	f_{min}		30	MHz	Input 400-800mV p-p	2
Power supply current	I_{CC}		11.9	mA	C_L = 3pF; pins 2, 8 linked	1
Output high voltage	V_{OH}	(V_{CC} -1.2)		V	I_L = -0.2mA	1
Output low voltage	V_{OL}		1	V	I_L = 0.2mA	1
Control input high voltage	V_{INH}	3.3	8	V	÷N	1
Control input low voltage	V_{INL}	0	1.7	V	÷N + 1	1
Control input high current	I_{INH}		0.41	mA	V_{INH} = 8V	1
Control input low current	I_{INL}	-0.20		mA	V_{INL} = 0V	1
Clock to output delay	t_p		28	ns	C_L = 10pF	2
Set-up time	t_s	10		ns	C_L = 10pF	2
Release time	t_r	10		ns	C_L = 10pF	2

NOTES
1. Tested at 25°C only.
2. Guaranteed but not tested.



NOTE
The set-up time t_s is defined as the minimum time that can elapse between a L→H transition of the control input and the next L→H clock pulse transition to ensure that the ÷N mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H→L transition of the control input and the next L→H clock pulse transition to ensure that the ÷(N + 1) mode is obtained.

Fig.3 Timing diagram



*Tested as specified in table of Electrical Characteristics

Fig.4 Typical input characteristics

OPERATING NOTES

1. The inputs are biased internally and coupled to a signal source with suitable capacitors.
2. If no signal is present the devices will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from one input to pin 4 (ground). This will reduce the sensitivity.
3. The circuits will operate down to DC but slew rate must be better than 100V/µs.
4. The output stage is of an unusual design and is intended to interface with CMOS. External pull-up resistors or circuits must not be used.
5. This device is NOT suitable for driving TTL or its derivatives.

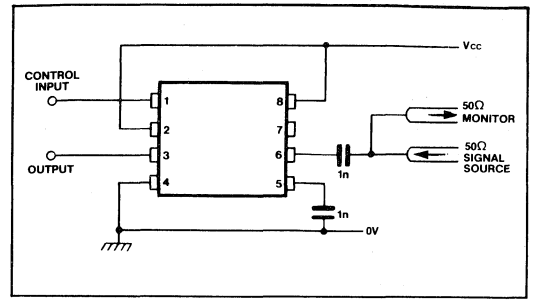


Fig.5 Toggle frequency test circuit

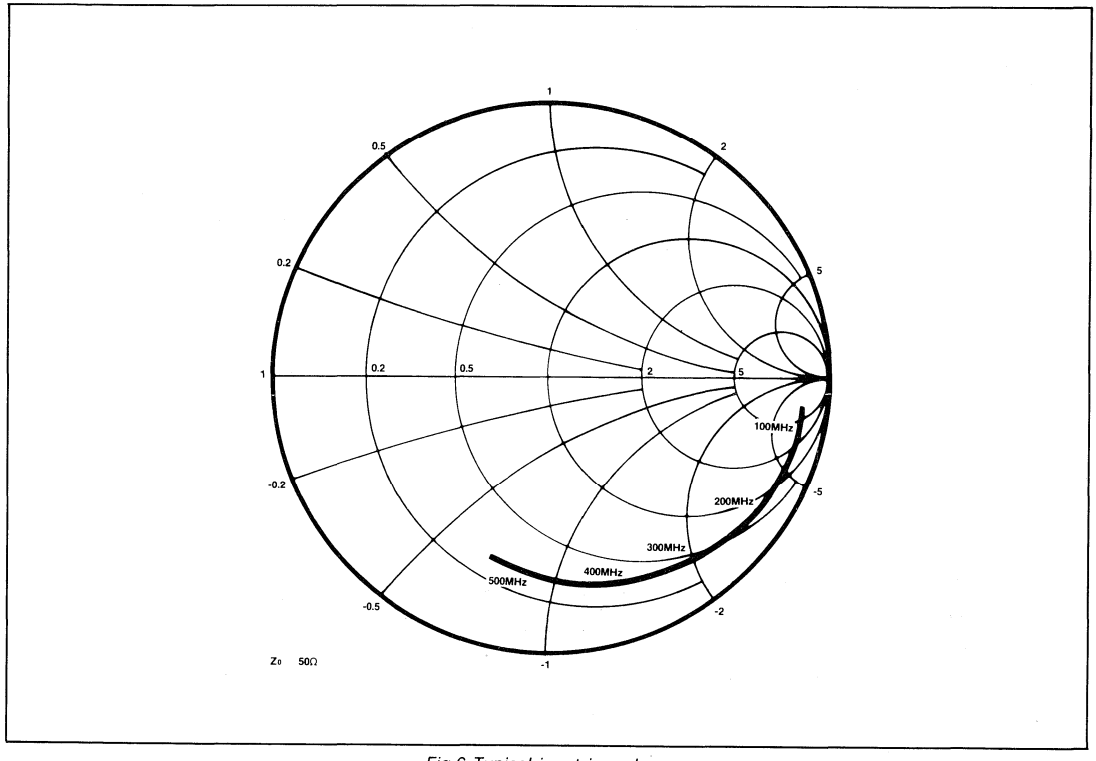


Fig.6 Typical input impedance

PLESSEY
Semiconductors

SP8789

225MHz ÷ 20/21 TWO MODULUS DIVIDER

The SP8789 is a low power programmable ÷20/21 counter.It divides by 20, when the control input is in the high state and by 21 when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

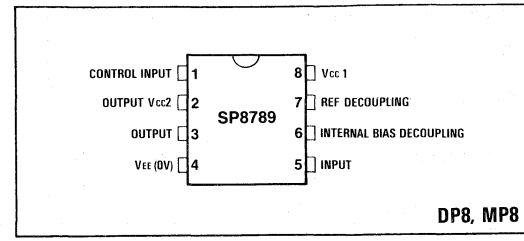


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

QUICK REFERENCE DATA

- Supply voltage: +5.2V or 6.8 to 9.5V
- Power consumption: 26mW Typical
- Temperature range: -40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6.0V pins 7 & 8 tied
Supply voltage	13.5V pin 8, pin 7 decoupled
Storage temperature range	-55°C to +125°C
Max. junction temperature	+175°C
Max. clock input voltage	2.5V p-p
V_{CC2}	Max. 10V

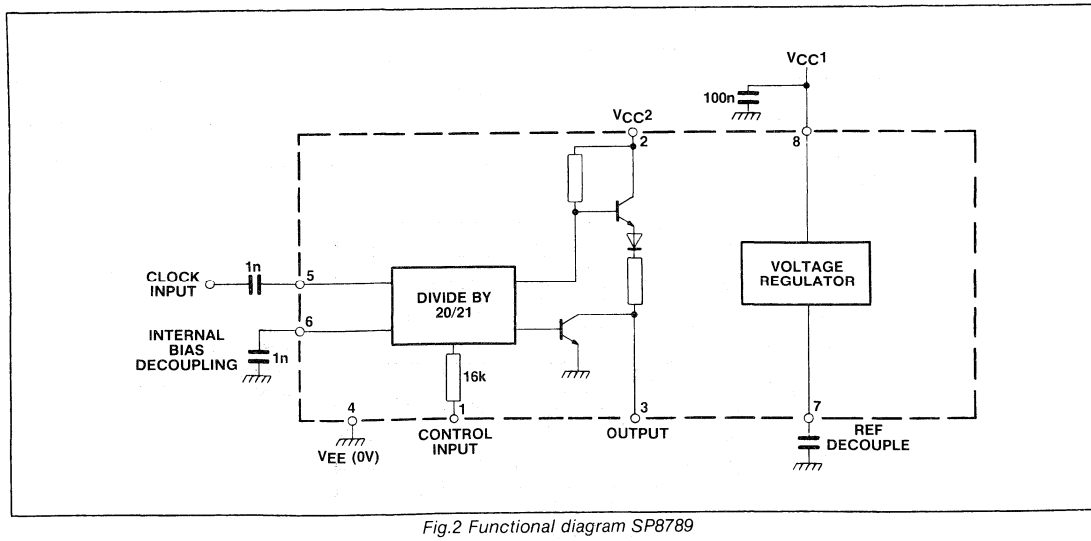


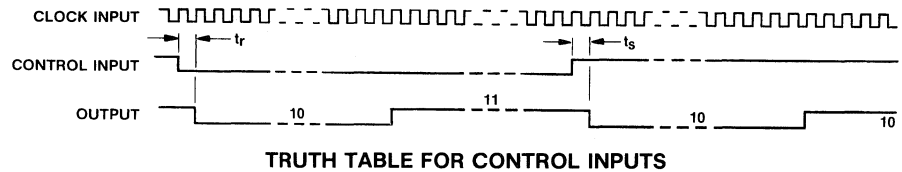
Fig.2 Functional diagram SP8789

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage: V_{CC} 1 & 2 = 5.2V ± 0.25V or 6.8V to 9.5V (see Operating Note 7);
V_{EE} = 0V; Temperature T_{amb} = -40°C to +85°C

Characteristic	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	225		MHz	Note 4	Input = 200-800mV p-p
Minimum frequency (sinewave input)	f_{min}		20	MHz	Note 4	Input = 400-800mV p-p
Power supply current	I_{EE}		7	mA	Note 4	
Control input high voltage	V_{INH}	4		V	Note 4	
Control input low voltage	V_{INL}		2	V	Note 4	
Output high voltage	V_{OH}	2.4		V	Note 4	Pins 2, 7 and 8 linked V_{CC} = 4.95V I_{OH} = 100μA
Output low voltage	V_{OL}		0.5	V	Note 4	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA
Set up time	t_s	14		ns	Note 3	25°C
Release time	t_r	20		ns	Note 3	25°C
Clock to output propagation time	t_p		45	ns	Note 3	25°C

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested only at 25°C.

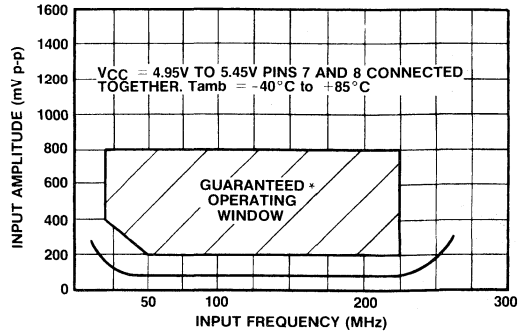


TRUTH TABLE FOR CONTROL INPUTS

Control input	Division ratio
0	21
1	20

Fig.3 Timing diagram SP8789

NOTES
The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and next L→H clock pulse transition to ensure ÷20 mode is selected.
The release time t_r is defined as minimum time that can elapse between H→L transition of the control input and the next L→H clock pulse transition to ensure the ÷21 mode is selected.



*Tested as specified in table of Electrical Characteristics

Fig.4 Input sensitivity SP8789

OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/μs is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The internal regulator has its input connected to Pin 8, while the internal reference voltage appears at Pin 7 and should be decoupled. For use from a 5.2V supply, Pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, Pins 7 and 8 should be separately decoupled, and the supply voltage applied to Pin 8.

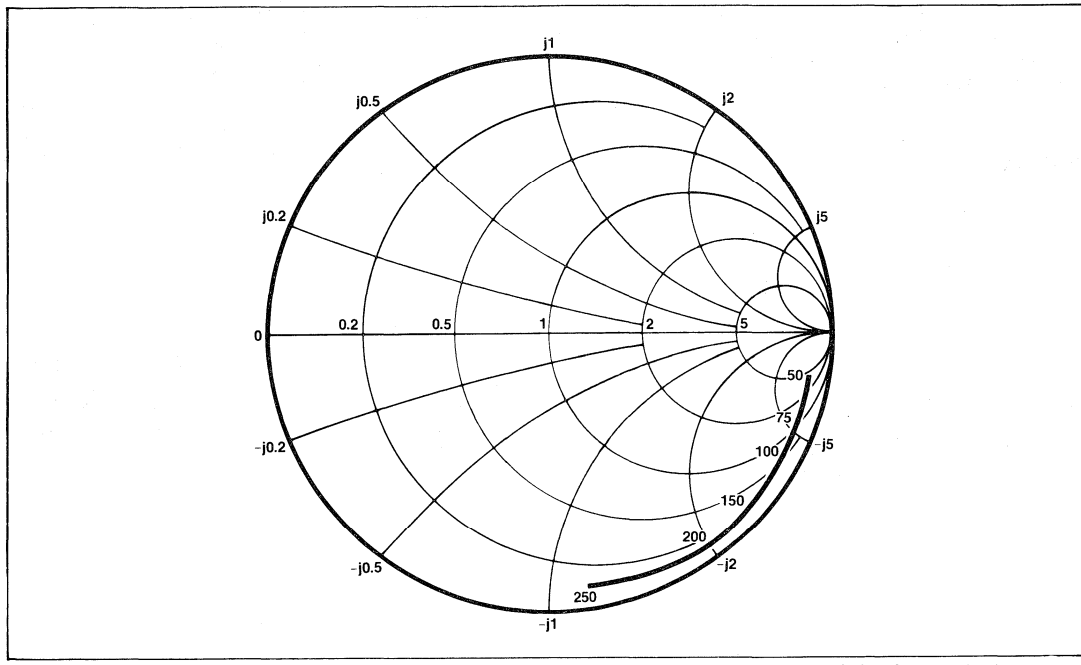


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

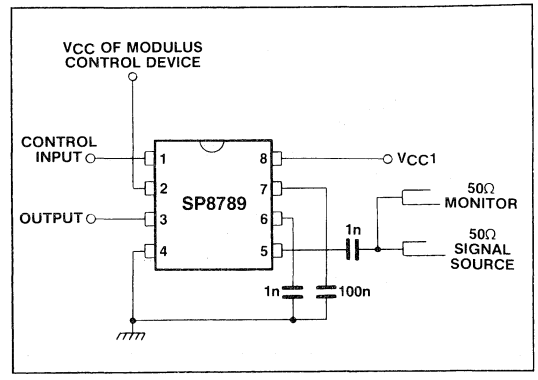


Fig.6 Toggle frequency test circuit

PLESSEY
Semiconductors

SP8792 225MHz ÷ 80/81
SP8793 225MHz ÷ 40/41

WITH ON-CHIP VOLTAGE REGULATOR

The SP8792 and SP8793 are low power programmable ÷80/81 and ÷40/41 counters, temperature range: -40°C to +85°C. They divide by 80(40) when control input is in the high state and by 81(41) when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

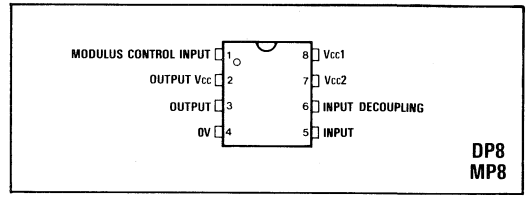


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

QUICK REFERENCE DATA

- Supply Voltage: +5.2V or 6.8V to 9.5V
- Power Consumption: 26mW

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6.0V pins 7 & 8 tied
Supply voltage	13.5V pin 8, pin 7 decoupled
Storage temperature range	-40°C to +85°C
Max. junction temperature	+175°C
Max. clock input voltage	2.5V p-p
Vcc2 max	10V

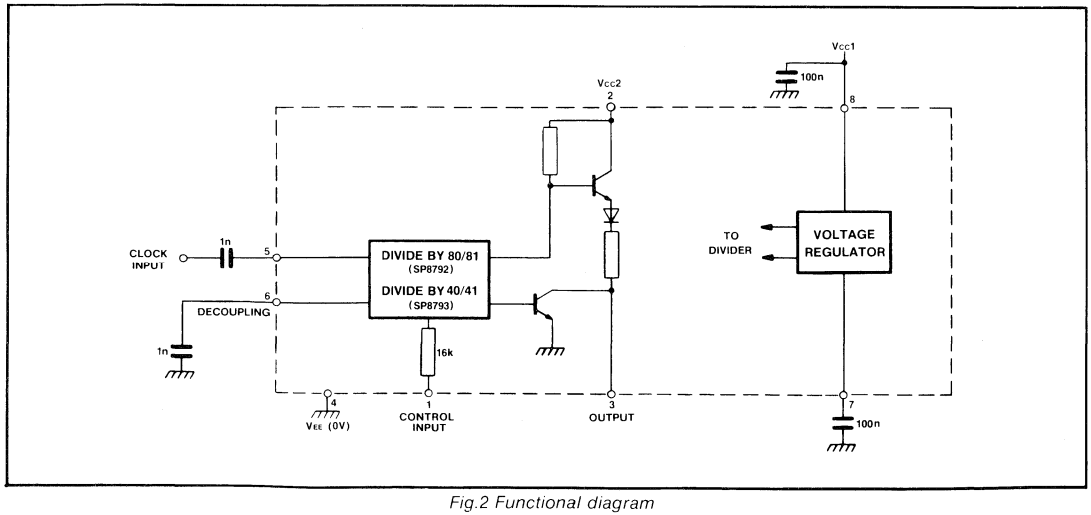


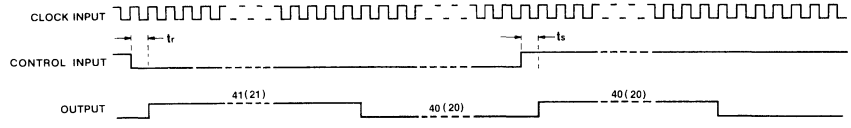
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 5.2V ± 0.25V or 6.8-9.5V (See Operating Note 6) V_{EE} = 0V
Temperature: T_{amb} = -40°C to +85°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	225		MHz	Input = 200-800mV p-p	Note 4
Minimum frequency (sinewave input)	f_{min}		20	MHz	Input = 400mV p-p	Note 4
Power supply current	I_{EE}		7	mA		Note 4
Control input high voltage	V_{INH}	4		V		Note 4
Control input low voltage	V_{INL}		2	V		Note 4
Output high voltage	V_{OH}	2.4		V	Pins 2,7 and 8 linked V_{CC} = 4.95V I_{OH} = 100µA	Note 4
Output low voltage	V_{OL}		0.5	V	Pin 2 open or linked to 8 and 7 I_{OL} = 1.6mA	Note 4
Set up time	t_s	14		ns	25°C	Note 3
Release time	t_r	20		ns	25°C	Note 3
Clock to output propagation time	t_p		45	ns	25°C	Note 3

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested at 25°C only.

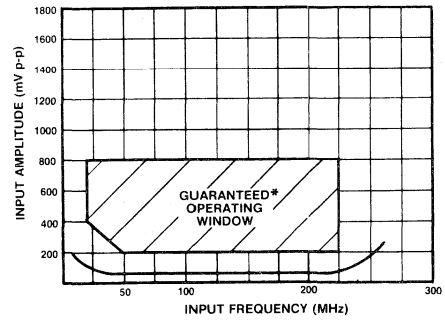


TRUTH TABLE FOR CONTROL INPUTS

Control Inputs	Division Ratio	
	SP8792	SP8793
0	81	41
1	80	40

Fig.3 Timing diagram SP8792/3

NOTES
The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure ÷80 or 40 mode is selected.
The release time t_r is defined as minimum time that can elapse between H→L transition of the control input and the next L→H clock pulse transition to ensure the ÷81 or 41 mode is selected.



*Tested as specified in table of Electrical Characteristics

Fig.4 Input sensitivity SP8792/SP8793

OPERATING NOTES

1. The clock input (pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, pin 6, to ground.
2. The output stage which is normally open collector (pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then pins 2 and 7 should be connected together to give a fan-out 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/μs is required.
4. The mark space ratio of output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig. 5.
6. The internal regulator has its input connected to pin 8, while the internal reference voltage appears at pin 7 and should be decoupled. For use from a 5.2V supply, pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, pins 7 and 8 should be separately decoupled, and the supply voltage applied to pin 8.
7. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.

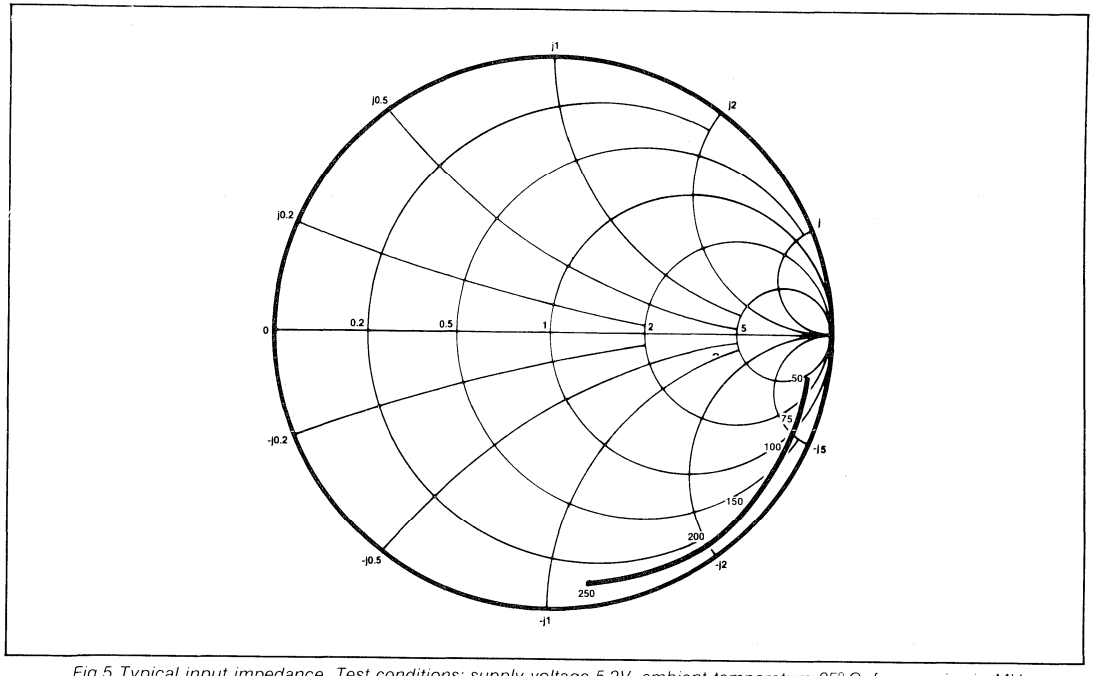


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

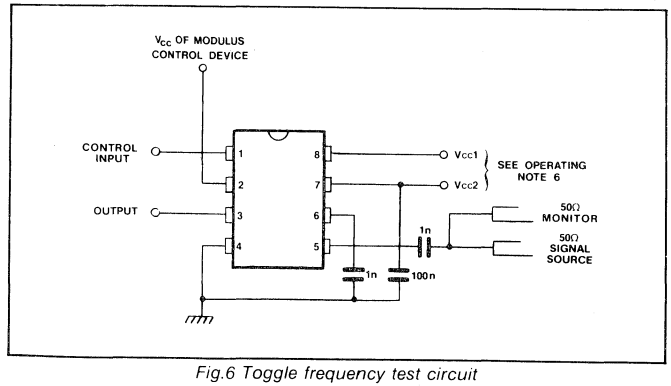


Fig.6 Toggle frequency test circuit

PLESSEY
Semiconductors

SP8795

225MHz ÷ 32/33 TWO MODULUS DIVIDER

The SP8795 is a low power programmable ÷32/33 counter.It divides by 32 when the control input is in the high state and by 33 when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

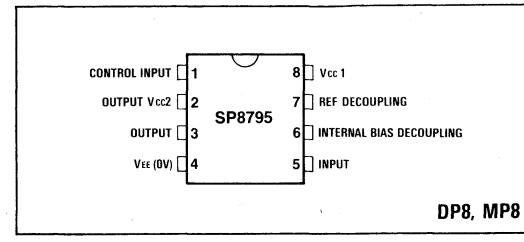


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

QUICK REFERENCE DATA

- Supply voltage: +5.2V or 6.8 to 9.5V
- Power consumption: 26mW Typical
- Temperature range: -40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6.0V Pins 7 & 8 tied
	13.5V Pin 8, Pin 7 decoupled
Storage temperature range	-55°C to +125°C
Max. junction temperature	+175°C
Max. clock input voltage	2.5V p-p
Vcc2	Max. 10V

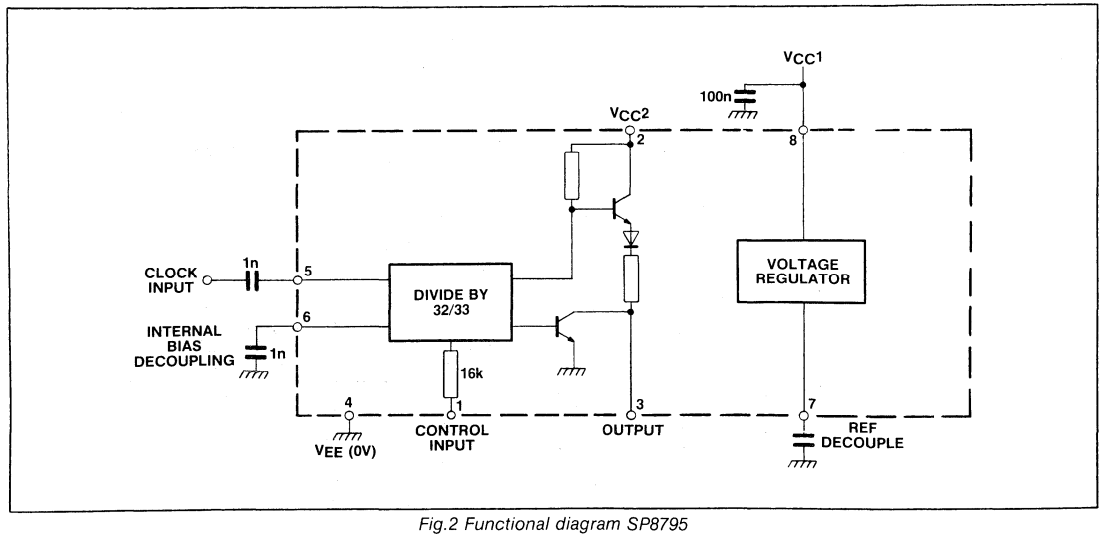


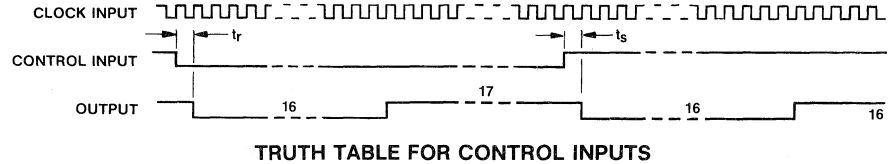
Fig.2 Functional diagram SP8795

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage: V_{CC} 1 & 2 = 5.2V ± 0.25V or 6.8V to 9.5V (see Operating Note 7);
V_{EE} = 0V; Temperature T_{amb} = -40°C to +85°C

Characteristic	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	225		MHz	Note 4	Input = 200-800mV p-p
Minimum frequency (sinewave input)	f_{min}		20	MHz	Note 4	Input = 400-800mV p-p
Power supply current	I_{EE}		7	mA	Note 4	
Control input high voltage	V_{INH}	4		V	Note 4	
Control input low voltage	V_{INL}		2	V	Note 4	
Output high voltage	V_{OH}	2.4		V	Note 4	Pins 2, 7 and 8 linked V_{CC} = 4.95V I_{OH} = 100μA
Output low voltage	V_{OL}		0.5	V	Note 4	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA
Set up time	t_s	14		ns	Note 3	25°C
Release time	t_r	20		ns	Note 3	25°C
Clock to output propagation time	t_p		45	ns	Note 3	25°C

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested only at 25°C.

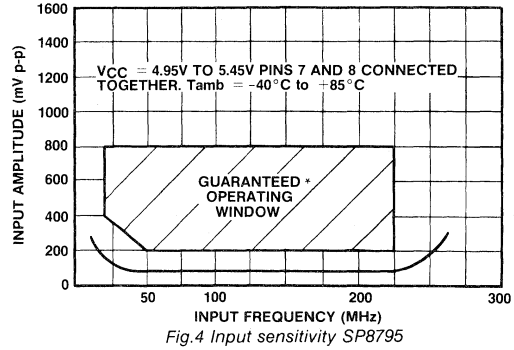


TRUTH TABLE FOR CONTROL INPUTS

Control input	Division ratio
0	33
1	32

Fig.3 Timing diagram SP8795

NOTES
The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and next L→H clock pulse transition to ensure ÷32 mode is selected.
The release time t_r is defined as minimum time that can elapse between H→L transition of the control input and the next L→H clock pulse transition to ensure the ÷33 mode is selected.



*Tested as specified in table of Electrical Characteristics

Fig.4 Input sensitivity SP8795

OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/μs is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The internal regulator has its input connected to Pin 8, while the internal reference voltage appears at Pin 7 and should be decoupled. For use from a 5.2V supply, Pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, Pins 7 and 8 should be separately decoupled, and the supply voltage applied to Pin 8.

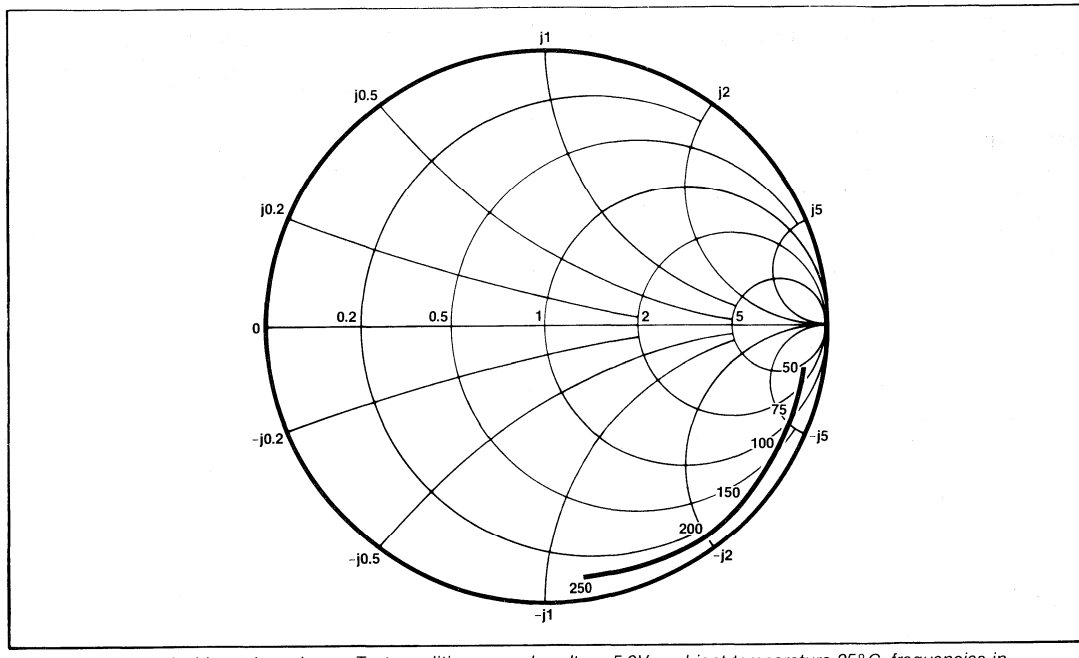


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

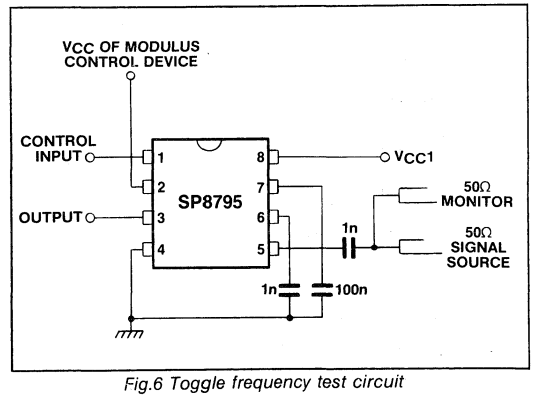


Fig.6 Toggle frequency test circuit

SP8797

225MHz ÷ 32/33 PRESCALER

The SP8797 is a low power programmable ÷32/33 counter. It divides by 32 when the control input is in the high state and by 33 when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

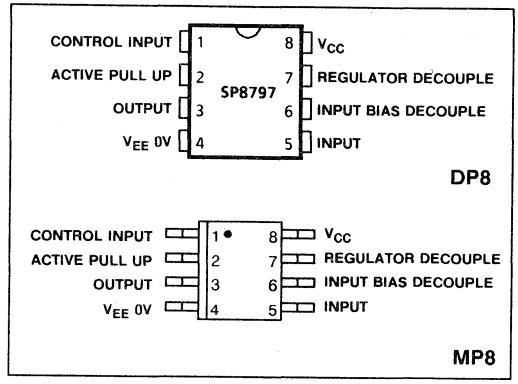


Fig 1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS and TTL Compatible
- AC Coupled Input
- Operation up to 9.5V Using Internal Regulator
- Buffer Amp for Good Reverse Isolation

QUICK REFERENCE DATA

- Supply voltage: 4.5V to 9.5V
- Power consumption 65mW at V_{CC} = 9.5V
- Temperature range: -40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage pin 7	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C
Supply Voltage pin8	13.5V

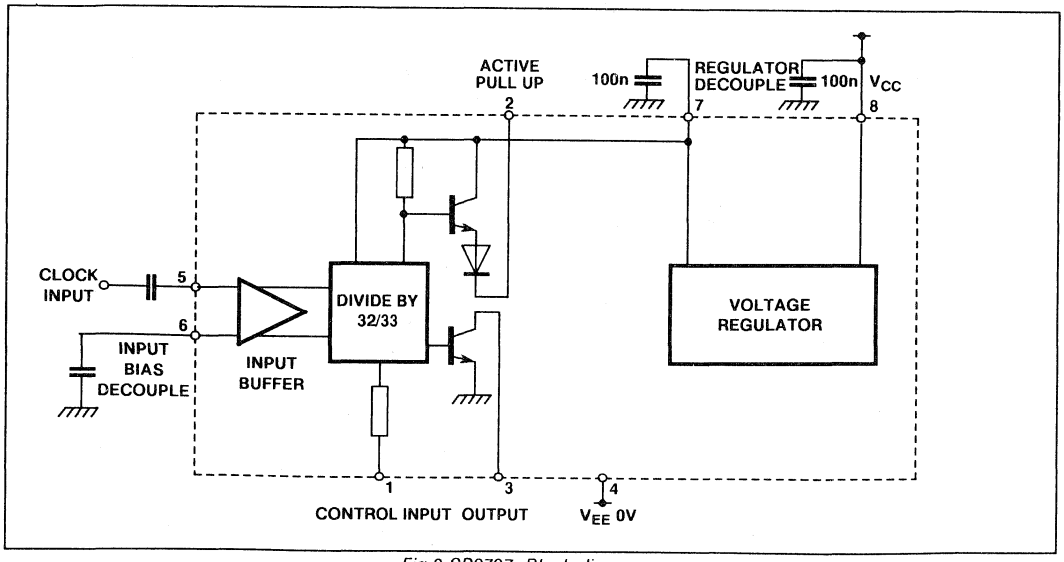
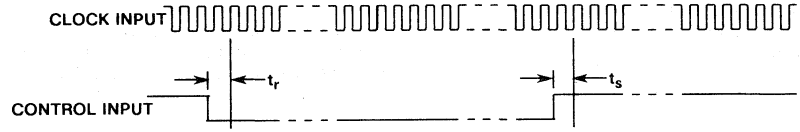


Fig 2 SP8797 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{CC} = +4.5V to +5.5V or Vreg = 6.5V to 9.5V Tamb = -40°C to +85°C

Characteristic	Sym	Value		Units	Conditions
		Min.	Max.		
Supply current	I_{CC}		7.8	mA	
Maximum frequency (sinewave input)	f_{MAX}	225		MHz	Input = 200mV to 800mV p-p
Minimum frequency (sinewave input)	f_{MIN}		20	MHz	Input = 200mV to 800mV p-p
Control input high voltage	V_{INH}	2	5.5	V	Pin 7 Voltage = 5.5V
Control input low voltage	V_{INL}	0	0.8	V	
Output high voltage	V_{OH}	2.5		V	Pin 2 connected to pin 3 V_{CC} = 4.5V I_{OH} = 100µA
Output low voltage	V_{OL}		0.5	V	Pin 2 connected to pin 3 IOL = 1.6mA
Set up time	t_s	14		ns	25°C
Release time	t_r	20		ns	25°C
Clock to output propagation time	t_p		45	ns	25°C



CONTROL INPUT	DIVISION RATIO
0	33
1	32

TRUTH TABLE FOR CONTROL INPUTS

Fig.3 Timing diagram SP8797

NOTES

1. The set up time t_s is defined as the minimum time that can elapse between the LOW to HIGH transition of control input and the next LOW to HIGH clock pulse transition to ensure ÷32 mode is selected.
2. The release time t_r is defined as the minimum time that can elapse between the HIGH to LOW transition of the control input and the next LOW to HIGH clock pulse transition to ensure ÷33 mode is selected.

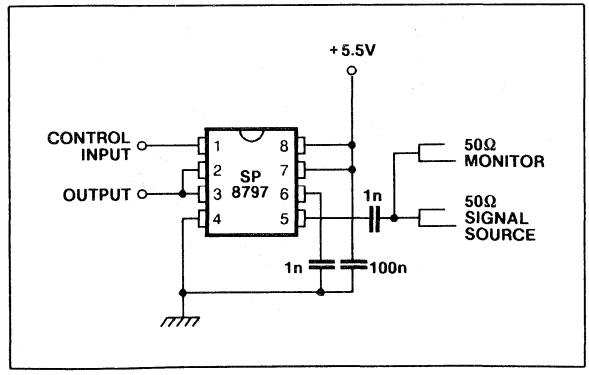


Fig.4 Toggle frequency test circuit

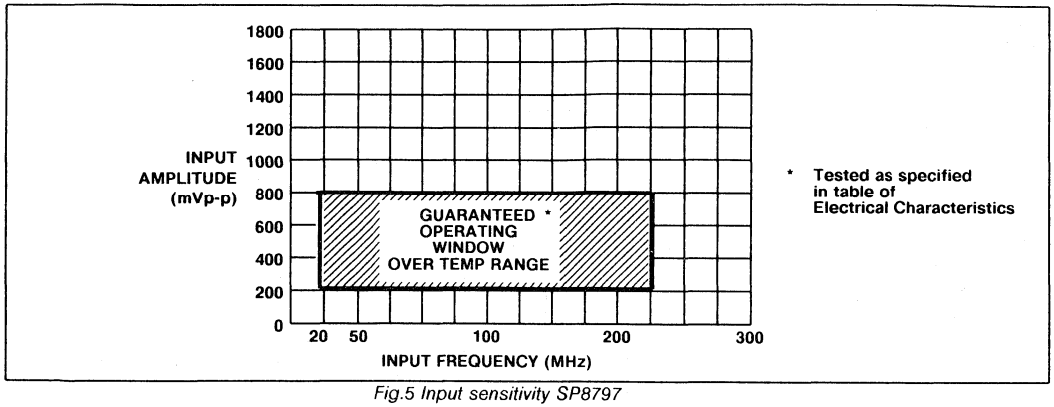


Fig.5 Input sensitivity SP8797

OPERATING NOTES

1. The clock input (pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output on pin 3 is an open collector and can be interfaced to CMOS by connecting a pull up resistor to a positive supply of up to +9.5V. The sink current through this resistor should not exceed 2mA. When an interface to TTL is required, the active pull up on pin 2 should be connected to pin 3, giving a fan out of 1. The supply current will be increased by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/µs is required on the clock input.
4. The mark to space ratio at the output is approximately 1.2:1 at 225 MHz.
5. Input impedance is a function of frequency. See Fig.6.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 680K resistor between the unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.

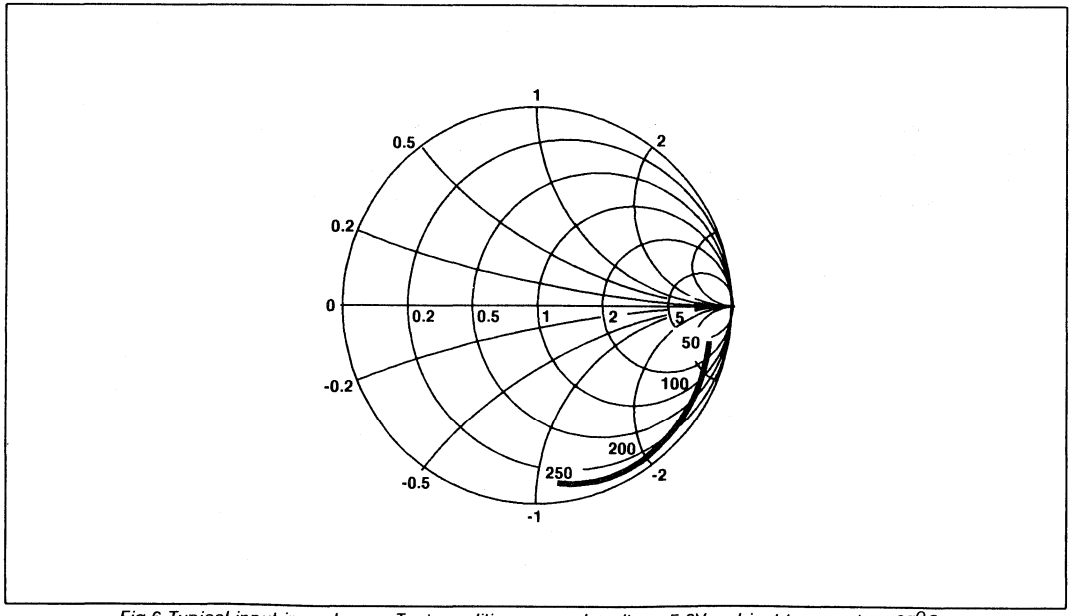


Fig.6 Typical input impedance. Test conditions: supply voltage 5.0V,ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

PLESSEY
Semiconductors

SP8799

225MHz ÷ 10/11 TWO MODULUS DIVIDER

The SP8799 is a low power programmable ÷10/11 counter.It divides by 10 when the control input is in the high state and by 11 when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

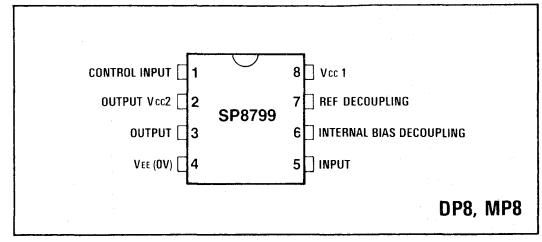


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

QUICK REFERENCE DATA

- Supply voltage: +5.2V or 6.8 to 9.5V
- Power consumption: 26mW Typical
- Temperature range: -40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6.0V Pins 7 & 8 tied
	13.5V Pin 8, Pin 7 decoupled
Storage temperature range	-55°C to +125°C
Max. junction temperature	+175°C
Max. clock input voltage	2.5V p-p
Vcc2	Max. 10V

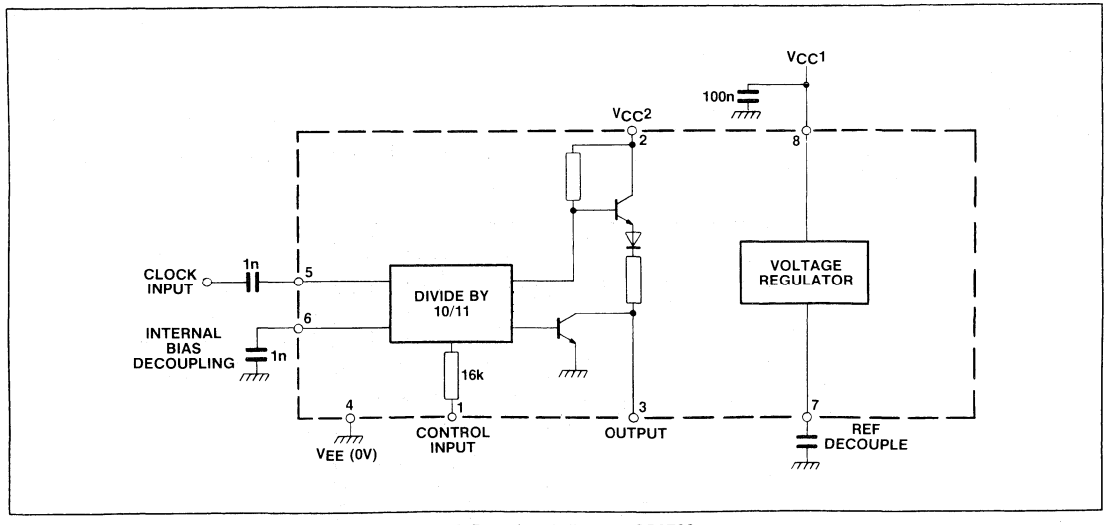


Fig.2 Functional diagram SP8799

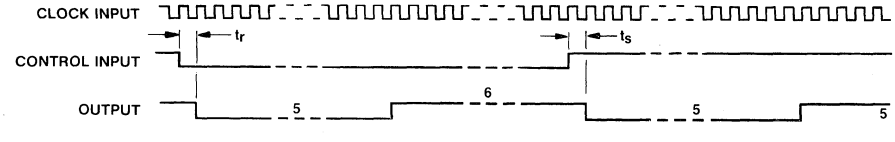
ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage: V_{CC} 1 & 2 = 5.2V ± 0.25V or 6.8V to 9.5V (see Operating Note 7);
V_{EE} = 0V; Temperature T_{amb} = -40°C to +85°C

Characteristic	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	225		MHz	Note 4	Input = 200-800mV p-p
Minimum frequency (sinewave input)	f_{min}		20	MHz	Note 4	Input = 400-800mV p-p
Power supply current	I_{EE}		7	mA	Note 4	
Control input high voltage	V_{INH}	4		V	Note 4	
Control input low voltage	V_{INL}		2	V	Note 4	
Output high voltage	V_{OH}	2.4		V	Note 4	Pins 2, 7 and 8 linked V_{CC} = 4.95V I_{OH} = 100μA
Output low voltage	V_{OL}		0.5	V	Note 4	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA
Set up time	t_s	14		ns	Note 3	25°C
Release time	t_r	20		ns	Note 3	25°C
Clock to output propagation time	t_p		45	ns	Note 3	25°C

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested only at 25°C.



TRUTH TABLE FOR CONTROL INPUTS

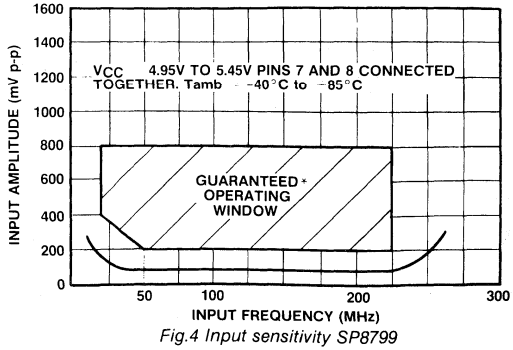
Control input	Division ratio
0	11
1	10

Fig.3 Timing diagram SP8799

NOTES

The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and next L→H clock pulse transition to ensure ÷10 mode is selected.

The release time t_r is defined as minimum time that can elapse between H→L transition of the control input and the next L→H clock pulse transition to ensure the ÷11 mode is selected.



*Tested as specified in table of Electrical Characteristics

Fig.4 Input sensitivity SP8799

OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/μs is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The internal regulator has its input connected to Pin 8, while the internal reference voltage appears at Pin 7 and should be decoupled. For use from a 5.2V supply, Pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, Pins 7 and 8 should be separately decoupled, and the supply voltage applied to Pin 8.

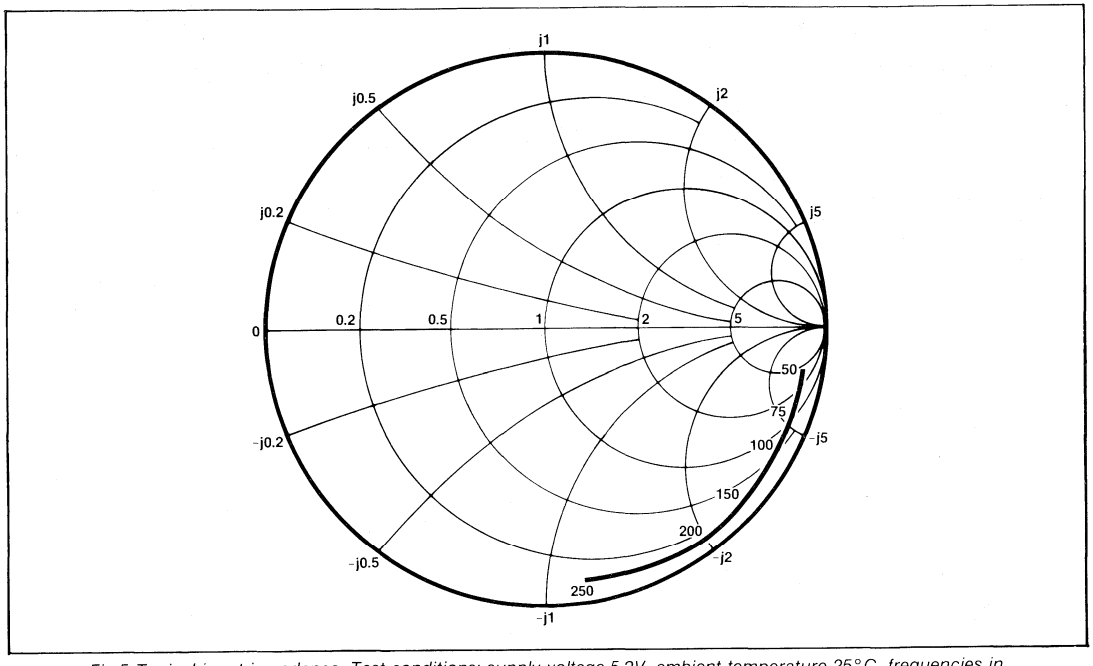


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

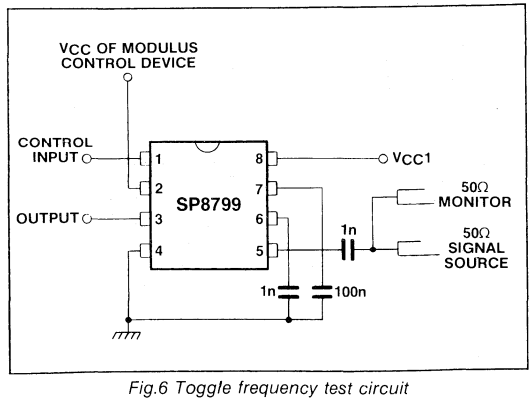


Fig.6 Toggle frequency test circuit

PLESSEY
Semiconductors

NJ8820, NJ8820B

FREQUENCY SYNTHESISER (PROM INTERFACE)

The NJ8820/NJ8820B is a synthesiser circuit fabricated on the Plessey 5-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words read from an external memory with the necessary timing signals generated internally.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

The NJ8820 is available in Plastic DIL (DP) and Miniature Plastic DIL (MP) packages, both with operating temperature range of -30°C to +70°C. The NJ8820B is available only in Ceramic DIL package with operating temperature range of -40°C to +85°C.

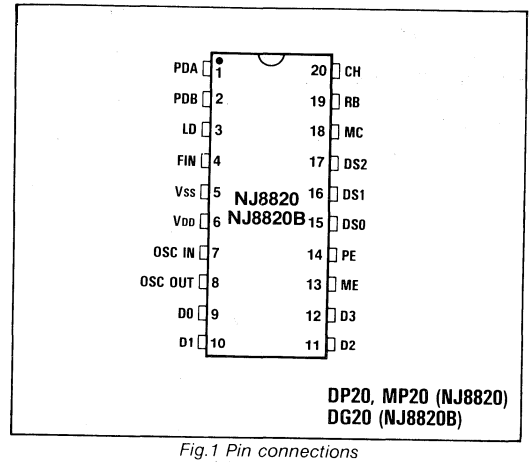


Fig.1 Pin connections

FEATURES

- Low Power Consumption
- Direct Interface to ROM or PROM
- High Performance Sample and Hold Phase Detector
- >10MHz Input Frequency

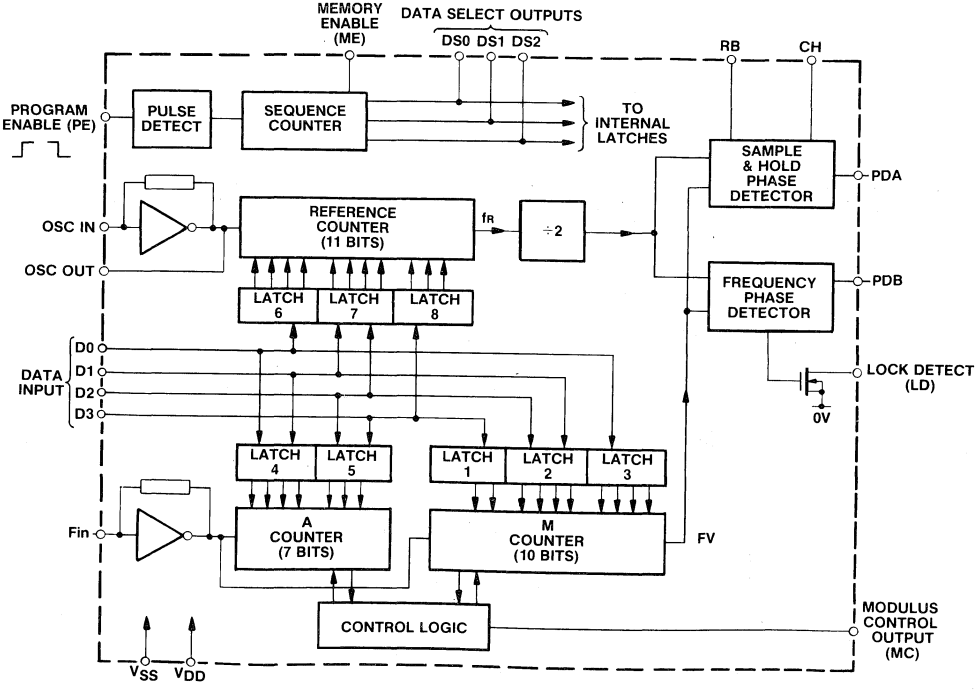


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{DD}-V_{SS} 5V ± 0.5V, Temperature range NJ8820: -30°C to +70°C, NJ8820B: -40°C to +85°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.5	5.5	mA	FOSC, FIN = 10MHz } 0 to 5V square wave
		0.7	1.5	mA	FOSC, FIN = 1.0MHz }
OUTPUT LEVELS					
ME output					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
DS OUTPUTS					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 2mA
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB Output					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	
INPUT LEVELS					
Data Inputs					
High level	4.25			V	TTL compatible
Low level			0.75	V	See note 1
Program Enable Input (PE)					
Trigger level	V_{bias} ±100mV			V	V_{bias} = self bias point of PE (nominally V_{DD}/2)

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10.6			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS} Note 5
Propagation delay, clock to modulus control		30	50	ns	Note 2
Program enable pulse length, t_w	5			μs	Pulse to V_{SS} or V_{DD}
Data set-up time, t_{SI}	1			μs	
Data hold time, t_{HI}	10			ns	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See Fig.7
Hold capacitor, CH			1	nF	Note 3
Output resistance PDA			5	kΩ	
Digital phase detector gain		1		V/Rad	
Power supply rise time	100			μs	10 % to 90 %. Note 4

NOTES

1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs. 2. All counters have outputs directly synchronous with their respective clock rising edges. 3. Finite output resistance of internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds. 4. To ensure correct operation of power-on programming. 5. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESIGNATION

Pin No.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. **Output at (V_{DD}-V_{SS})/2 when in lock.** Voltage increases as FV phase lead increases and decreases as FR phase lead increases. Output is linear over only a narrow phase window determined by gain programmed by RB.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses FV < FR or FR leading: negative pulses FV = FR and phase error within PDA window: high impedance
3	LD	An open drain lock detect output at low level when phase error within PDA window (in lock). High impedance at all other times.
4	FIN	The input to the main counters normally driven from a prescaler which may be AC coupled or when a full logic swing is available may be DC coupled.
5	V_{SS}	Negative supply (normally ground)
6	V_{DD}	Positive supply
7,8	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal-generated reference signal may alternatively be applied to OSC.IN. This may be a low-level signal AC coupled into OSC.IN or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 6-4094 in steps of 2, with the division ratio being twice the programmed number.
9,10,11,12	D0-D3	Information on these inputs is transferred to the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
13	ME	An open-drain output for use in controlling the power supply to an external ROM or PROM. This output is low during the data read period and high impedance at other times.
14	PE	A positive or negative pulse or edge AC coupled into this pin initiates the single-shot data read procedure. Grounding this pin repeats the data read procedure in a cyclic manner.
15,16,17	DS0-DS2	Internally generated three-state data select outputs which may be used to address external memory.
18	MC	Signal for controlling an external dual-modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N +A where N and N +1 represent the dual modulus prescale values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The program range of the 'M' counter is 3-1023 and for correct program operation M ≥A. Where every possible channel is required, the minimum division ratio should be N^2-N.
19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
20	CH	An external hold capacitor should be connected between this pin and V_{SS}.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD} - V_{SS})	-0.5V to 7V
Input voltage	
Open drain O/Ps (pins 3 and 13)	7V
All other pins	V_{SS} -0.3V to V_{DD} +0.3V
Storage temperature	-65°C to +150°C (DG package, NJ8820B)
Storage temperature	-55°C to +125°C (DP and MP packages, NJ8820)

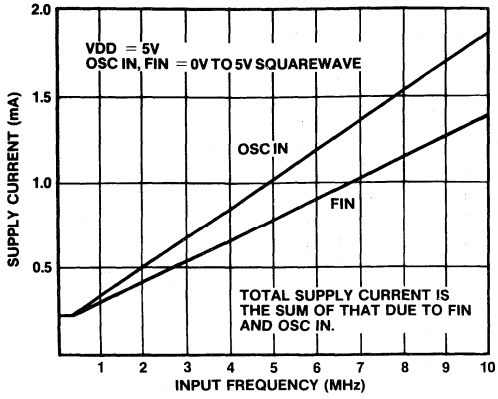


Fig.3 Typical supply current versus input frequency

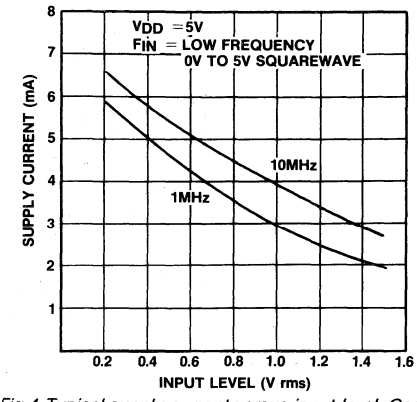


Fig.4 Typical supply current versus input level, Osc In

PROGRAMMING

Program information can be obtained from an external ROM or PROM under control of the NJ8820/NJ8820B. Twenty-eight data bits are required per channel arranged as eight 4-bit words leaving four redundant bits, two of which are available on the data bus driving the data-transfer time slot and may be used for external control purposes. A suitable PROM may be the 74S287 giving up to 32 channel capability as shown in Fig.5. Note that the choice of PNP transistor and supply bypass capacitor on the ROM should be such that the ROM will power up in time: for example, at 10MHz oscillator frequency, the ROM must be powered up in less than 25μs.

Reading of this data is normally done in a single shot mode with the data read cycle started by either a positive or negative pulse on the program enable pin. The data read cycle is generated from a program clock at 1/64th of the reference oscillator frequency. A memory enable signal is supplied to allow power-down of the memory when not in use. Data select outputs remain in a high-impedance state when the program cycle is completed to allow the address bus to be used for other functions if desired. The data map, data read cycle and timing diagram appears as Figs. 6 to 8. Data is latched internally during the shaded portions of the program cycle and all data is transferred to the counters and latched during the data transfer time slot.

Alternatively, the PE pin may be grounded causing the data read cycle to repeat in a cyclic manner to allow continuous up-dating of the program information. In this mode external memory will be enabled continuously, (ME low) and the data read cycle will repeat every sixteen cycles of the internal program clock, i.e. every 1024/fosc seconds. This programming method is not recommended because the higher power consumption and the possibilities of noise injection into the loop from the digital data lines.

Power-on programming On power-up the data read cycle is automatically initiated making it unnecessary to provide a PE pulse on power-up. The circuit detects the power supply rising above a threshold point, (nominally 1.5V) and after an internally generated delay to allow the supply to rise fully the circuit is programmed in the normal way. This delay is generated by counting reference oscillator pulses and is therefore dependent on the crystal used. The delay consists of 53248 reference oscillator cycles giving a delay of about 5ms at 10MHz.

To ensure correct operation of this function the power supply rise time should be less than 5ms, (at 10MHz) rising smoothly through the threshold point.

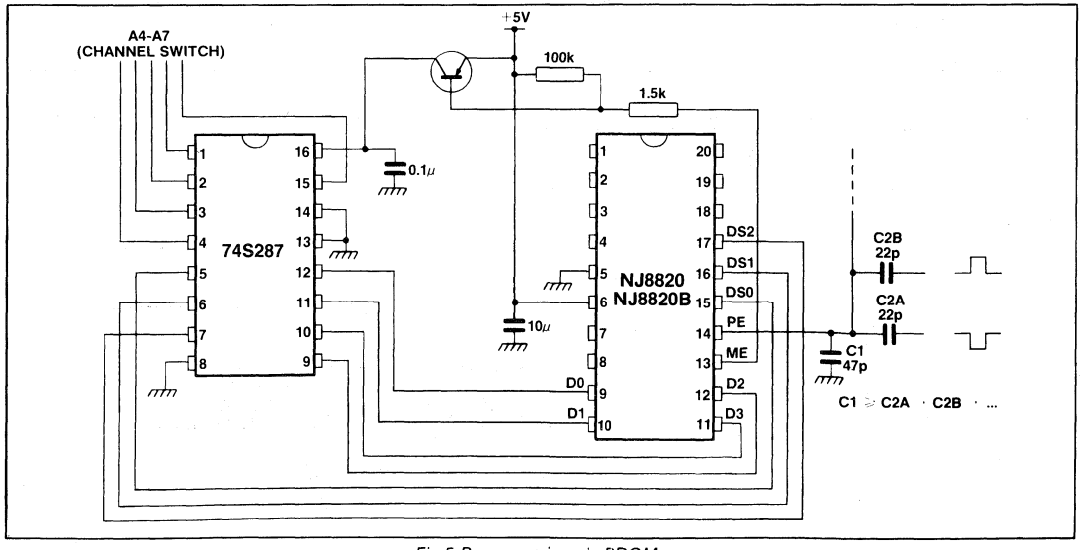


Fig.5 Programming via PROM

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig.6 Data map

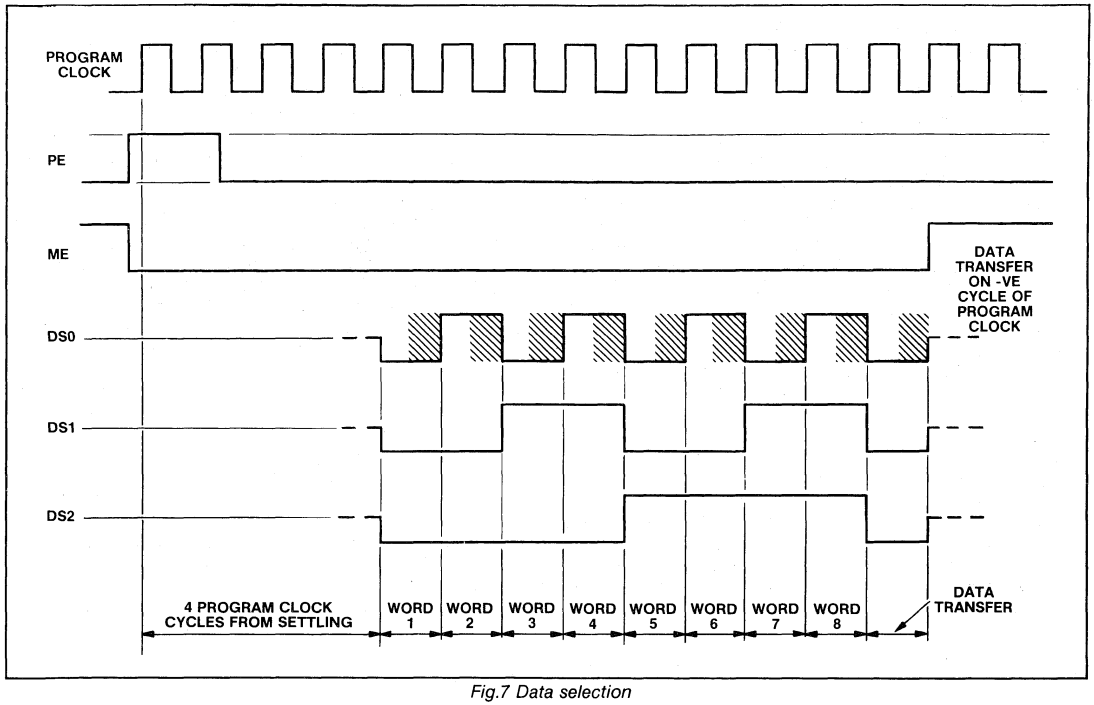


Fig.7 Data selection

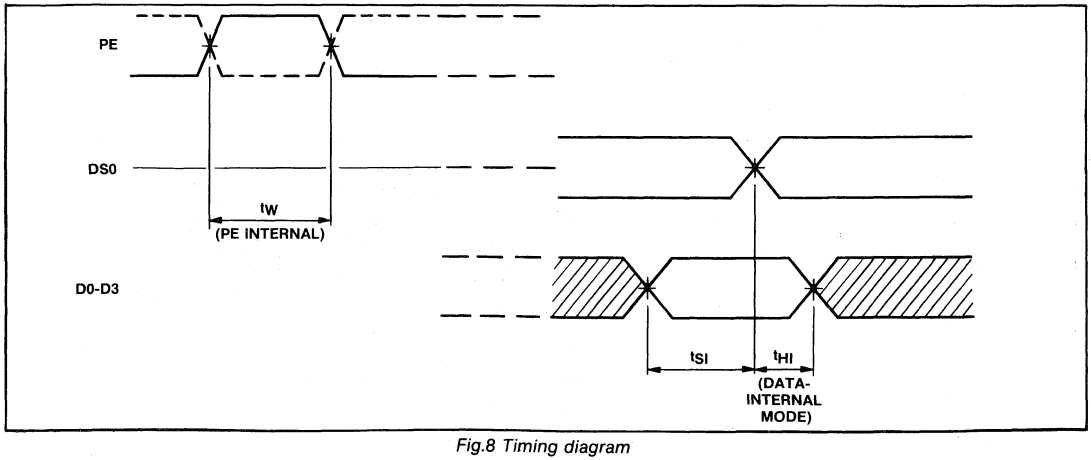


Fig.8 Timing diagram

PHASE COMPARATORS

A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels. This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

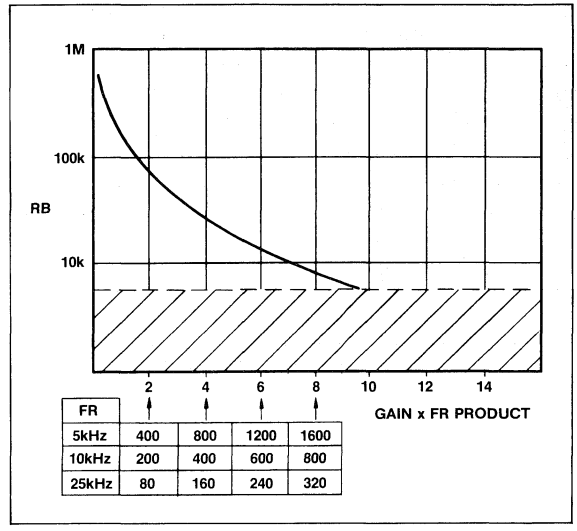
An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at (V_{DD}-V_{SS})/2 and any offset from this would be proportional to phase error. The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}\text{-}V_{SS}\text{-}0.7\text{-}89(RB^{-\frac{1}{2}})]}{2 \times \pi\ 50\times10^{-12} \times RB \times FR}$$

The value of RB should be chosen to give the required gain at the reference frequency used. Fig.9 for example shows that to achieve a gain of 380V per radian at 10kHz requires approximately 39kΩ. A second external component is required; this is a hold capacitor of non-critical value which might typically be 470pF, a smaller value being sufficient if the sideband performance required is not high. Fig.9 shows the gain normalised to a 1Hz comparison frequency; to obtain the value for any other frequency, divide the value of gain frequency product by the desired frequency.

The output from these phase detectors should be combined and filtered to generate a single control voltage to drive the VCO as in Fig.8.



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320

Fig.9 RB versus gain and reference frequency

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

APPLICATION EXAMPLE

An application example for a synthesiser for operation up to 520MHz is given in Fig.10. This gives up to 32 channels with a maximum supply current of 17mA, (typically 12mA) at 520MHz excluding the VCO. With careful construction the circuit is capable of providing sideband attenuation in excess of 90dB with lock-times of only a few milliseconds for a 1MHz frequency step.

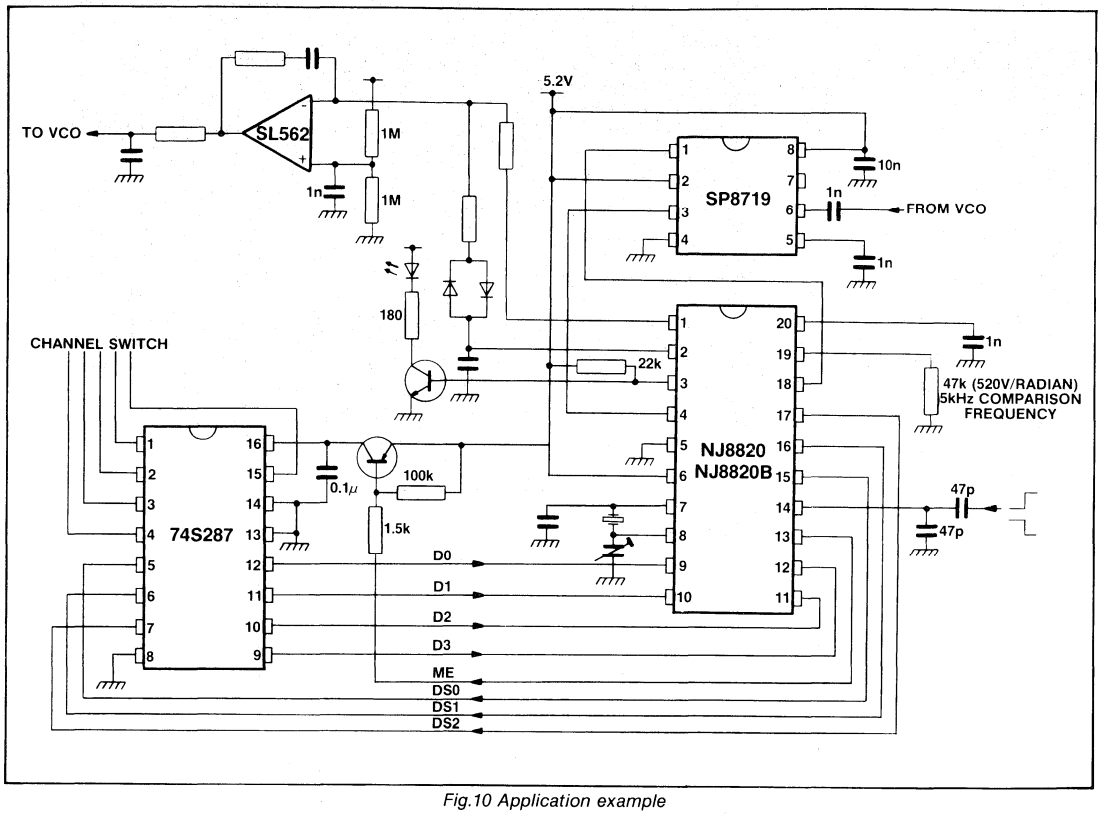


Fig.10 Application example

PLESSEY
Semiconductors

NJ8820GG

FREQUENCY SYNTHESISER (PROM INTERFACE)

The NJ8820GG is a synthesiser circuit fabricated with the 2-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words in one of two modes. Data may be read from an external memory with the necessary timing signals generated internally.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

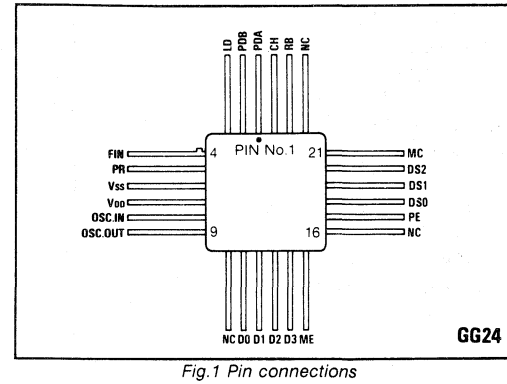


Fig.1 Pin connections

FEATURES

- Low Power Consumption
- Direct Interface to ROM or PROM
- High Performance Sample and Hold Phase Detector
- Microprocessor Compatible
- > 10MHz Input Frequency

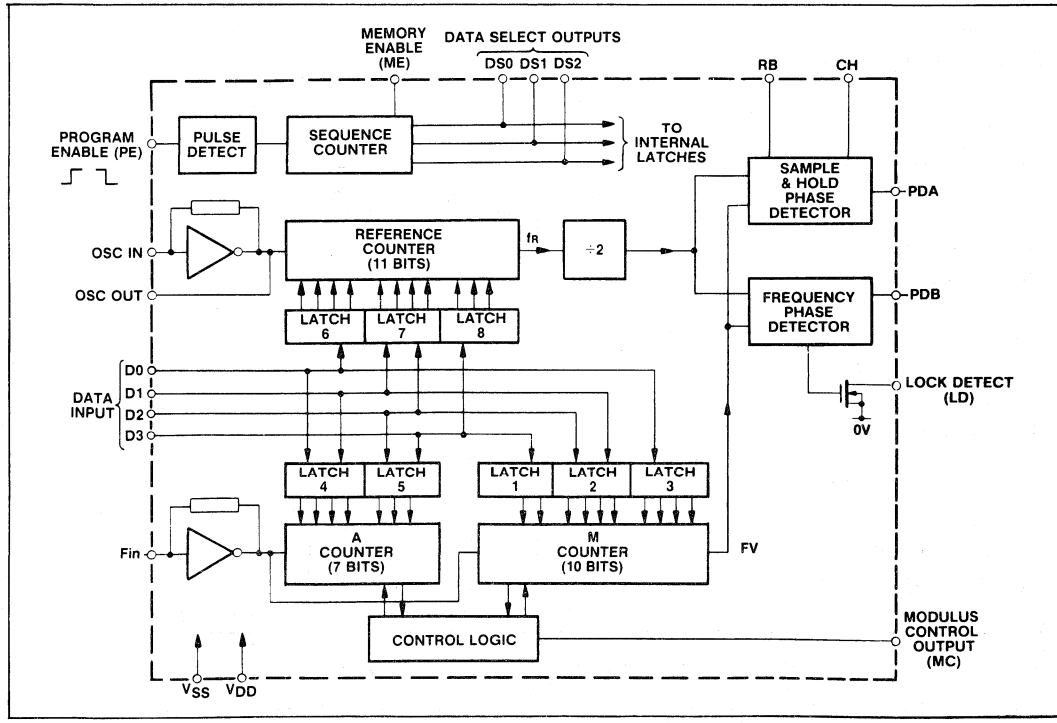


Fig.2 Block diagram

NJ8820GG

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD}-V_{SS} 5V ± 0.5V Temperature range -30° C to +70° C

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.5	5.5	mA	FOSC, FIN = 10MHz } 0 to 5V
		0.7	1.5	mA	FOSC, FIN = 1.0MHz } square wave
OUTPUT LEVELS					
ME output					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
DS OUTPUTS					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 2mA
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB Output					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	
INPUT LEVELS					
Data Inputs					
High level	4.25			V	TTL compatible
Low level			0.75	V	See note 1
Program Enable input (PE)					
Trigger level	V_{bias} ±100mV			V	V_{bias} = self bias point of PE (nominally V_{DD}/2)

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10.6			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS} Note 5
Propagation delay, clock to modulus control		30	50	ns	Note 2
Program enable pulse length, t_w	5			μs	Pulse to V_{SS} or V_{DD}
Data set-up time, t_{SI}	1			μs	
Data hold time, t_{HI}	10			ns	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See Fig.7
Hold capacitor, CH			1	nF	Note 3
Output resistance PDA			5	kΩ	
Digital phase detector gain		1		V/Rad	
Power supply rise time	100			μs	10 % to 90 %. Note 4

NOTES
1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. Finite output resistance of internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds.
4. To ensure correct operation of power-on programming.
5. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESIGNATION

Pin No.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. **Output at (V_{DD}-V_{SS})/2 when in lock.** Voltage increases as FV phase lead increases and decreases as FR phase lead increases. Output is linear over only a narrow phase window determined by gain programmed by RB.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses FV < FR or FR leading: negative pulses FV = FR and phase error within PDA window: high impedance
3	LD	An open drain lock detect output at low level when phase error within PDA window (in lock). High impedance at all other times.
4	FIN	The input to the main counters normally driven from a prescaler which may be AC coupled or when a full logic swing is available may be DC coupled.
5	PR	This pin allows selection between programming modes. For internal control the pin should be left open circuit and should be grounded to allow external control.
6	V_{SS}	Negative supply (normally ground)
7	V_{DD}	Positive supply
8,9	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal-generated reference signal may alternatively be applied to OSC.IN. This may be a low-level signal AC coupled into OSC.IN or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 6-4094 in steps of 2, with the division ratio being twice the programmed number.
11,12,13,14	D0-D3	Information on these inputs is transferred to the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
15	ME	An open-drain output for use in controlling the power supply to an external ROM or PROM. This output is low during the data read period and high impedance at other times.
17	PE	This pin has two functions. In internal mode a positive or negative pulse AC coupled into this pin initiates the single-shot data read procedure. Grounding this pin repeats the data read procedure in a cyclic manner. In external mode this pin is used as a strobe for the data. A logic high on this pin transfers data from the data pins to the internal latch selected by the address, (data select) lines, while a logic zero disables the data lines.
18,19,20	DS0-DS2	Internally generated three-state data select outputs which may be used to address external memory. In external mode these pins became inputs to control the addressing of data latches.
21	MC	Signal for controlling an external dual-modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N +A where N and N +1 represent the dual modulus prescale values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The program range of the 'M' counter is 3-1023 and for correct program operation M ≥A. Where every possible channel is required, the minimum division ratio should be N^2-N.
23	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
24	CH	An external hold capacitor should be connected between this pin and V_{SS}.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD}-V_{SS}): -0.5V to 7V
Input voltage at any pin * V_{SS} -0.3V to V_{DD} +0.3V

Storage temperature: -65°C to +150°C

*Except on open drain outputs where this is 7V.

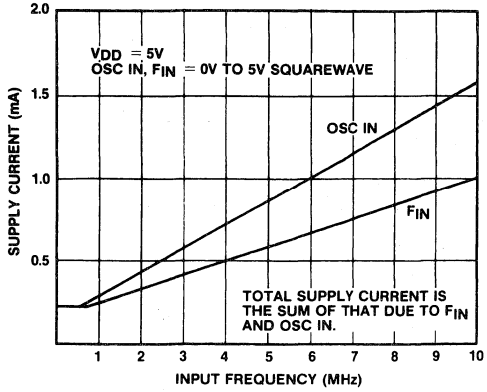


Fig.3 Typical supply current versus input frequency

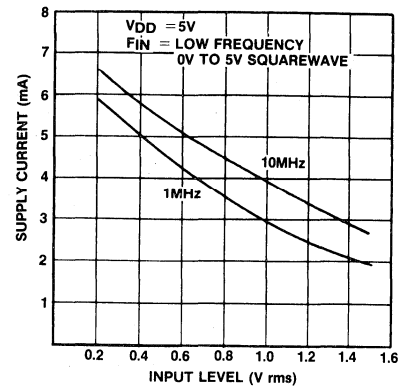


Fig.4 Typical supply current versus input level, Osc In

PROGRAMMING IN INTERNAL MODE

This mode of operation allows program information to be obtained from an external ROM or PROM under control of the NJ8820GG. Twenty-eight data bits are required per channel arranged as eight 4-bit words leaving four redundant bits, two of which are available on the data bus driving the data-transfer time slot and may be used for external control purposes. A suitable PROM may be the 74S287 giving up to 32 channel capability. Note that the choice of PNP transistor and supply bypass capacitor on the ROM should be such that the ROM will power up in time: for example, at 10MHz oscillator frequency, the ROM must be powered up in less than 25μs.

Reading of this data is normally done in a single shot mode with the data read cycle started by either a positive or negative pulse on the program enable pin. The data read cycle is generated from a program clock at 1/64th of the reference oscillator frequency. A memory enable signal is supplied to allow power-down of the memory when not in use. Data select outputs remain in a high-impedance state when the program cycle is completed to allow the address bus to be used for other functions if desired.

Data is latched internally during the shaded portions of the program cycle and all data is transferred to the counters and latched during the data transfer time slot.

Alternatively, the PE pin may be grounded causing the data read cycle to repeat in a cyclic manner to allow continuous up-dating of the program information. In this mode external memory will be enabled continuously, (ME low) and the data read cycle will repeat every sixteen cycles of the internal program clock, i.e. every 1024/fosc seconds. This programming method is not recommended because of higher power consumption and the possibilities of noise injection into the loop from the digital data lines.

Power-on programming On power-up the data read cycle is automatically initiated making it unnecessary to provide a PE pulse on power-up. The circuit detects the power supply rising above a threshold point, (nominally 1.5V) and after an internally generated delay to allow the supply to rise fully the circuit is programmed in the normal way. This delay is generated by counting reference oscillator pulses and is therefore dependent on the crystal used. The delay consists of 53248 reference oscillator cycles giving a delay of about 5ms at 10MHz.

To ensure correct operation of this function the power supply rise time should be less than 5ms, (at 10MHz) rising smoothly through the threshold point.

PROGRAMMING IN EXTERNAL MODE

The external mode of programming is selected by grounding the program pin, (PR). In this mode timing is generated externally, normally from a microprocessor, and allows the user to change the data in selected latches. The data map is as Fig.5 with the PE pin used as a strobe for the data. Taking the PE pin high will transfer data from the data pins into the selected latch and taking this pin low will disable the data pins, retaining that data on the selected latch. Data transfer from all internal latches into the counters will occur simultaneously with the transfer of data into latch 1 and therefore this would normally be the final latch addressed during each channel change. Timing information for this mode of operation is given in Fig.8.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig.5 Data map

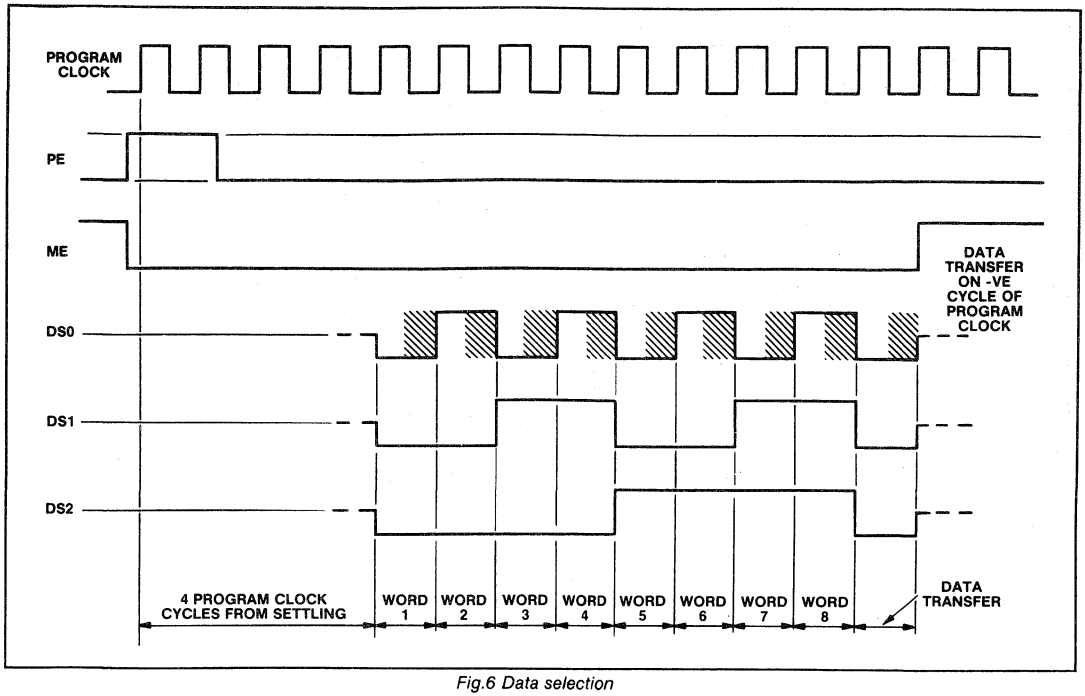


Fig.6 Data selection

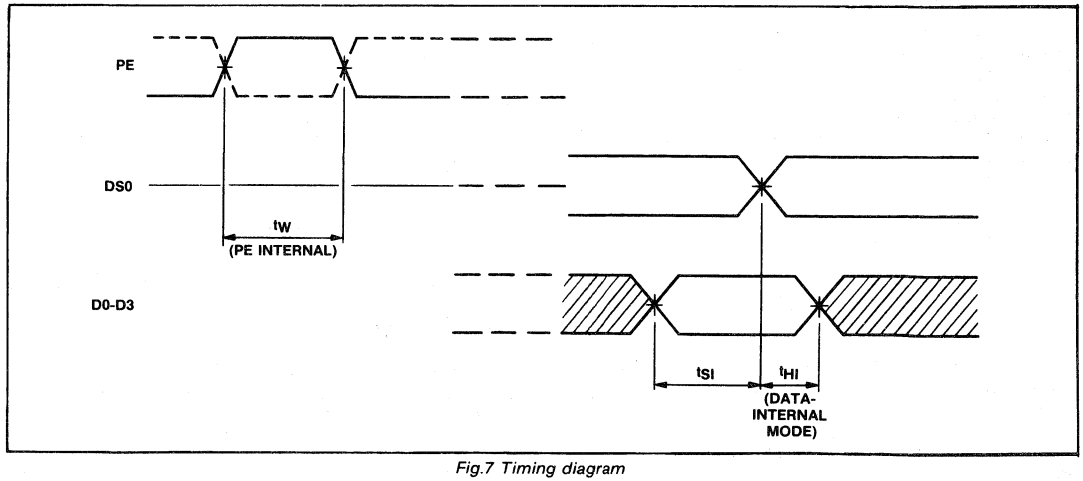


Fig.7 Timing diagram

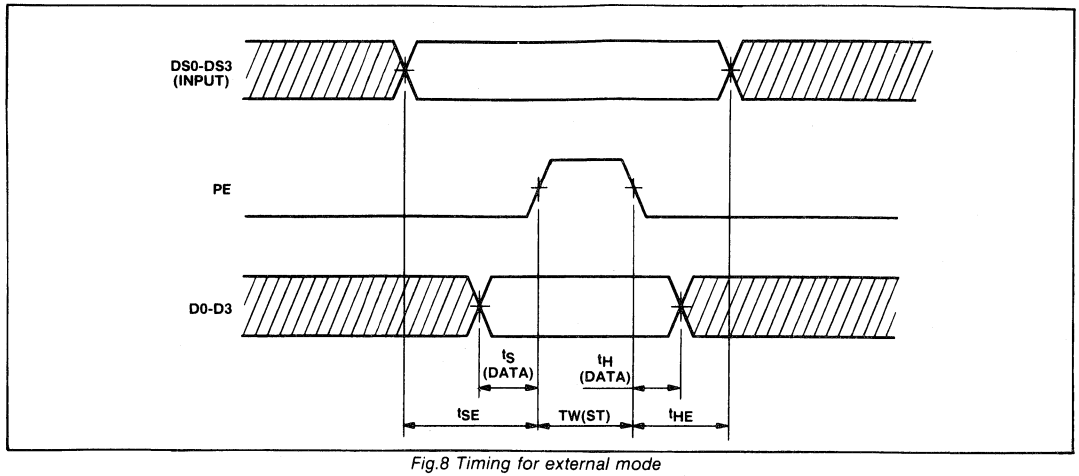


Fig.8 Timing for external mode

PHASE COMPARATORS

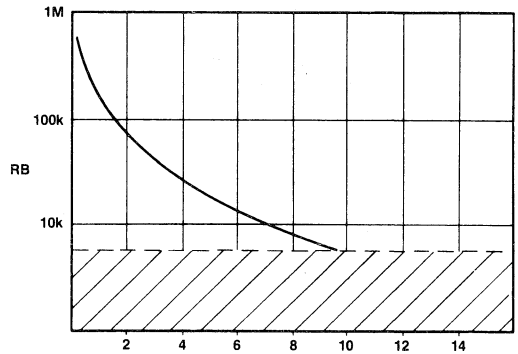
A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels. This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at (V_{DD}-V_{SS})/2 and any offset from this would be proportional to phase error. The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}\text{-}V_{SS}\text{-}0.7\text{-}89(RB^{-½})]}{2 \times \pi\ 50\text{x}10^{12} \times RB\text{x}FR}$$

The value of RB should be chosen to give the required gain at the reference frequency used. Fig.9 for example shows that to achieve a gain of 380V per radian at 10kHz requires approximately 39kΩ. A second external component is required; this is a hold capacitor of non-critical value which might typically be 470pF, a smaller value being sufficient if the sideband performance required is not high. Fig.9 shows the gain normalised to a 1Hz comparison frequency; to obtain the value for any other frequency, divide the value of Gain Frequency product by the desired frequency.



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320

Fig.9 RB versus gain and reference frequency

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

PLESSEY
Semiconductors

NJ8821, NJ8821B

FREQUENCY SYNTHESISER (MICROPROCESSOR INTERFACE) WITH RESETTABLE COUNTERS

The NJ8821/NJ8821B is a synthesiser circuit fabricated on the Plessey 5-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words under external control from a suitable microprocessor.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

The NJ8821 is available in Plastic DIL (DP) and Miniature Plastic DIL (MP) packages, both with operating temperature range of -30°C to +70°C. The NJ8821B is available only in Ceramic DIL package with operating temperature range of -40°C to +85°C.

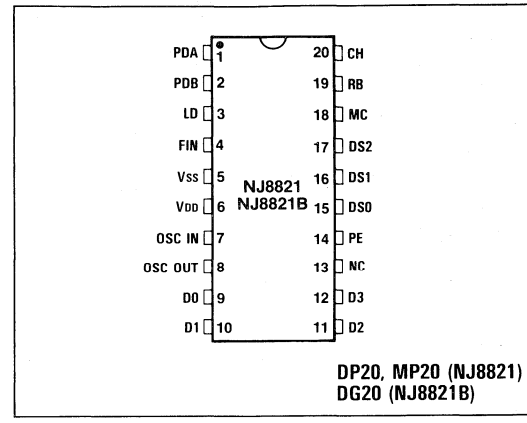


Fig.1 Pin connections

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Microprocessor Compatible
- >10MHz Input Frequency

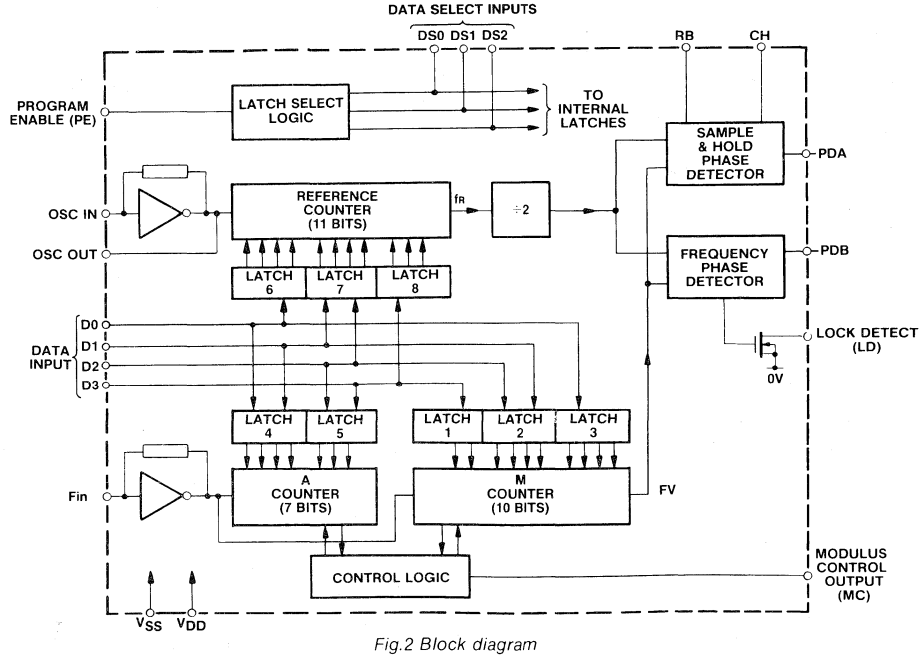


Fig.2 Block diagram

ELECTRICAL CONDITIONS

Test conditions (unless otherwise stated):

V_{DD}-V_{SS} 5V ± 0.5V

Temperature range NJ8821: -30°C to +70°C, NJ8821B: -40°C to +85°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.5	5.5	mA	FOSC, FIN = 10MHz, 0 to 5V square wave
		0.7	1.5	mA	FOSC, FIN = 1.0MHz, 0 to 5V square wave
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB Output					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	
INPUT LEVELS					
Data Inputs					
High level	4.25			V	TTL compatible
Low level			0.75	V	See note 1
Program Enable Input					
High level	4.25			V	
Low level			0.75	V	
DS INPUTS					
High level	4.25			V	
Low level			0.75	V	

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10.6			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS}. Note 4
Propagation delay, clock to modulus control		30	50	ns	Note 2
Strobe pulse width external mode, $t_{w(ST)}$	2			μs	
Data set-up time, $t_{s(DATA)}$	1			μs	
Data hold time, $t_{H(DATA)}$	1			μs	
Address set-up time, t_{SE}	1			μs	
Address hold time, t_{HE}	1			μs	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See Fig.6
Hold capacitor, CH			1	nF	Note 3
Output resistance PDA			5	kΩ	
Digital phase detector gain		1		V/Rad	

NOTES

1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. Finite output resistance of internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds.
4. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESIGNATION

Pin No.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. **Output at (V_{DD}-V_{SS})/2 when in lock.** Voltage increases as FV phase lead increases and decreases as FR phase lead increases. Output is linear over only a narrow phase window determined by gain programmed by RB.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses FV < FR or FR leading: negative pulses FV = FR and phase error within PDA window: high impedance
3	LD	An open drain lock detect output at low level when phase error within PDA window (in lock). High impedance at all other times.
4	FIN	The input to the main counters normally driven from a prescaler which may be AC coupled or when a full logic swing is available may be DC coupled.
5	V_{SS}	Negative supply (normally ground)
6	V_{DD}	Positive supply
7,8	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal-generated reference signal may alternatively be applied to OSC.IN. This may be a low-level signal AC coupled into OSC.IN or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 6-4094 in steps of 2, with the division ratio being twice the programmed number.
9,10,11,12	D0-D3	Information on these inputs is transferred to the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
14	PE	This pin is used as a strobe for the data. A logic high on this pin transfers data from the data pins to the internal latch selected by the address, (data select) lines, while a logic zero disables the data lines.
15,16,17	DS0-DS2	Data-select inputs to control the addressing of data latches.
18	MC	Signal for controlling an external dual-modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N +A where N and N +1 represent the dual modulus prescale values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The program range of the 'M' counter is 3-1023 and for correct program operation M ⩾A. Where every possible channel is required, the minimum division ratio should be N^2-N.
19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
20	CH	An external hold capacitor should be connected between this pin and V_{SS}.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD} - V_{SS})	-0.5V to 7V
Input voltage	
Open drain O/P (pin 3)	7V
All other pins	V_{SS} -0.3V to V_{DD} +0.3V
Storage temperature	-65°C to +150°C (DG Package, NJ8821B)
Storage temperature	-55°C to +125°C (DP and MP packages, NJ8821)

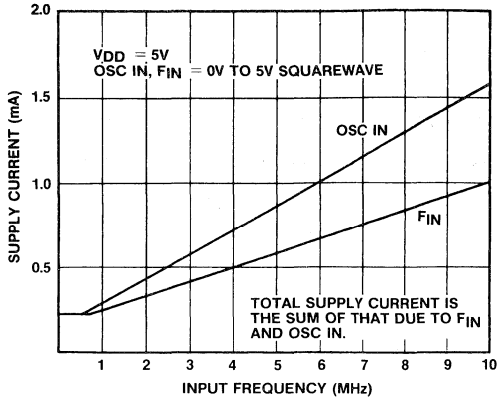


Fig.3 Typical supply current versus input frequency

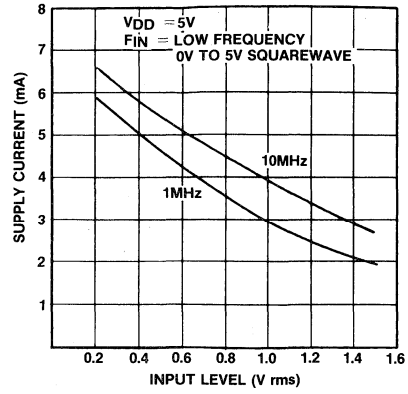


Fig.4 Typical supply current versus input level, Osc In

PROGRAMMING

Timing is generated externally, normally from a microprocessor, and allows the user to change the data in selected latches. The data map is Fig.5 with the PE pin used as a strobe for the data. Taking the PE pin high will transfer data from the data pins into the selected latch and taking this pin low will disable the data pins, retaining that data on the selected latch. Data transfer from all internal latches into the counters will occur simultaneously with the transfer of data into latch 1 and therefore this would normally be the final latch addressed during each channel change. Timing information for this mode of operation is given in Fig.6.

When re-programming, a reset to zero state is followed by reloading with the new counter values. This means the synthesiser loop lock up time will be well defined and less than 10msec. If shorter lock up times are required, when making only small changes in frequency, the non-resettable version NJ8823 should be considered.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig.5 Data map

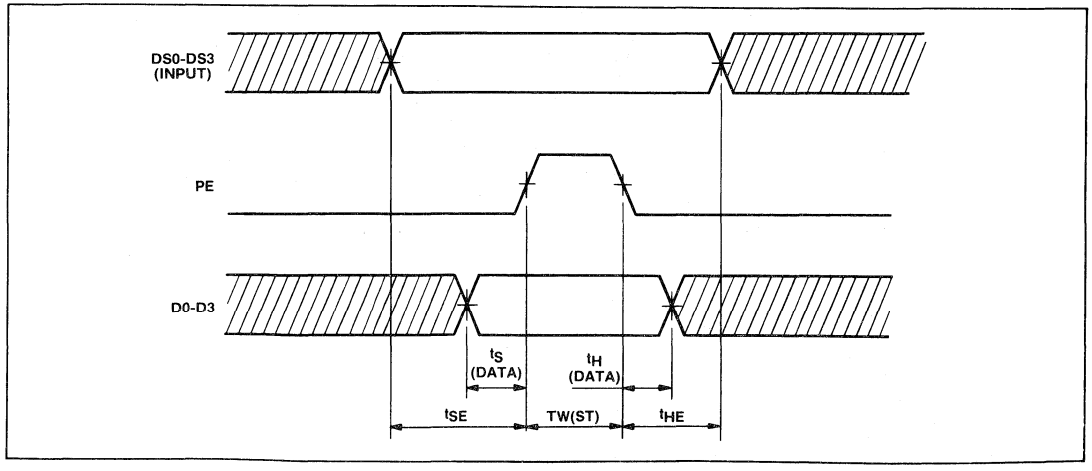


Fig.6 Timing diagram

PHASE COMPARATORS

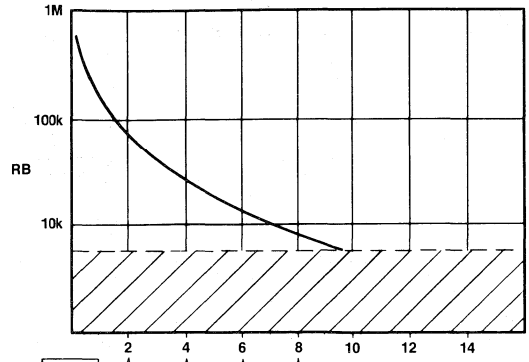
A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels. This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error. The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}-V_{SS}-0.7-89(RB^{-½})]}{2 \times \pi\ 50\times10^{-12} \times RB \times FR}$$

The value of RB should be chosen to give the required gain at the reference frequency used. Fig.7 for example shows that to achieve a gain of 380V per radian at 10kHz requires approximately 39kΩ. A second external component is required; this is a hold capacitor of non-critical value which might typically be 470pF, a smaller value being sufficient if the sideband performance required is not high. Fig.7 shows the gain normalised to a 1Hz comparison frequency; to obtain the value for any other frequency, divide the value of Gain Frequency product by the desired frequency.



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320

Fig.7 RB versus gain and reference frequency

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

PLESSEY Semiconductors

PRELIMINARY INFORMATION

NJ8821GG

FREQUENCY SYNTHESISER (MICROPROCESSOR INTERFACE)

The NJ8821GG is a synthesiser circuit fabricated with the 2-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words under external control from a suitable microprocessor.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

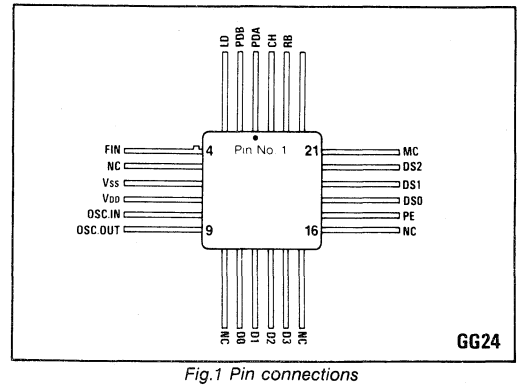


Fig.1 Pin connections

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Microprocessor Compatible
- > 10MHz Input Frequency

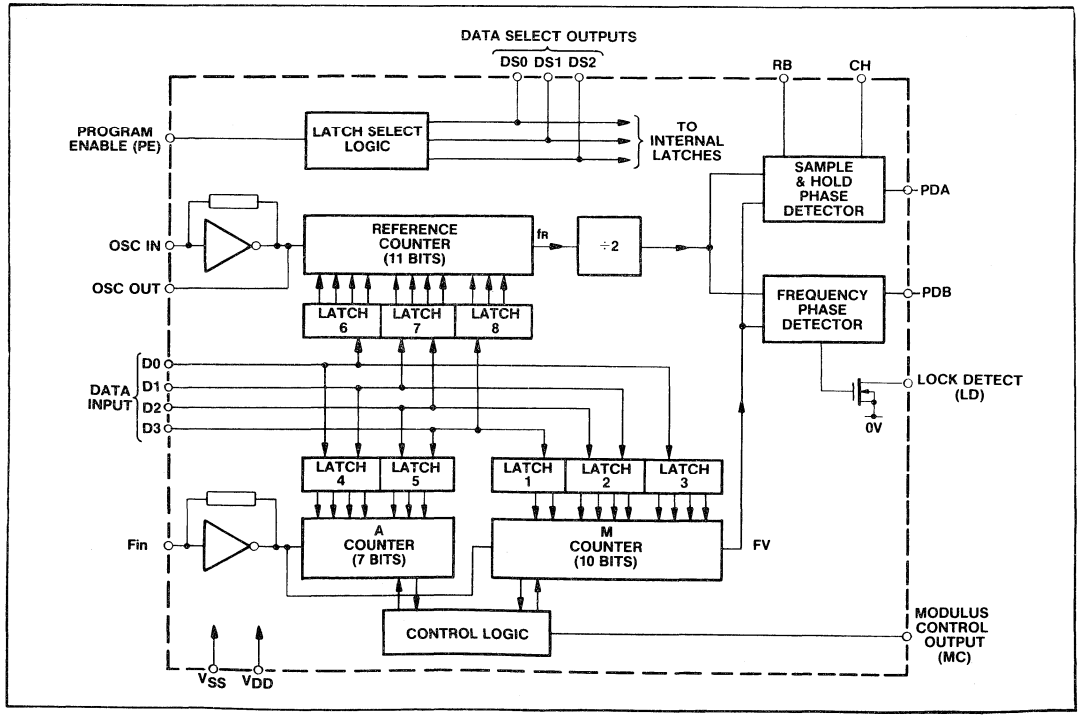


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD}-V_{SS} 5V ± 0.5V
Temperature range -30°C to +70°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.5	7.0	mA	FOSC, FIN = 10MHz } 0 to 5V
		0.7	2.0	mA	FOSC, FIN = 1.0MHz } square wave
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB Output					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	
INPUT LEVELS					
Data Inputs					
High level	4.25			V	TTL compatible
Low level			0.75	V	See note 1
Program Enable Input					
High level	4.25			V	
Low level			0.75	V	
DS INPUTS					
High level	4.25			V	
Low level			0.75	V	

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10.6			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS}. Note 4
Propagation delay, clock to modulus control		30	50	ns	Note 2
Strobe pulse width external mode, $t_{w(ST)}$	2			μs	
Data set-up time, $t_{s(DATA)}$	1			μs	
Data hold time, $t_{H(DATA)}$	1			μs	
Address set-up time, t_{SE}	1			μs	
Address hold time, t_{HE}	1			μs	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See Fig.6
Hold capacitor, CH			1	nF	Note 3
Output resistance PDA			5	kΩ	
Digital phase detector gain		1		V/Rad	

NOTES
1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. Finite output resistance of internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds.
4. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESIGNATION

Pin No.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. **Output at (V_{DD}-V_{SS})/2 when in lock.** Voltage increases as FV phase lead increases and decreases as FR phase lead increases. Output is linear over only a narrow phase window determined by gain programmed by RB.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses FV < FR or FR leading: negative pulses FV = FR and phase error within PDA window: high impedance
3	LD	An open drain lock detect output at low level when phase error within PDA window (in lock). High impedance at all other times.
4	FIN	The input to the main counters normally driven from a prescaler which may be AC coupled or when a full logic swing is available may be DC coupled.
6	V_{SS}	Negative supply (normally ground)
7	V_{DD}	Positive supply
8,9	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal-generated reference signal may alternatively be applied to OSC.IN. This may be a low-level signal AC coupled into OSC.IN or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 6-4094 in steps of 2, with the division ratio being twice the programmed number.
11,12,13,14	D0-D3	Information on these inputs is transferred to the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
17	PE	This pin is used as a strobe for the data. A logic high on this pin transfers data from the data pins to the internal latch selected by the address, (data select) lines, while a logic zero disables the data lines.
18,19,20	DS0-DS2	Data-select inputs to control the addressing of data latches.
21	MC	Signal for controlling an external dual-modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N +A where N and N +1 represent the dual modulus prescale values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The program range of the 'M' counter is 3-1023 and for correct program operation M ≥A. Where every possible channel is required, the minimum division ratio should be N^2-N.
23	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
24	CH	An external hold capacitor should be connected between this pin and V_{SS}.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD}-V_{SS}): -0.5V to 7V
Input voltage at any pin * V_{SS} -0.3V to V_{DD} +0.3V
Storage temperature: -65° C to +150° C

*Except on open drain outputs where this is 7V.

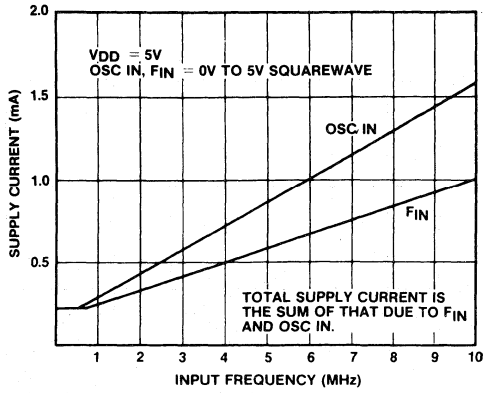


Fig.3 Typical supply current versus input frequency

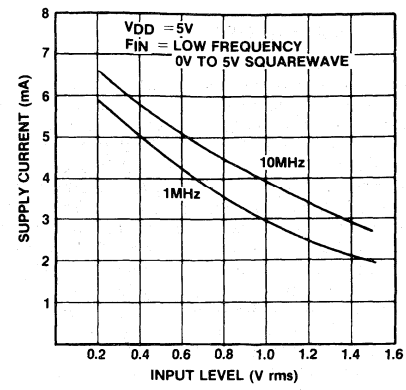


Fig.4 Typical supply current versus input level, Osc In

PROGRAMMING

Timing is generated externally, normally from a microprocessor, and allows the user to change the data in selected latches. The data map is Fig.5 with the PE pin used as a strobe for the data. Taking the PE pin high will transfer data from the data pins into the selected latch and taking this pin low will disable the data pins, retaining that data on the selected latch. Data transfer from all internal latches into the counters will occur simultaneously with the transfer of data into latch 1 and therefore this would normally be the final latch addressed during each channel change. Timing information for this mode of operation is given in Fig.6.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig.5 Data map

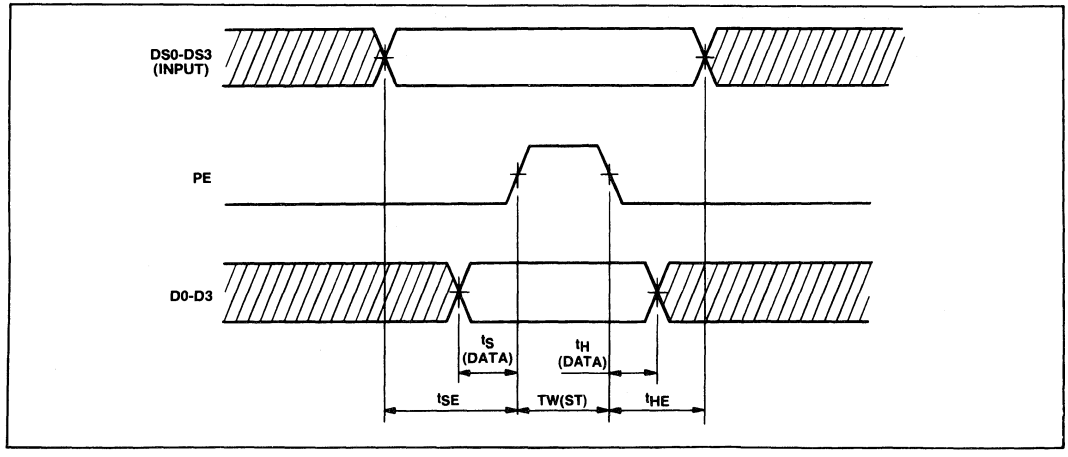


Fig.6 Timing diagram

NJ8821GG

PHASE COMPARATORS

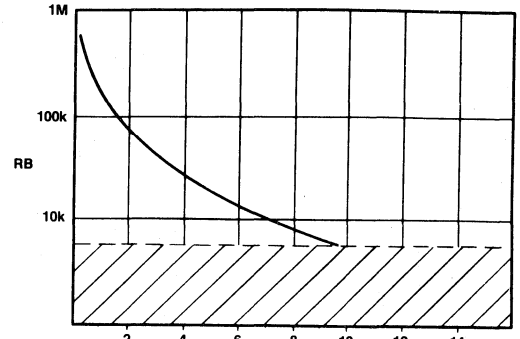
A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels. This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error. The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}-V_{SS}-0.7-89(RB^{-\frac{1}{2}})]}{2 \times \pi\ 50\times10^{-12} \times RB \times FR}$$

The value of RB should be chosen to give the required gain at the reference frequency used. Fig.7 for example shows that to achieve a gain of 380V per radian at 10kHz requires approximately 39kΩ. A second external component is required; this is a hold capacitor of non-critical value which might typically be 470pF, a smaller value being sufficient if the sideband performance required is not high. Fig.7 shows the gain normalised to a 1Hz comparison frequency; to obtain the value for any other frequency, divide the value of Gain Frequency product by the desired frequency.



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320

Fig.7 RB versus gain and reference frequency

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

PLESSEY
Semiconductors

NJ8822, NJ8822B

FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE) WITH RESETTABLE COUNTERS

The NJ8822 is a synthesiser circuit fabricated on the Plessey 5-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although 28 bits of data are initially required to program all counters subsequent updating can be abbreviated to 17 bits when only the 'A' and 'M' counters require changing.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 or SP8704 series to produce a universal binary coded synthesiser for up to 950MHz operation.

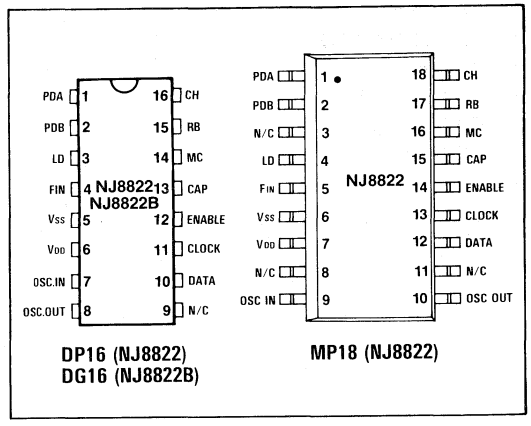


Fig. I Pin connections - top view, not to scale

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature
- >i10MHz Input Frequency

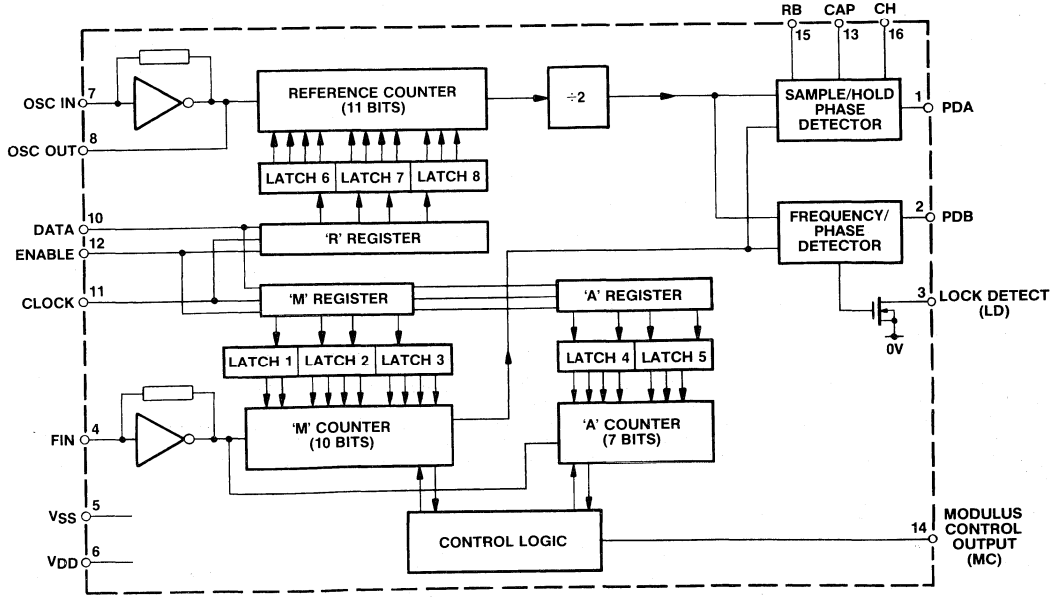


Fig.2 Block diagram. Pin numbers for MP package are shown in brackets.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{DD}-V_{SS} 5V ± 0.5V

Temperature range: NJ8822 -30°C to +70°C, NJ8822B -40°C to +85°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current			5.5	mA	FOSC, FIN = 10MHz } 0 to 5V square wave
			1.5	mA	FOSC, FIN = 1MHz }
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB OUTPUT					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS}, 25°C
Propagation delay, clock to modulus control		30	50	ns	Note 2
Programming inputs					
Clock high time, t_{cH}	0.5			μs	All timing periods are referenced to the negative transition of the clock waveform
Clock low time, t_{cL}	0.5			μs	
Enable set-up time, t_{ES}	0.2		t_{CH}	μs	
Enable hold time, t_{EH}	0.2			μs	
Data set-up time, t_{DS}	0.2			μs	
Data hold time, t_{DH}	0.2			μs	
Clock rise and fall times	0.2			μs	
Positive going threshold, V_{T+}	3			V	Note 1
Negative going threshold, V_{T-}			2	V	
Phase Detector					
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	
Hold capacitor, CH			1	nF	Note 3
Programming capacitor, CAP			1	nF	
Output resistance, PDA			5	kΩ	

NOTES

1. Data, Clock and Enable inputs are high impedance Schmitt buffers without pull up resistors. They are therefore not TTL compatible.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds.
4. The inputs to the device should be at logic '0' when power is applied if latch up conditions are to be avoided. This includes the signal/osc. frequency inputs.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD}-V_{SS}) -0.5V to 7V

Input voltage

Open drain O/P (pin 3 (DG) pin 4 (MP)) 7V

All other pins V_{SS} -0.3V to V_{DD} +0.3V

Storage temperature -55°C to +125°C (DP and MP packages, NJ8822)

Storage temperature -65°C to +150°C (DG package, NJ8822B)

PIN DESIGNATION

Pin No. DG,DP	Pin No. MP	Name	Description
1	1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as FV (FV is the output from the 'M' counter) phase lead increases and decreases as FR (FR is the output from the reference counter) phase lead increases. Output is linear over only a narrow phase window determined by gain (programmed by RB). **In a type 2 loop, this pin is at (V_{DD}-V_{SS})/2 when the system is in lock.**
-	3	N/C	Not connected.
2	2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses. FV < FR or FR leading: negative pulses. FV = FR and phase error within PDA window: high impedance.
3	4	LD	An open drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
4	5	FIN	The input to the main counters. It is normally driven from a prescaler which may be AC coupled or, when a full logic swing is available, may be DC coupled.
5	6	V_{SS}	Negative supply (ground).
6	7	V_{DD}	Positive supply (normally 5V).
-	8	N/C	Not connected.
7,8	9,10	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a 220 ohm resistor between Pin 8 and the crystal will improve stability. An external reference signal may alternatively be applied to OSC.IN. This may be a low-level signal, AC coupled, or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 3 to 2047 in steps of 1, with the division ratio being twice that programmed.
9	-	N/C	Not connected.
10	12	DATA	Information on this input is transferred to the internal latches during the appropriate data read time slot. Data is high for a '1' and low for a '0'. There are three data words which control the NJ8822, MSB is first in the order, 'A' - (7 bits), 'M' - (10 bits), 'R' - (11 bits).
11	13	CLK	Data is clocked in on the negative transition of the clock waveform. If less than 28 negative clock transitions have been received when the enable line goes low (i.e. only 'M' and 'A' will have been clocked in) then the 'R' counter latch will remain unchanged and only 'M' and 'A' will be transferred from the input shift register to the counter latches. This will protect the 'R' counter from being corrupted by any glitches on the clock line after only 'M' and 'A' have been loaded. If 28 negative transitions have been counted then the 'R' counter will be loaded with the new data.
12	14	ENABLE	When the enable is low the data and clock inputs are disabled internally. As soon as the enable is high the data and clock input are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the enable input and both inputs to the phase detector are synchronised to each other. Enable transitions only allowed when CLK is high.
13	15	CAP	This pin allows an external capacitor to be put in parallel with the ramp capacitor, and allows further programming of the device. (This capacitor is connected from CAP to V_{SS}).
14	16	MC	Output for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N + A where N and N + 1 represent the dual modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷ 128/129. The programming range of the 'M' counter is 3-1023 and for correct program operation M ⩾ A. Where every possible channel is required, the minimum division ratio should be $N^2 - N$.
15	17	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
16	18	CH	An external hold capacitor should be connected between this pin and V_{SS}.

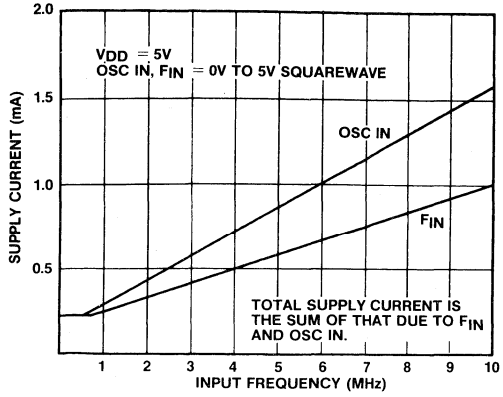


Fig.3 Typical supply current v. input frequency

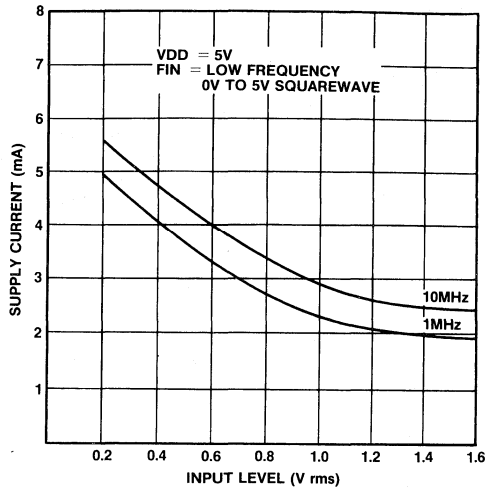


Fig.4 Typical supply current v. input level, Osc In

PROGRAMMING

Reference Divider Chain

The comparison frequency depends upon the crystal oscillator frequency and the division ratio of the R counter, which can be programmed in the range 3 to 2047.

$$R = \frac{fosc}{2 \times fcomp}$$

ie where *fcomp* = comparison frequency
fosc = oscillator frequency
R = R counter ratio

For example where crystal frequency = 10MHz and a channel spacing comparison frequency of 12.5kHz is required,

$$R = \frac{10^7}{2 \times 12.5 \times 10^3} = 400$$

Thus the R register would be programmed to 400 expressed in binary.
NB The total divider range is from 6 to 4094 in steps of 2.

VCO Divider Chain

The synthesised frequency of the voltage control oscillator (VCO) will depend on the division ratio of the M and A counters, the value of the external two modulus prescaler ($N/N + 1$) and the value of the comparison frequency *fcomp*.

The division ratio $P = NM + A$
where *M* is the ratio of the M counter in the range 3 to 1023 and *A* is the ratio of the A counter in the range 1 to 127.
Note $M \geqslant A$

$$\text{Also } P + \frac{fvco}{fcomp}$$

For example if the desired VCO frequency = 275MHz, the comparison frequency is 12.5kHz and a two modulus prescaler of ÷64/65 is being used, then:

$$P = \frac{275 \times 10^6}{12.5 \times 10^3} = 22 \times 10^3$$

Now $P = NM + A$
which can be rearranged to be $P/N = M + A/N$
In our example we have

$$\frac{22 \times 10^3}{64} = M + \frac{A}{6} \quad \text{therefore } 343.75 = M + \frac{A}{64}$$

M is programmed to the integer part = 343 and *A* is programmed to the fractional part times 64
ie $A = 0.75 \times 64 = 48$
NB The minimum ratio that can be used is $N^2 - N$
To check $P = 343 \times 64 + 48 = 22000$ which is the required divide ratio.

When re-programming, a reset to zero state is followed by reloading with the new counter values. This means the synthesiser loop lock up time will be well defined and less than 10msec. If shorter lock up times are required, when making only small changes in frequency, the non resettable version NJ8824 should be considered.

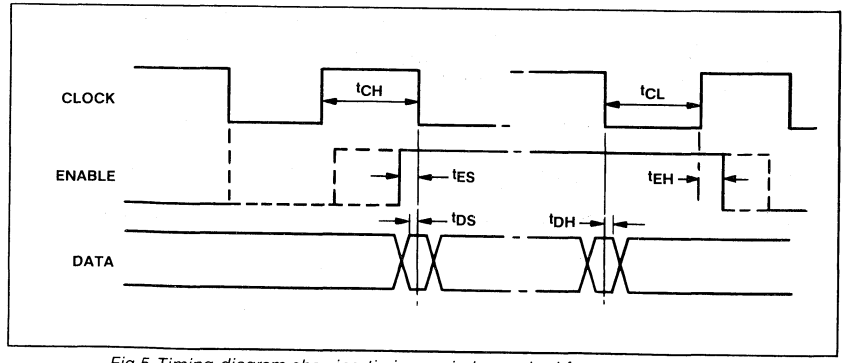


Fig.5 Timing diagram showing timing periods required for correct operation

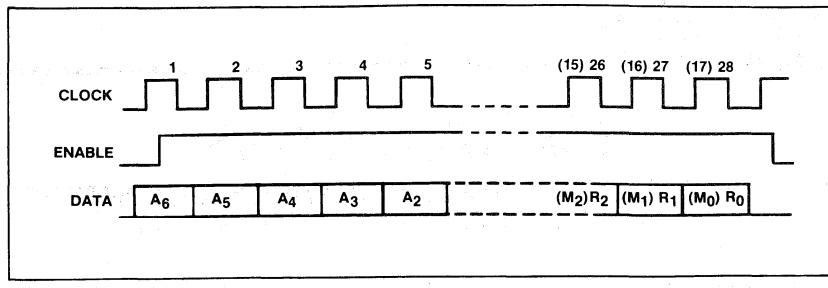


Fig.6 Timing diagram showing programming details

PHASE COMPARATORS

Noise output from a synthesiser loop is related to loop gain $K_\Phi K_V/P$, where K_Φ is phase detector constant (volts/rad), K_V is the VCO constant (rad-secs/volt) and P is the overall loop division ratio. When P is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase detector within the NJ8822 has both a high gain and uses a double sampling technique to reduce spurious ouputs to a low level.

A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels.

This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error.

The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB and a capacitor, CAP.

An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}-V_{SS}-0.7-89(RB^{-1/2})]}{2\pi\,[CAP + 50\times10^{-12}] \times RB \times FR}$$

The value of RB and CAP should be chosen to give the required gain at the reference frequency used. Fig.8 shows that to achieve a gain of 380V per radian at 10kHz requires RB to be approximately 39kΩ, CAP is zero. A hold capacitor (CH) of non-critical value which might be typically 470pF is connected from CH to V_{SS}. A smaller value is sufficient if the sideband performance required is not high.

The output from the sample/phase detector should be combined with that of the coarse phase/frequency detector and filtered to generate a single control voltage to drive the VCO.

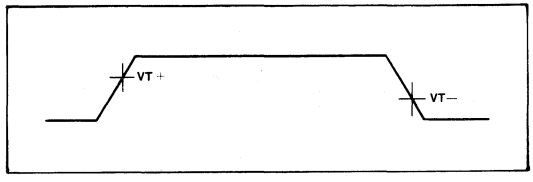


Fig.7 Timing diagram showing voltage thresholds

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

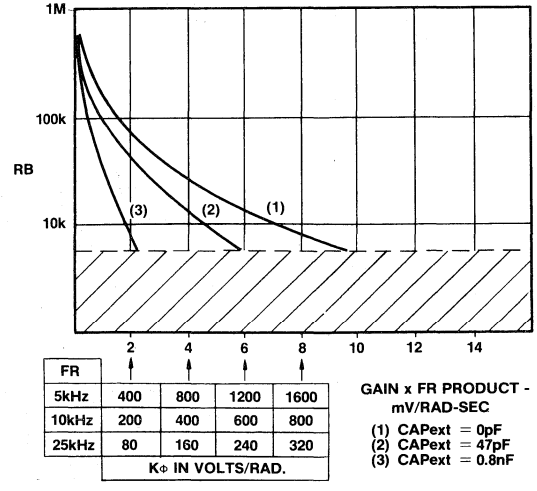


Fig.8 RB v. gain and reference frequency

NJ8823, NJ8823B

FREQUENCY SYNTHESISER (MICROPROCESSOR INTERFACE) WITH NON-RESETTABLE COUNTERS

The NJ8823/NJ8823B is a synthesiser circuit fabricated on the Plessey 5-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words under external control from a suitable microprocessor.

The NJ8823 is available in Plastic DIL (DP) and Miniature Plastic DIL (MP) poackages, both with operating temperature range of -30°C to +70°C. The NJ8823B is available only in Ceramic DIL package with operating temperature range of -40°C to +85°C.

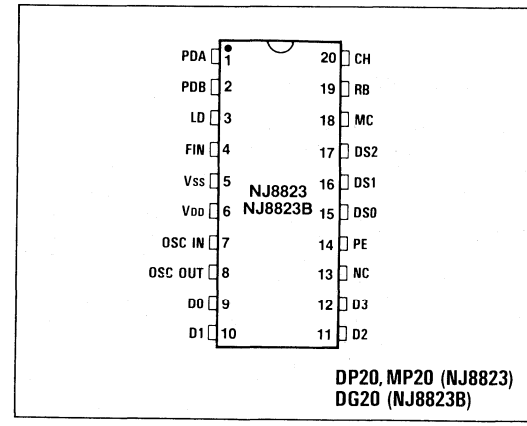


Fig.1 Pin connections

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Microprocessor Compatible
- > 10MHz Input Frequency
- Fast Lock Up Time

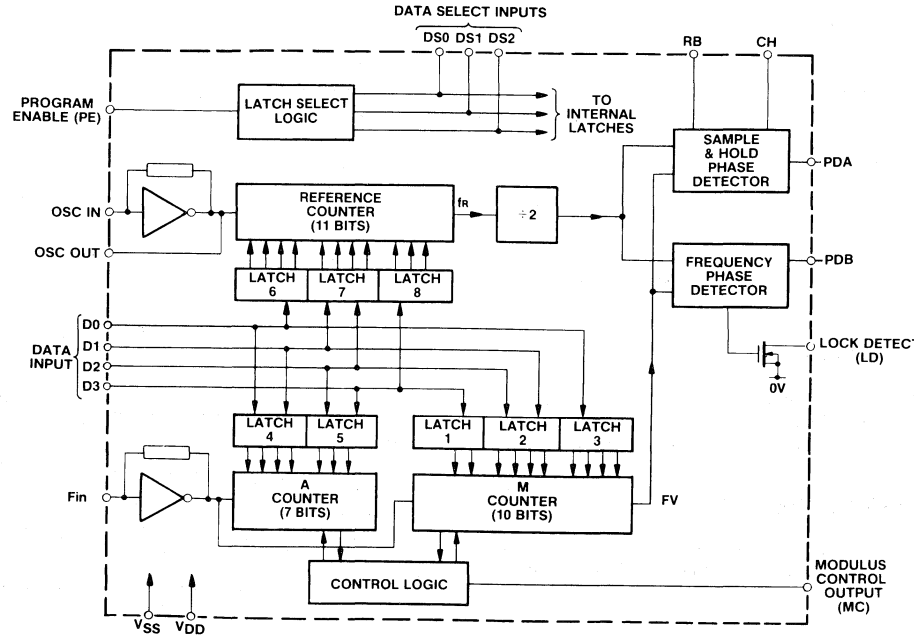


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{DD}-V_{SS} 5V ± 0.5V

Temperature range: NJ8823 -30°C to +70°C, NJ8823B -40°C to +85°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.5	5.5	mA	FOSC, FIN = 10MHz } 0 to 5V square wave
		0.7	1.5	mA	FOSC, FIN = 1.0MHz }
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB Output					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	
INPUT LEVELS					
Data Inputs					
High level	4.25			V	TTL compatible
Low level			0.75	V	See note 1
Program Enable Input					
High level	4.25			V	
Low level			0.75	V	
DS INPUTS					
High level	4.25			V	
Low level			0.75	V	

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10.6			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS}.Note 4
Propagation delay, clock to modulus control		30	50	ns	Note 2
Strobe pulse width external mode, $t_{w(ST)}$	2			μs	
Data set-up time, $t_{s(DATA)}$	1			μs	
Data hold time, $t_{H(DATA)}$	1			μs	
Address set-up time, t_{SE}	1			μs	
Address hold time, t_{HE}	1			μs	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See Fig.6
Hold capacitor, CH			1	nF	Note 3
Output resistance PDA			5	kΩ	
Digital phase detector gain		1		V/Rad	

NOTES

1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. Finite output resistance of internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds.
4. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESIGNATION

Pin No.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. **Output at (V_{DD}-V_{SS})/2 when in lock.** Voltage increases as FV phase lead increases and decreases as FR phase lead increases. Output is linear over only a narrow phase window determined by gain programmed by RB.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses FV < FR or FR leading: negative pulses FV = FR and phase error within PDA window: high impedance
3	LD	An open drain lock detect output at low level when phase error within PDA window (in lock). High impedance at all other times.
4	FIN	The input to the main counters normally driven from a prescaler which may be AC coupled or when a full logic swing is available may be DC coupled.
5	V_{SS}	Negative supply (normally ground)
6	V_{DD}	Positive supply
7,8	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal-generated reference signal may alternatively be applied to OSC.IN. This may be a low-level signal AC coupled into OSC.IN or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 6-4094 in steps of 2, with the division ratio being twice the programmed number.
9,10,11,12	D0-D3	Information on these inputs is transferred to the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
14	PE	This pin is used as a strobe for the data. A logic high on this pin transfers data from the data pins to the internal latch selected by the address, (data select) lines, while a logic zero disables the data lines.
15,16,17	DS0-DS2	Data-select inputs to control the addressing of data latches.
18	MC	Signal for controlling an external dual-modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N +A where N and N +1 represent the dual modulus prescale values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The program range of the 'M' counter is 3-1023 and for correct program operation M ≥A. Where every possible channel is required, the minimum division ratio should be N^2-N.
19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
20	CH	An external hold capacitor should be connected between this pin and V_{SS}.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD} - V_{SS})	-0.5V to 7V
Input voltage	
Open drain O/P (pin 3)	7V
All other pins	V_{SS} -0.3V to V_{DD} +0.3V
Storage temperature	-65 °C to +150 °C (DG Package, NJ8823B)
Storage temperature	-55 °C to +125 °C (DP and MP Packages, NJ8823)

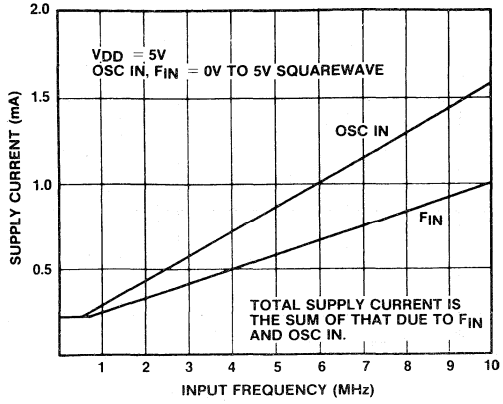


Fig.3 Typical supply current versus input frequency

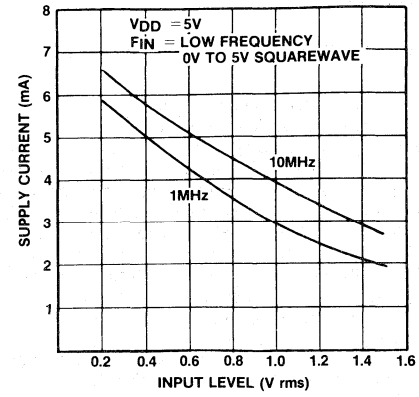


Fig.4 Typical supply current versus input level, Osc In

PROGRAMMING

Timing is generated externally, normally from a microprocessor, and allows the user to change the data in selected latches. The data map is Fig.5 with the PE pin used as a strobe for the data. Taking the PE pin high will transfer data from the data pins into the selected latch and taking this pin low will disable the data pins, retaining that data on the selected latch. Data transfer from all internal latches into the counters will occur simultaneously with the transfer of data into latch 1 and therefore this would normally be the final latch addressed during each channel change. Timing information for this mode of operation is given in Fig.6.

When re-programming, the counters are changed only when they reach a zero state. There is no reset to zero state. This means the synthesiser loop lock up time will be variable. For the case when only small changes in frequency are required, the non-resettable synthesiser should achieve the shortest loop lock up times.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig.5 Data map

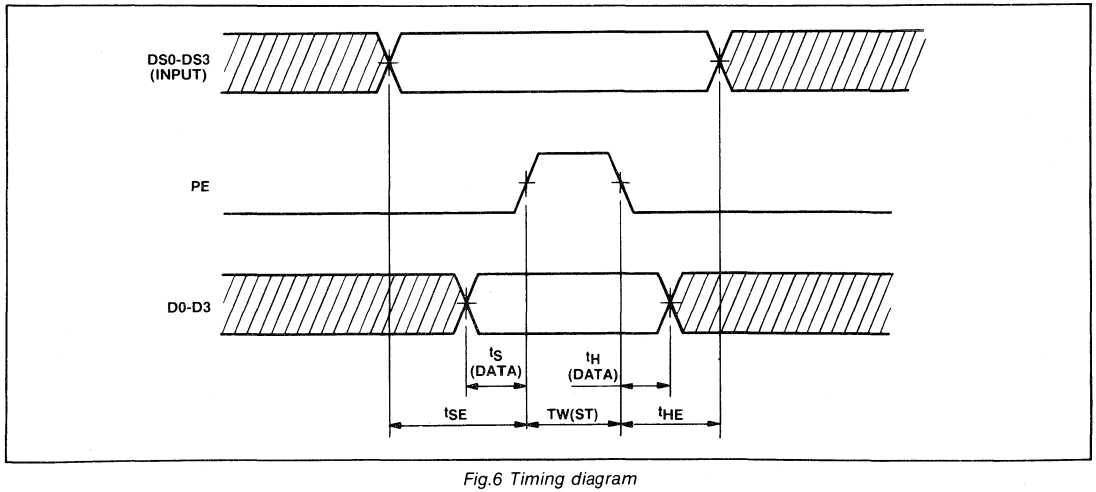


Fig.6 Timing diagram

PHASE COMPARATORS

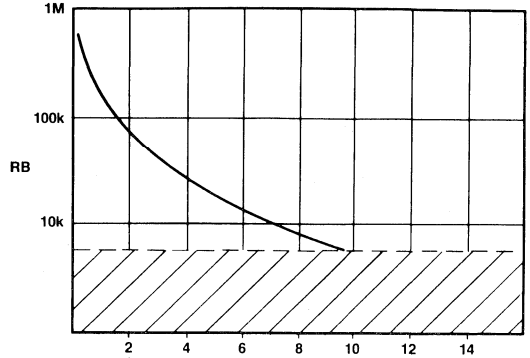
A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels. This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error. The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}-V_{SS}-0.7-89(RB^{-½})]}{2 \times \pi\ 50\times10^{-12} \times RB \times FR}$$

The value of RB should be chosen to give the required gain at the reference frequency used. Fig.7 for example shows that to achieve a gain of 380V per radian at 10kHz requires approximately 39kΩ. A second external component is required; this is a hold capacitor of non-critical value which might typically be 470pF, a smaller value being sufficient if the sideband performance required is not high. Fig.7 shows the gain normalised to a 1Hz comparison frequency; to obtain the value for any other frequency, divide the value of Gain Frequency product by the desired frequency.



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320

Fig.7 RB versus gain and reference frequency

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

PLESSEY
Semiconductors

NJ8824, NJ8824B

FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE) WITH NON-RESETTABLE COUNTERS

The NJ8824 is a synthesiser circuit fabricated on the Plessey 5-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although 28 bits of data are initially required to program all counters subsequent updating can be abbreviated to 17 bits when only the 'A' and 'M' counters require changing.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 or SP8704 series to produce a universal binary coded synthesiser for up to 960MHz operation.

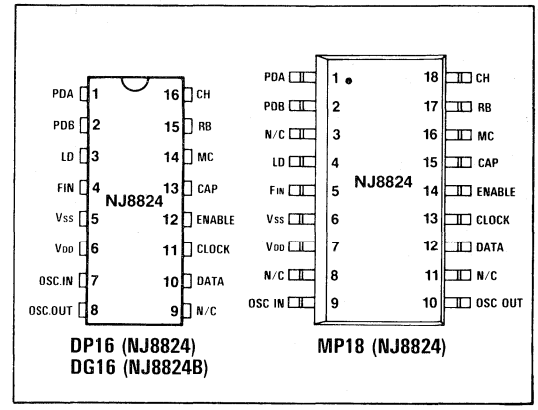


Fig. I Pin connections - top view, not to scale

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature
- >10MHz Input Frequency
- Fast Lock Up Time

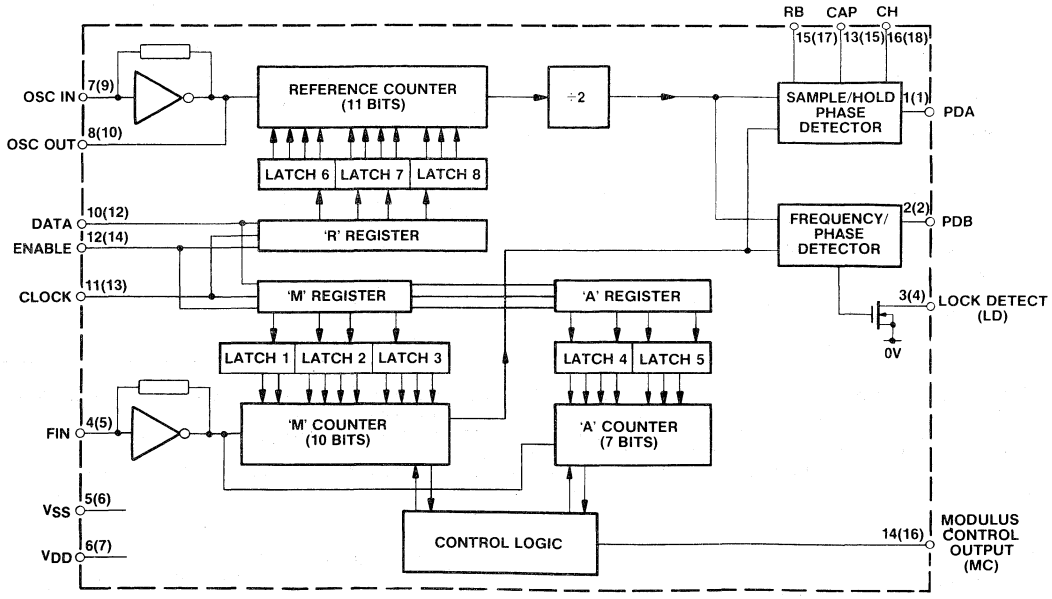


Fig.2 Block diagram. Pin numbers for MP package are shown in brackets.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD}-V_{SS} 5V ± 0.5V
Temperature range: NJ8824 -30°C to +70°C, NJ8824B -40°C to +85°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current			5.5	mA	FOSC, FIN = 10MHz } 0 to 5V square wave
			1.5	mA	FOSC, FIN = 1MHz }
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB OUTPUT					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS}, 25°C
Propagation delay, clock to modulus control		30	50	ns	Note 2
Programming inputs					
Clock high time, t_{cH}	0.5			μs	All timing periods are referenced to the negative transition of the clock waveform
Clock low time, t_{cL}	0.5			μs	
Enable set-up time, t_{ES}	0.2		t_{CH}	μs	
Enable hold time, t_{EH}	0.2			μs	
Data set-up time, t_{DS}	0.2			μs	
Data hold time, t_{DH}	0.2			μs	
Clock rise and fall times	0.2			μs	
Positive going threshold, V_T +	3			V	Note 1
Negative going threshold, V_T-			2	V	
Phase Detector					
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	
Hold capacitor, CH			1	nF	Note 3
Programming capacitor, CAP			1	nF	
Output resistance, PDA			5	kΩ	

NOTES
1. Data, Clock and Enable inputs are high impedance Schmitt buffers without pull up resistors. They are therefore not TTL compatible.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds.
4. The inputs to the device should be at logic '0' when power is applied if latch up conditions are to be avoided. This includes the signal/osc. frequency inputs.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD}-V_{SS}) -0.5V to 7V
Input voltage
Open drain O/P (pin 3 (DG) pin 4 (MP)) 7V
All other pins V_{SS} -0.3V to V_{DD} +0.3V

Storage temperature -55°C to +125°C (DP and MP packages, NJ8824)
Storage temperature -65°C to +150°C (DG packages, NJ8824B)

PIN DESIGNATION

Pin No. DP	Pin No. MP	Name	Description
1	1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as FV (FV is the output from the 'M' counter) phase lead increases and decreases as FR (FR is the output from the reference counter) phase lead increases. Output is linear over only a narrow phase window determined by gain (programmed by RB). **In a type 2 loop, this pin is at (V_{DD}-Vss)/2 when the system is in lock.**
-	3	N/C	Not connected.
2	2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses. FV < FR or FR leading: negative pulses. FV = FR and phase error within PDA window: high impedance.
3	4	LD	An open drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
4	5	FIN	The input to the main counters. It is normally driven from a prescaler which may be AC coupled or, when a full logic swing is available, may be DC coupled.
5	6	V_{SS}	Negative supply (ground).
6	7	V_{DD}	Positive supply (normally 5V).
-	8	N/C	Not connected.
7,8	9,10	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a 220 ohm resistor between Pin 8 and the crystal will improve stability. An external reference signal may alternatively be applied to OSC.IN. This may be a low-level signal, AC coupled, or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 3 to 2047 in steps of 1, with the division ratio being twice that programmed.
9	-	N/C	Not connected.
10	12	DATA	Information on this input is transferred to the internal latches during the appropriate data read time slot. Data is high for a '1' and low for a '0'. There are three data words which control the NJ8824, MSB is first in the order, 'A' - (7 bits), 'M' - (10 bits), 'R' - (11 bits).
11	13	CLK	Data is clocked in on the negative transition of the clock waveform. If less than 28 negative clock transitions have been received when the enable line goes low (i.e. only 'M' and 'A' will have been clocked in) then the 'R' counter latch will remain unchanged and only 'M' and 'A' will be transferred from the input shift register to the counter latches. This will protect the 'R' counter from being corrupted by any glitches on the clock line after only 'M' and 'A' have been loaded. If 28 negative transitions have been counted then the 'R' counter will be loaded with the new data.
12	14	ENABLE	When the enable is low the data and clock inputs are disabled internally. As soon as the enable is high the data and clock input are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the enable input and both inputs to the phase detector are synchronised to each other. Enable transitions only allowed when CLK is high.
13	15	CAP	This pin allows an external capacitor to be put in parallel with the ramp capacitor, and allows further programming of the device. (This capacitor is connected from CAP to V_{SS}).
14	16	MC	Output for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N + A where N and N + 1 represent the dual modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷ 128/129. The programming range of the 'M' counter is 3-1023 and for correct program operation M ⩾ A. Where every possible channel is required, the minimum division ratio should be N^2 - N.
15	17	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
16	18	CH	An external hold capacitor should be connected between this pin and V_{SS}.

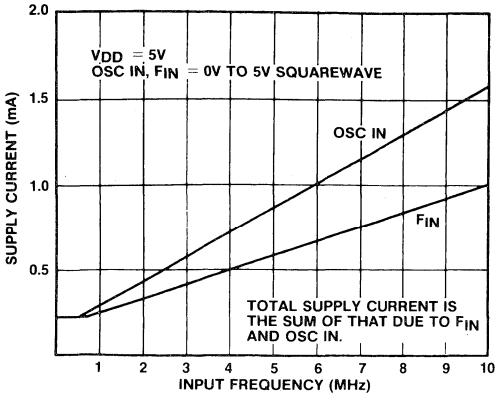


Fig.3 Typical supply current v. input frequency

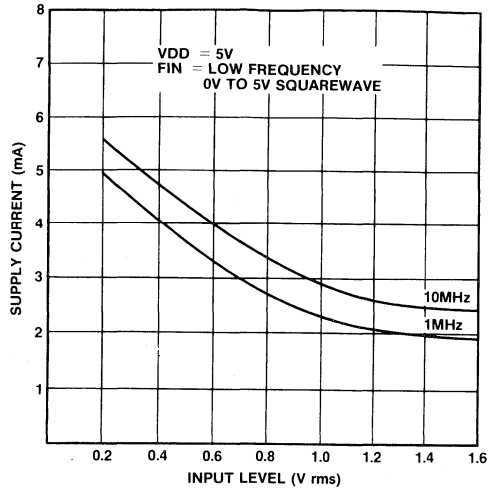


Fig.4 Typical supply current v. input level, Osc In

PROGRAMMING

Reference Divider Chain

The comparison frequency depends upon the crystal oscillator frequency and the division ratio of the R counter, which can be programmed in the range 3 to 2047.

$$R = \frac{fosc}{2 \times fcomp}$$

ie where *fcomp* = comparison frequency
fosc = oscillator frequency
R = R counter ratio

For example where crystal frequency = 10MHz and a channel spacing comparison frequency of 12.5kHz is required,

$$R = \frac{10^7}{2 \times 12.5 \times 10^3} = 400$$

Thus the R register would be programmed to 400 expressed in binary.
NB The total divider range is from 6 to 4094 in steps of 2.

VCO Divider Chain

The synthesised frequency of the voltage control oscillator (VCO) will depend on the division ratio of the M and A counters, the value of the external two modulus prescaler ($N/N + 1$) and the value of the comparison frequency *fcomp*.

The division ratio $P = NM + A$
where *M* is the ratio of the M counter in the range 3 to 1023 and *A* is the ratio of the A counter in the range 1 to 127.
Note $M \geqslant A$

$$\text{Also } P + \frac{fvco}{fcomp}$$

For example if the desired VCO frequency = 275MHz, the comparison frequency is 12.5kHz and a two modulus prescaler of ÷64/65 is being used, then:

$$P = \frac{275 \times 10^6}{12.5 \times 10^3} = 22 \times 10^3$$

Now $P = NM + A$
which can be rearranged to be $P/N = M + A/N$
In our example we have

$$\frac{22 \times 10^3}{64} = M + \frac{A}{6} \quad \text{therefore } 343.75 = M + \frac{A}{64}$$

M is programmed to the integer part = 343 and *A* is programmed to the fractional part times 64
ie $A = 0.75 \times 64 = 48$
NB The minimum ratio that can be used is $N^2 - N$
To check $P = 343 \times 64 + 48 = 22000$ which is the required divide ratio.

When re-programming, the counters are changed only when they reach a zero state. There is no reset to zero state. This means the synthesiser loop lock up time will be variable. For the case when only small changes in frequency are required, the non-resettable synthesiser should achieve the shortest loop lock up times.

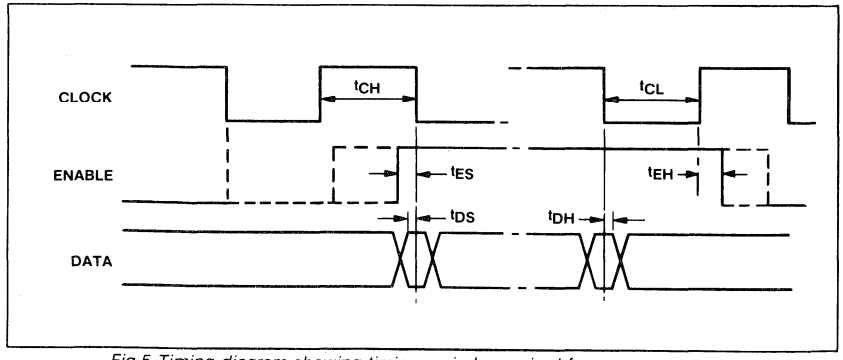


Fig.5 Timing diagram showing timing periods required for correct operation

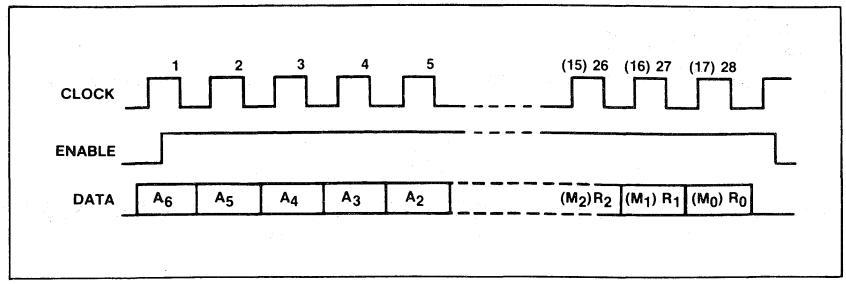


Fig.6 Timing diagram showing programming details

PHASE COMPARATORS

Noise output from a synthesiser loop is related to loop gain $K_\Phi K_V/P$, where K_Φ is phase detector constant (volts/rad), K_V is the VCO constant (rad-secs/volt) and P is the overall loop division ratio. When P is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase detector, within the NJ8824 has both a high gain and uses a double sampling technique to reduce spurious outputs to a low level.

A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels.

This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error.

The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB and a capacitor, CAP.

An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}-V_{SS}-0.7-89(RB^{-1/2})]}{2\pi\,[CAP + 50\times10^{-12}] \times RB \times FR}$$

The value of RB and CAP should be chosen to give the required gain at the reference frequency used. Fig.8 shows that to achieve a gain of 380V per radian at 10kHz requires RB to be approximately 39kΩ, CAP is zero. A hold capacitor (CH) of non-critical value which might be typically 470pF is connected from CH to V_{SS}. A smaller value is sufficient if the sideband performance required is not high.

The output from the sample/phase detector should be combined with that of the coarse phase/frequency detector and filtered to generate a single control voltage to drive the VCO.

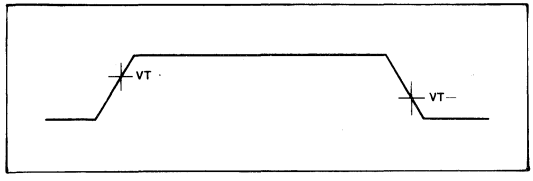


Fig.7 Timing diagram showing voltage thresholds

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

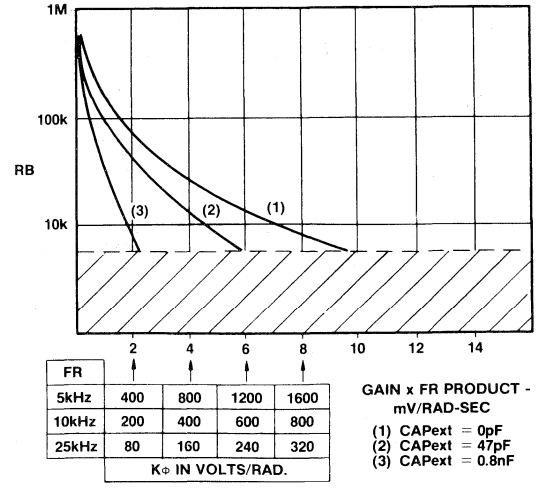


Fig.8 RB v. gain and reference frequency

PLESSEY
Semiconductors

NJ88C25

FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE)

The NJ88C25 is a synthesiser circuit fabricated on the 2-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter, latched and buffered Band 0 and Band 1 outputs and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although thirty bits of data are initially required to program all counters, subsequent updating can be abbreviated to nineteen bits when only the 'A', 'M' and 'B' counters require changing.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

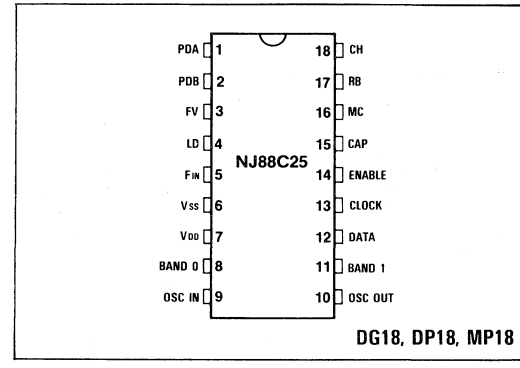


Fig.1 Pin connections - top view

FEATURES

- 3.0V to 5.0V Supply Range
- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature
- > 20MHz Input Frequency

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD} - V_{SS})	-0.5V to 7V
Input voltage	
Open drain O/Ps (pins 3 & 4)	7V
All other pins	V_{SS} -0.3V to V_{DD} +0.3V
Storage temperature	-65°C to +150°C

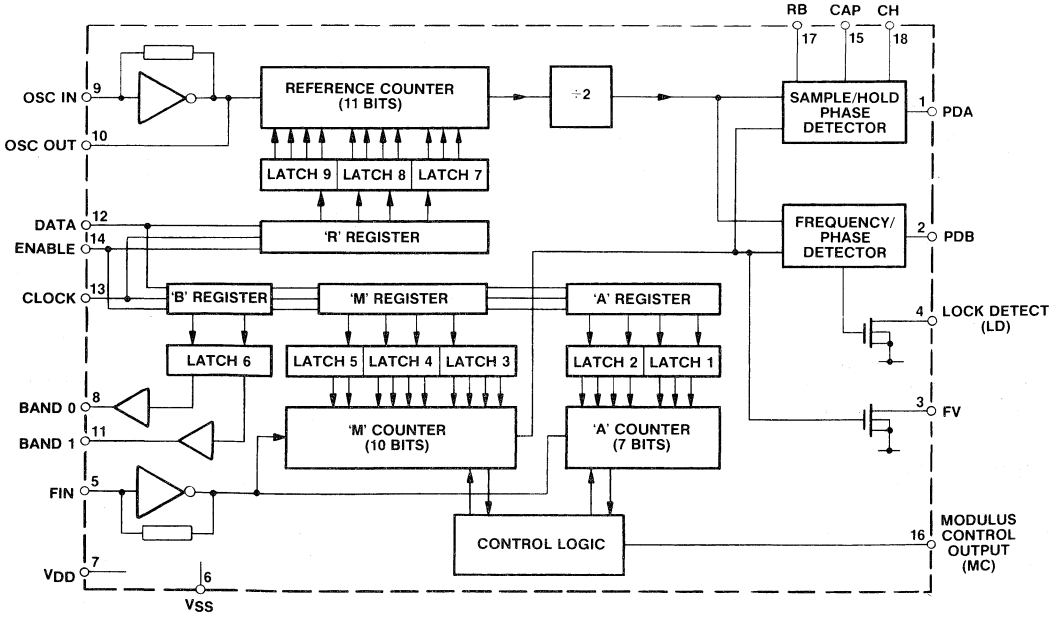


Fig.2 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} - V_{SS} 2.7V to 5.5V, Temperature Range -30°C to +70°C

DC Characteristics at V_{DD} = 5.0V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5.5	TBA	mA	FOSC, FIN = 20MHz } 0 to 5V
		0.7	TBA	mA	FOSC, FIN = 1MHz } square
		3.7	TBA	mA	FOSC, FIN = 10MHz } wave
Modulus Control out, BAND 0, BAND 1					
High level	V_{DD}-0.4			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
Lock Detect Out, FV					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			7	V	
PDB output					
High level	4.6			V	I_{source} 4mA
Low level			0.4	V	I_{sink} 4mA
3-state leakage			±0.1	μA	

AC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC outputs	200			mV RMS	20MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	20			MHz	V_{DD} = 5V, 0 to 5V square wave
Propagation delay, clock to modulus control		30	50	ns	Note 2
Programming inputs					
Clock high time, t_{CH}	0.5			μs	
Clock low time, t_{CL}	0.5			μs	
Enable set-up time, t_{ES}	0.2		t_{CH}	μs	Note 5
Enable hold time, t_{EH}	0.2			μs	
Data set-up time, t_{DS}	0.2			μs	
Data hold time, t_{DH}	0.2			μs	
Clock rise and fall times	0.2			μs	
Positive going threshold, V_T+	3			V	TTL compatible
Negative going threshold, V_T-			2	V	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	
Hold capacitor, CH			1	nF	Note 3
Programming capacitor, CAP			1	nF	
Output resistance, PDA			5	kΩ	

NOTES
1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time constant of 5 microseconds.
4. The inputs to the device should be at logic '0' when power is applied if latch up conditions are to be avoided. This includes the signal/osc. frequency inputs.
5. Clock to enable set up time is variable, dependent on frequency of OSC. IN, it needs to be specified in terms of OSC. IN frequency, clock high time (t_{CH}) and clock low time (t_{CL}). Enable set-up time, t_{ES} must meet following conditions: $4 \times 1/\text{OSC. IN} \leqslant t_{ES} < (t_{CH} + t_{CL})$.

PIN DESIGNATION

Pin No.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as FV (FV is the output from the 'M' counter) phase lead increases and decreases as FR (FR is the output from the reference counter) phase lead increases. Output is linear over only a narrow phase window determined by gain (programmed by RB). **In a type 2 loop, this pin is at (V_{DD}-Vss)/2 when the system is in lock.**
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses. FV < FR or FR leading: negative pulses. FV = FR and phase error within PDA window: high impedance.
3	FV	This pin is an open drain output from the 'M' counter.
4	LD	An open drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
5	FIN	The input to the main counters. It is normally driven from a prescaler which may be AC coupled or, when a full logic swing is available, may be DC coupled.
6	V_{SS}	Negative supply (ground).
7	V_{DD}	Positive supply (normally 5V).
9,10	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a 220Ω resistor between Pin 8 and the crystal will improve stability. An external reference signal may alternatively be applied to OSC.IN. This may be a low-level signal, AC coupled, or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 3 to 2047 in steps of 1, with the division ratio being twice that programmed.
8,11	BAND 0/1	Two latch outputs, providing an output of the data from the register 'B'.
12	DATA	Information on this input is transferred to the internal latches during the appropriate data read time slot. Data is high for a '1' and low for a '0'. There are four data words which control the NJ88C25, MSB is first in the order, 'A' - (7 bits), 'M' - (10 bits), 'B' (2 bits) and 'R' (11 bits).
13	CLOCK	Data is clocked in on the negative transition of the clock waveform. If less than 30 negative clock transitions have been received when the enable line goes low (ie only 'B', 'M' and 'A' have been clocked in) then the 'R' counter latch will remain unchanged and only 'B', 'M' and 'A' will be transferred from the input shift register to the counter latches. This will protect the 'R' counter from being corrupted by any glitches on the clock line after only 'B', 'M' and 'A' have been loaded. If 30 negative transitions have been counted then the 'R' counter will be loaded with the new data.
14	ENABLE	When the enable is low the data and clock inputs are disabled internally. As soon as the enable is high the data and clock inputs are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the enable input and both inputs to the phase detector are synchronised to each other. Enable transitions are only allowed when CLK is high.
15	CAP	This pin allows an external capacitor to be put in parallel with the ramp capacitor, and allows further programming of the device. (This capacitor is connected from CAP to Vss.)
16	MC	Output for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle.The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N + A where N and N + 1 represent the dual modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The programming range of the 'M' counter is 3-1023 and for correct program operation M ≥ A. Where every possible channel is required, the minimum division ratio should be N^2-N.
17	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and Vss.
18	CH	An external hold capacitor should be connected between this pin and Vss.

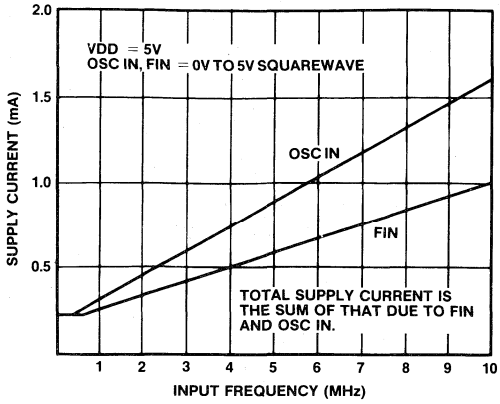


Fig.3 Typical supply current versus input frequency

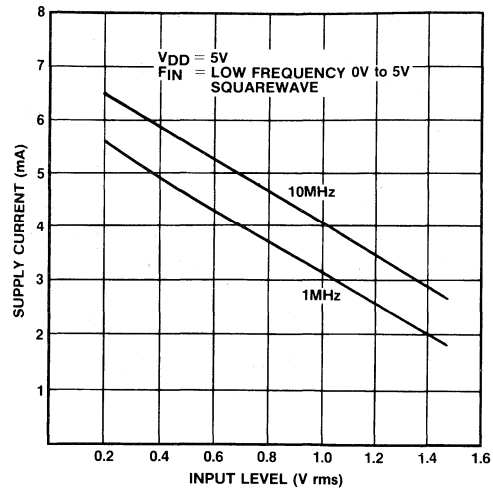


Fig.4 Typical supply current versus input level, Osc In

PROGRAMMING

Reference Divider Chain

The comparison frequency depends upon the crystal oscillator frequency and the division ratio of the R counter, which can be programmed in the range 3 to 2047.

$$R = \frac{fosc}{2 \times fcomp}$$

ie where *fcomp* = comparison frequency
fosc = oscillator frequency
R = R counter ratio

For example where crystal frequency = 10MHz and a channel spacing comparison frequency of 12.5kHz is required,

$$R = \frac{10^7}{2 \times 12.5 \times 10^3} = 400$$

Thus the R register would be programmed to 400 expressed in binary.
NB The total divider range is from 6 to 4094 in steps of 2.

VCO Divider Chain

The synthesised frequency of the voltage control oscillator (VCO) will depend on the division ratio of the M and A counters, the value of the external two modulus prescaler ($N/N + 1$) and the value of the comparison frequency *fcomp*.

The division ratio $P = NM + A$
where M is the ratio of the M counter in the range 3 to 1023 and *A* is the ratio of the A counter in the range 1 to 127
Note $M \geqslant A$

$$\text{Also } P = \frac{fvco}{fcomp}$$

For example if the desired VCO frequency = 275MHz, the comparison frequency is 12.5kHz and a two modulus prescaler of ÷64/65 is being used, then:

$$P = \frac{275 \times 10^6}{12.5 \times 10^3} = 22 \times 10^3$$

Now $P = NM + A$
which can be rearranged to be $P/N = M + A/N$
In our example we have

$$\frac{22 \times 10^3}{64} = M + \frac{A}{6} \text{ therefore } 343.75 = M + \frac{A}{64}$$

M is programmed to the integer part = 343 and *A* is programmed to the fractional part times 64
ie $A = 0.75 \times 64 = 48$
NB The minimum ratio that can be used is $N^2 - N$
To check $P = 343 \times 64 + 48 = 22000$ which is the required dividers ratio.

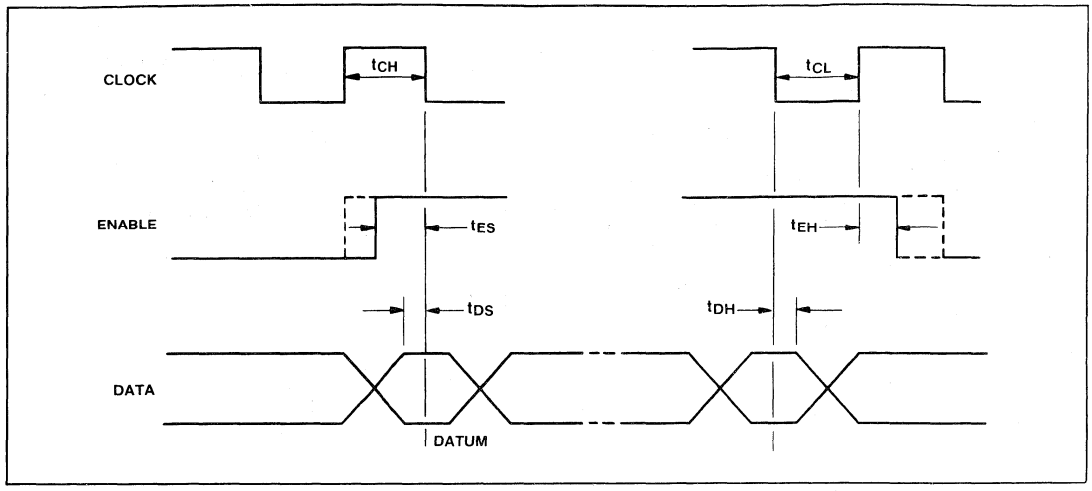


Fig.5 Timing diagram showing timing periods required for correct operation

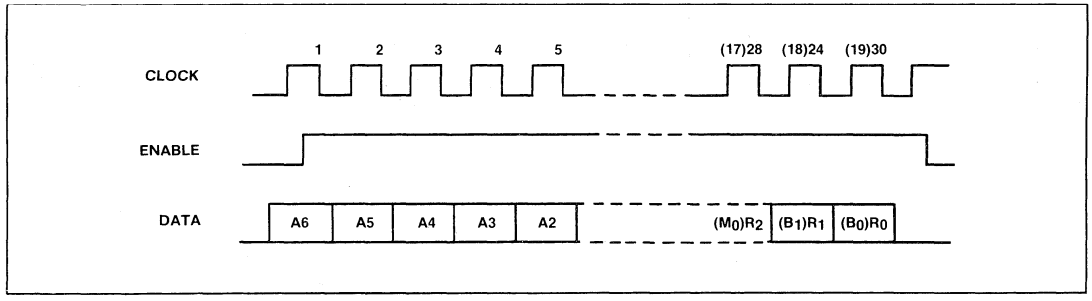


Fig.6 Timing diagram showing programming details

PHASE COMPARATORS

Noise output from a synthesiser loop is related to loop gain $K\Phi Kv/P$, where $K\Phi$ is phase detector constant (volts/rad), Kv is the VCO constant (rad-secs/volt) and P is the overall loop division ratio. When P is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase detector within the NJ88C25 has both a high gain and uses a double sampling technique to reduce spurious outputs to a low level.

A standard digital phase/frequency detetor driving a three-state output provides a 'coarse' error signal to enable fast switching between channels.

This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error.

The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB and a capacitor, CAP.

An internal 50pF capacitor is used in the sample and hold comparator.

The gain is typically

$$GAIN = \frac{10\ |V_{DD} - V_{SS} - 0.7 - 89(RB^{-1/2})|}{2\pi\ |CAP + 50 \times 10^{-12}| \times RB \times FR}$$

The value of RB and CAP should be chosen to give the required gain at the reference frequency used.

Fig.8 shows that to achieve a gain of 380V per radian at 10kHz requires RB to be approximately 39kΩ, CAP is zero. A hold capacitor (CH) of non-critical value which might be typically 470pF is connected from CH to V_{SS}. A smaller value is sufficient if the sideband performance required is not high.

The output from the sample/phase detector should be combined with that of the coarse phase/frequency detector and filtered to generate a single control voltage to drive the VCO.

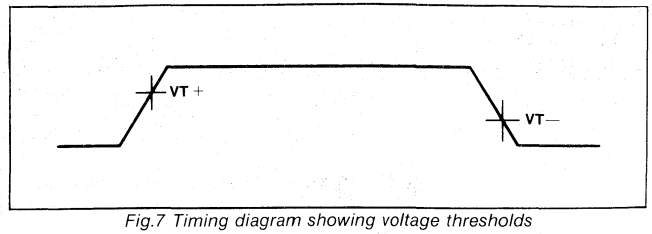
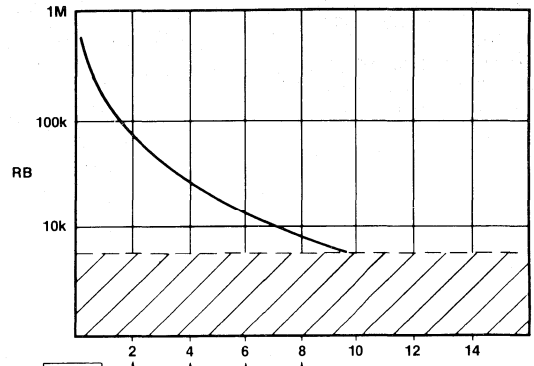


Fig.7 Timing diagram showing voltage thresholds



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320
	KΦ IN VOLTS/RAD.			

Fig.8 RB versus gain and reference frequency

NJ88C30

VHF SYNTHESISER

The NJ88C30 contains all the logic needed for a VHF PLL synthesiser and is fabricated on the Plessey high performance small geometry CMOS. The circuit contains a reference oscillator and divider, a two modulus prescaler and 4-bit control register, a 12-bit programmable divider, a phase comparator and the necessary data input and control logic.

FEATURES

- Low Power CMOS
- Easy to Use
- Low Cost
- Single Chip Synthesiser to VHF
- Lock Detect Output

APPLICATIONS

- Mobile Radios
- Hand Held Portable Radios
- Sonobuoys

ABSOLUTE MAXIMUM RATINGS

V_{DD}	-0.3V to +6V
Voltage on any pin	-0.3V to V_{DD} +0.3V
Operating temperature	-30°C to +70°C
Storage temperature	-55°C to +125°C

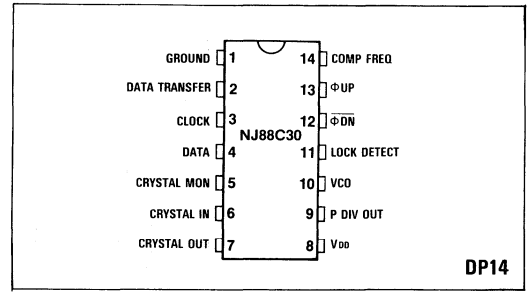


Fig.1 Pin connections (plastic DIL - top view)

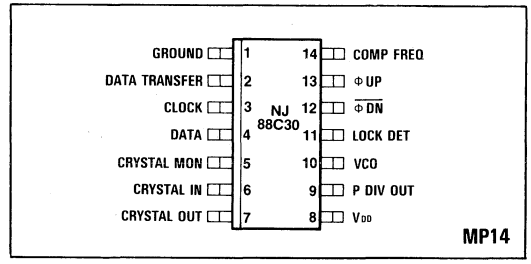


Fig.2 Pin connections (miniature plastic DIL - top view)

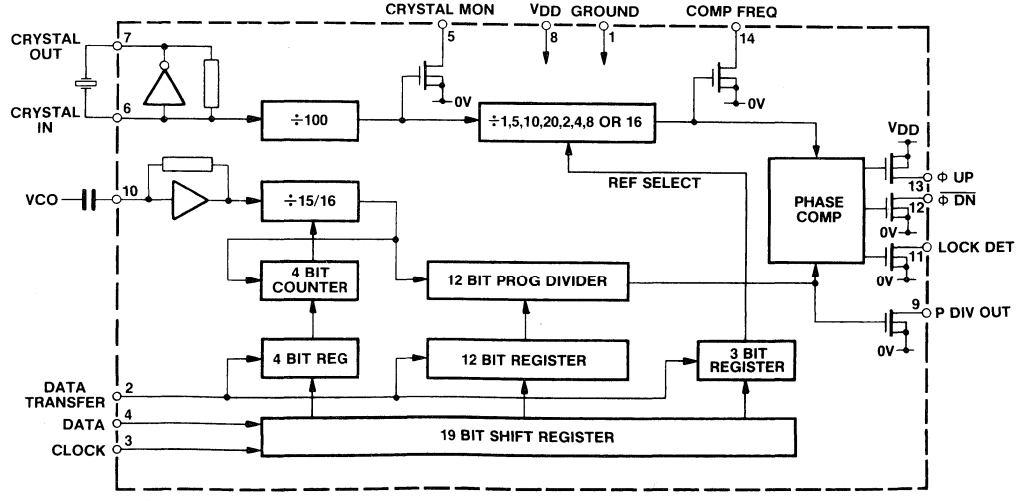
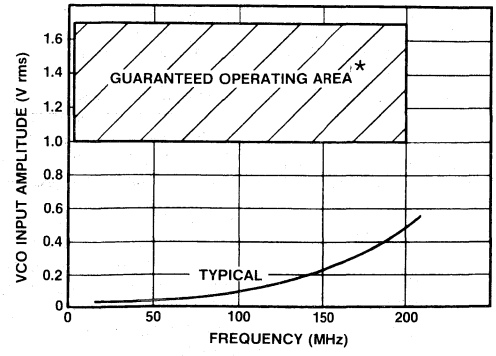


Fig.3 Functional block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -30°C to +70°C, V_{DD} = 5V ± 0.5V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply						
Supply current	8		4	7	mA	1V rms VCO input at 200MHz and f_{XTAL} = 10MHz
Crystal oscillator						
Frequency	6,7		10	15	MHz	Parallel resonant, fundamental crystal
External input level	6	1			V rms	AC coupled
High level	6	V_{DD}-1			V	DC coupled
Low level	6			1	V	DC coupled
VCO input						
VCO input sensitivity	10	1			V rms	At 200MHz, see Fig.4
Slew rate VCO input	10	4			V/μs	
VCO input impedance	10		5pF/10kΩ			
DATA, DATA TRANSFER, CLOCK inputs		V_{DD}-1				
High level	2,3,4				V	
Low level	2,3,4			1	V	
Rise, fall time	2,3			200	ns	
Data set up time	3,4	200			ns	See Fig.5
Clock frequency	3			2	MHz	
Transfer pulse width	2	500			ns	
Crystal monitor output						
Current sink	5	0.8			mA	V_{OUT} = 0.5V
Comp freq, LOCK DET, P DIV						
Current sink	9,11,14	1.6			mA	V_{OUT} = 0.5V
Φ UP/$\overline{\Phi}$ DN						
Current sink	12	0.8			mA	V_{OUT} = 0.5V
Current source	13	0.8			mA	V_{OUT} = V_{DD} - 0.5V



*Tested as specified in Table of Electrical Characteristics

Fig.4 Input sensitivity

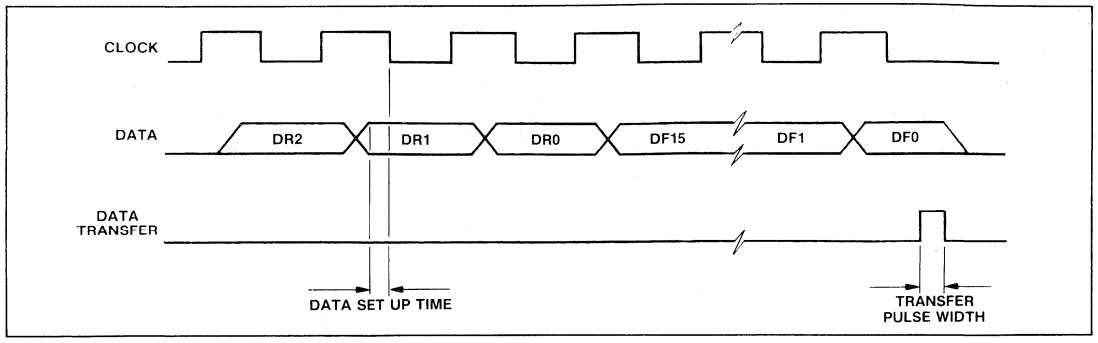


Fig.5 Input data timing diagram

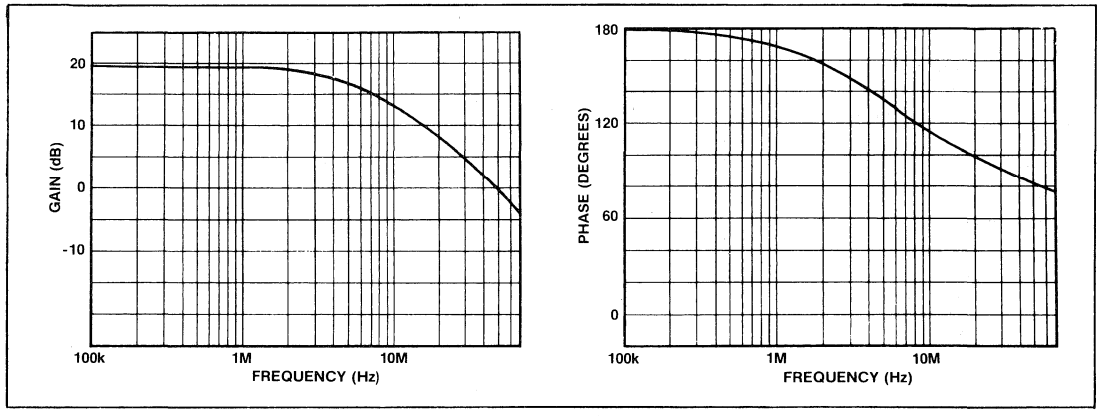


Fig.6 Gain phase characteristics of reference oscillator inverter

CIRCUIT DESCRIPTION

Crystal Oscillator and Reference Divider

The reference oscillator consists of a Pierce type oscillator intended for use with parallel resonant fundamental crystals. Typical gain and phase characteristics for the oscillator inverter are shown in Fig.6. An external reference oscillator may be used by either capacitively coupling a 1V rms sinewave into the CRYSTAL IN pin or if CMOS logic levels are available by connecting directly to CRYSTAL IN pin.

The reference oscillator drives a divider to produce a range of comparison frequencies which are selected by decoding the first three bits (DR2, DR1, DR0) of the input data. The possible division ratios and the comparison frequencies if a 10MHz crystal is used are shown in Fig.7.

DR2	DR1	DR0	Division Ratio	Comparison Frequency for 10MHz Ref. Osc.
0	0	0	1600	6.25kHz
0	0	1	800	12.5kHz
0	1	0	400	25kHz
0	1	1	200	50kHz
1	0	0	2000	5kHz
1	0	1	1000	10kHz
1	1	0	500	20kHz
1	1	1	100	100kHz

Fig.7 Reference divider division ratios

To assist in trimming the crystal, an open drain output at one hundredth of the reference oscillator frequency is provided on CRYSTAL MONITOR pin 1.

Programmable Divider

The programmable divider consits of a ÷15/16 two modulus prescaler with a 4-bit control register followed by a 12-bit programmable divider. A 1V rms sinewave should be capacitively coupled from the VCO to the divider input VCO pin.

The overall division ratio is selected by a single 16-bit word (DF 15 to 0) loaded through the serial data bus. A lower limit of 240 ensures correct prescaler operation; the upper limit is 65535. The VCO frequency in a locked system will be this division ratio multiplied by the comparison frequency.

Phase Comparator

The phase comparator consists of a digital type phase comparator with open drain Φ UP and $\overline{\Phi}$ DN outputs and an open drain lock detect output. Open drain outputs from the reference divider and programmable divider are provided for monitoring purposes or for use with an external phase comparator. Waveforms for all these outputs are shown in Fig.8. The duty cycle of Φ UP and $\overline{\Phi}$ DN versus phase difference are shown in Fig.9. The phase comparator is linear over a $\pm 2\pi$ range and if the phase gains or slips by more than 2π the phase comparator outputs repeat with a 2π period.

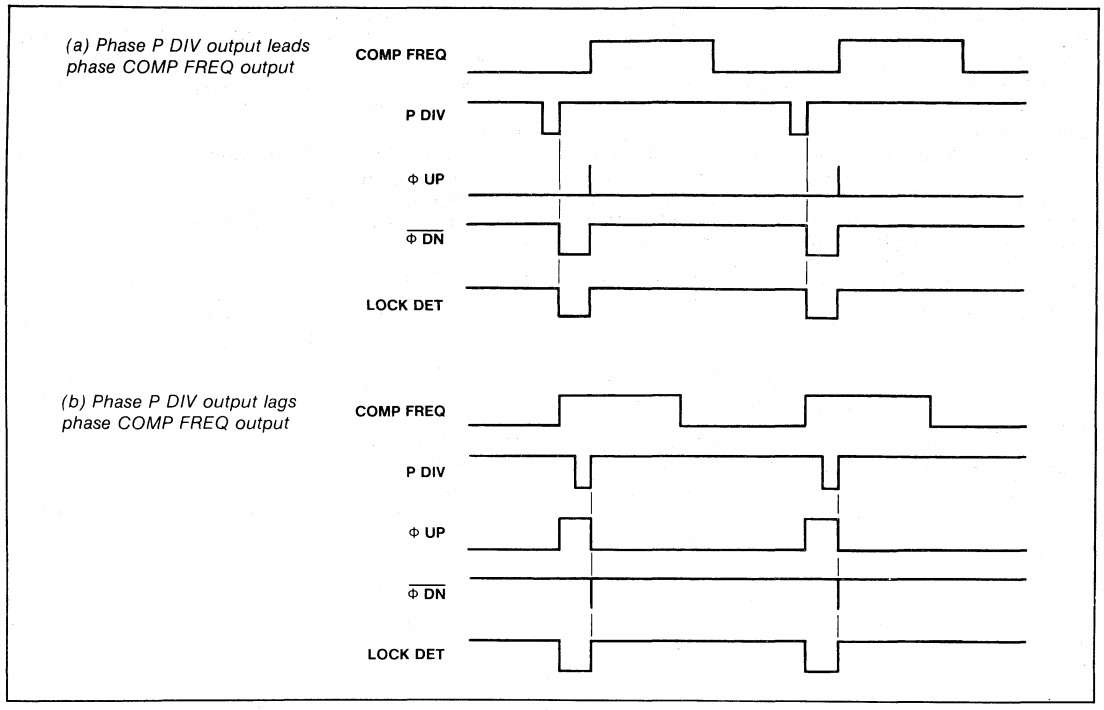


Fig.8 Phase comparator waveforms

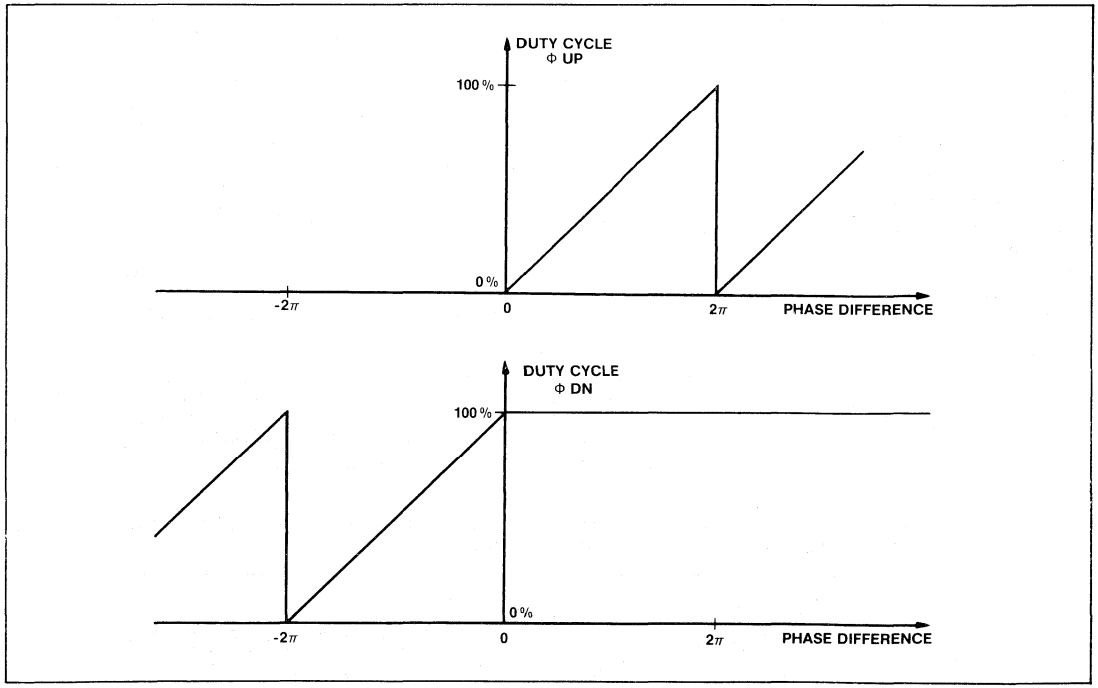


Fig.9 Phase comparator output characteristics

Once the phase difference exceeds 2π the comparator will gain or slip one cycle and then try to lock to the new zero phase difference. Note very narrow pulses may be seen on the inactive phase comparator output at the end of the pulse on the active output.

Data Input and Control Register

To control the synthesiser a simple three line serial input is used with Data, Clock and Data Transfer signals. The data consists of 19 bits, the first three DR2, DR1, DR0 control the reference divider, the next sixteen, DF15 to DF0, control the prescaler and programmable divider. Until the synthesiser receives the Data Transfer pulse it will use the previously loaded data; on receiving the pulse it will switch rapidly to the new data.

APPLICATIONS

A simplified circuit for a synthesiser intended for VHF broadcast receiver applications is shown in Fig.10. When the varicap line drive voltage necessary to tune the required band is greater than 5V, some form of level shifter such as the operational amplifier shown in Fig.10 is required. Pulses from the phase comparator are filtered by R_1, R_2 and C_1. Their values can be determined, given a required natural loop bandwidth ω_n and damping factor δ, by the following equations:

$$R_1C_1 = \frac{K}{\omega_{n^2}}, \quad R_2C_1 = \frac{2\delta}{\omega_n} \quad \text{and} \quad K = \frac{GK_0V_{CC}}{2\pi N}$$

where

ω - natural loop bandwidth (rad/s)
δ - damping factor
K_0 - VCO gain factor (rad/Vs)
V_{CC} - charge pump supply voltage (V)
N - division ratio = f_{OUT}/f_{COMP}
G - gain of amplifier

The values in Fig. 10 were calculated for:

ω_n = 3000 rad/s
δ = 0.707
K_0 = 18 Mrad/Vs
V_{CC} = 5V
f_{OUT} = 100MHz
f_{COMP} = 50kHz
G = 2

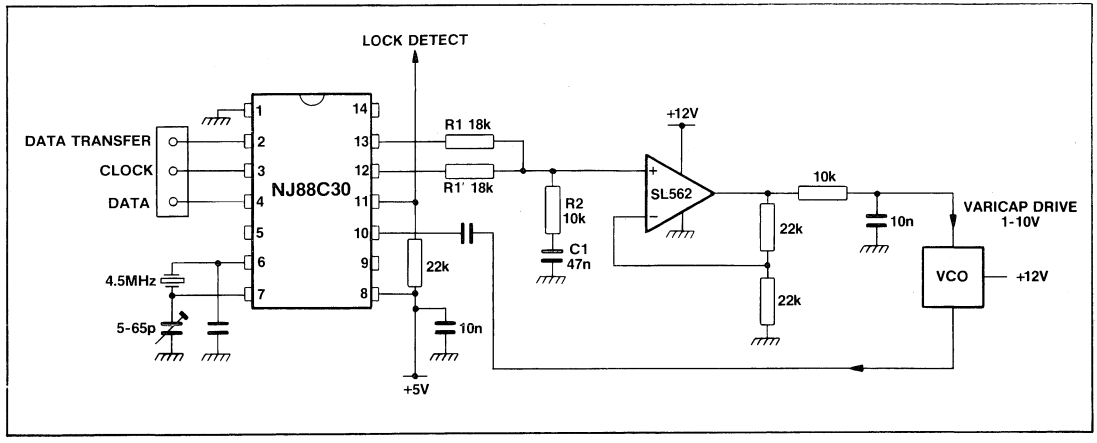


Fig.10 Typical application

Example of Programming

For a channel spacing (comparison frequency) of 5kHz when using a crystal oscillator of 10MHz the reference divider ratio will need to be 2000 (see Fig.7). This is programmed as binary 100 in the most significant three of the 19 bits (MSB programmed first).

To obtain the maximum VCO frequency of 200MHz the programmable divider ratio would be:

$$\frac{200 \times 10^6}{5 \times 10^3} = 40 \times 10^3 \text{ which is 9C40 Hex.}$$

The complete program word would then be:

	DR			DF															
	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	1	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0
Hex	4			9				C				4				0			

Using the same crystal and 5kHz channel spacing the minimum VCO frequency programmable would be 1.2MHz with the division ratio of 240 (= F0 Hex). The program word would then be:

	DR			DF															
	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0
Hex	4			0				0				F				0			

PLESSEY
Semiconductors

ADVANCE INFORMATION

NJ88C33

FREQUENCY SYNTHESISER (I²C BUS PROGRA[illegible]E) WITH CURRENT SOURCE PHASE DETECTOR

The NJ88C33 is a synthesiser circuit fabricated on the Plessey 1.4 micron CMOS process assuring very high performance. It is I²C compatible but can be programmed at up to 2MHz. It contains a 16-bit R counter, 12-bit N counter and a 7-bit A counter.

A digital phase comparator gives improved loop stability with current source outputs to reduce loop components. A voltage doubler is provided for use with the phase detector.

FEATURES

- Low Power Consumption
- Digital Phase Comparator
- Serial (I²C Compatible) Programming
- 100MHz Input Frequency at 5V (40MHz at 3V)
- Standby Mode
- Use of Prescaler is Optional

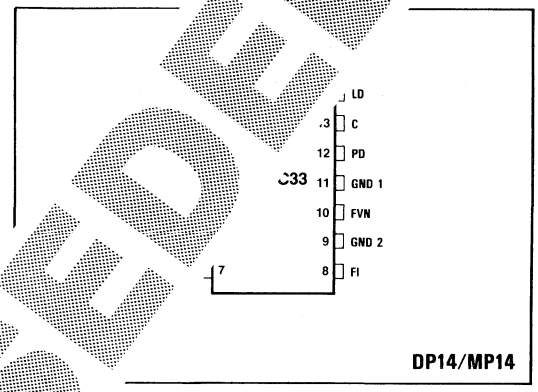


Fig.1 Pin connections - top view

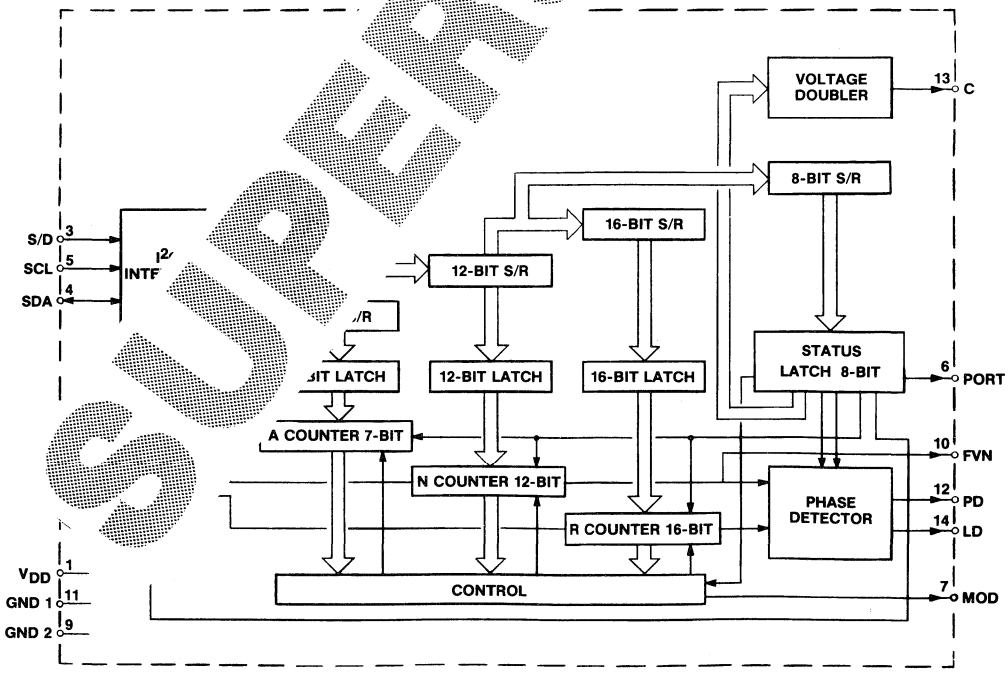


Fig.2 Functional block diagram

Application Notes

SL2365 Applications

The SL2365 is an array of transistors configured to form a dual long-tailed pair with tail transistors which are current mirrored to similar transistors whose bases and collectors are connected internally.

The ICs are manufactured on a very high speed bipolar process which has a typical f_T of 5GHz. The device is available in a surface mounted DIL package (MP14), the pin connections of which are shown below.

Various applications are described including a 900MHz amplifier, a frequency doubler, a frequency tripler and a single balanced mixer.

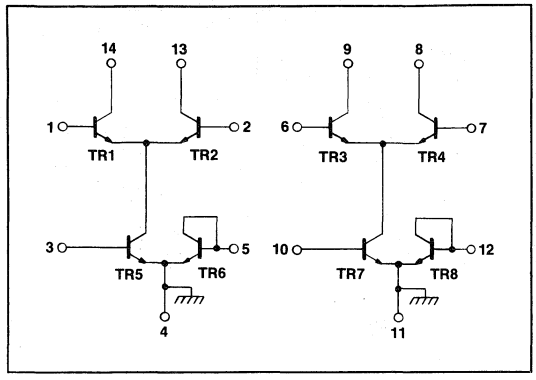


Fig.1 SL2365 schematic diagram

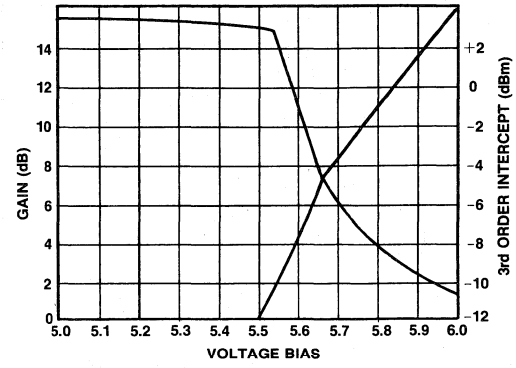


Fig.3 3rd order intercept at gain of 12.5dB (using current mirror at 4mA) = -7dBm

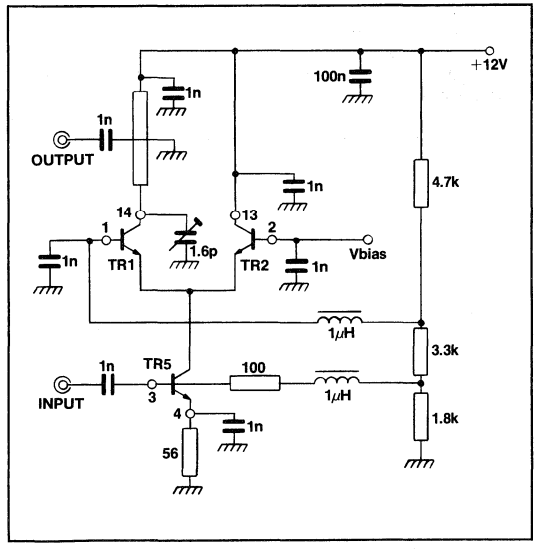


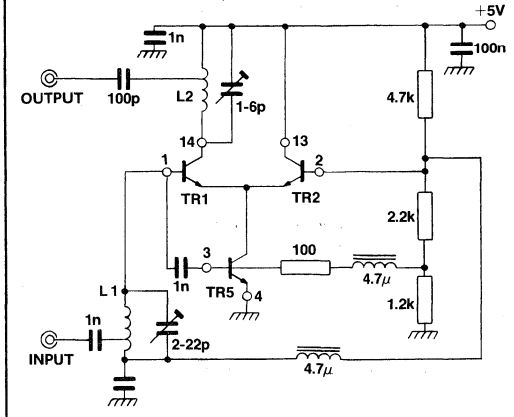
Fig.2

A 900MHz GAIN CONTROLLED AMPLIFIER

In Fig.2, the collector load of TR1 is a transformer composed of a 14mm length of 75Ω stripline resonated with a 1-6pF variable capacitor. The secondary of the transformer is a small loop of stiff wire grounded at one end and located a few mm above the stripline. The gain and 3rd order intercept versus V bias is shown in Fig.3. The noise figure at full gain is 9dB.

A 150-300MHz FREQUENCY DOUBLER

The frequency doubler, Fig.4, has a gain of +1dB for a -20dB input and input frequency rejection of 18dB.

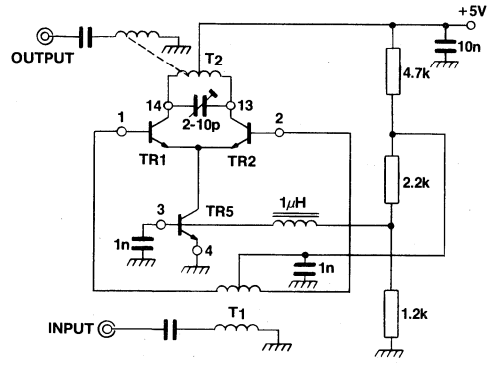


NOTES
L_1 = 4 turns 20 swg tinned wire 5mm diameter. Tapped 1 turn from ground end
L_2 = 3 turns 20 swg tinned wire 5mm diameter. Tapped 1 turn from 5V rail end

Fig.4

A 100-300MHz FREQUENCY TRIPLER

Fig.5 shows a 100-300MHz frequency tripler with a gain of -40dB, input frequency rejection of 30dB and second harmonic rejection of 28dB.

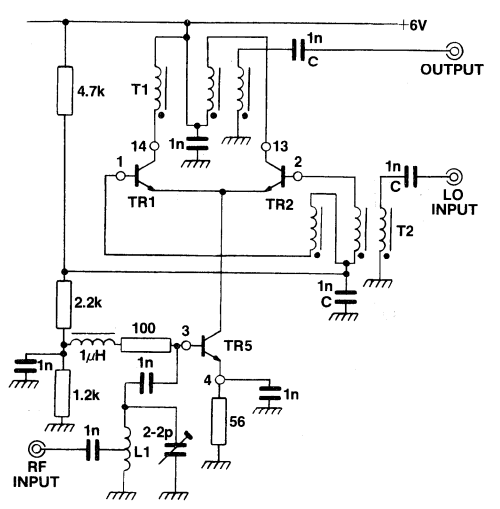


NOTES
T_1 Primary = 4 turns 36 swg enamelled wire wound on ferrite core
T_1 Secondary = 4 turns 36 swg enamelled wire wound on LF ferrite core (twisted pair)
T_2 Primary = 2 turns 20 swg tinned wire 5mm diameter
T_2 Secondary = 4 turns 20 swg tinned wire 5mm diameter, positioned axially relative to T_2 Primary

Fig.5

A SINGLE BALANCED MIXER

The mixer of Fig.6 has a gain of 13dB, 3rd order intercept = -13dBm. -10dBm (using 2mA in current mirror) and noise figure = 10dB.



NOTES
L_1 = 4 turns 20 swg tinned wire 5mm diameter. Tapped 1 turn from ground end
T_1 and T_2 = 4 turns of trifilar wound 36 swg enamelled wire wound on LF ferrite core

Fig.6

Radio Synthesiser Circuits
Loop Filter Design

LOOP BANDWIDTH

An important choice in the design of the Phase Locked Loop is the Loop Bandwidth. This determines parameters such as lock up time, noise and modulation capability, and generally is made as wide as possible in single loop synthesisers. There are conflicting requirements however, and single loop synthesisers are not always practicable - Refs. 1, 2.

The NJ8820 series use two phase detectors, a digital 'steering' detector and an analog high gain linear detector. This latter detector is a sample-and-hold type in which an internal 50pF capacitor is discharged at a constant current. This current is set by the gain programming resistor *RB*, and the voltage on the capacitor is sampled at the reference frequency. Thus the gain of the detector is fixed by the time available for the capacitor to be discharged. If the discharge current was constant, the phase detector would have a gain directly proportional to frequency and current, but the departure from constant current gives a correcting factor, and the gain is thus:

$$K\Phi = 10\ \frac{[V_{SUPPLY} - 0.7 - 89\ (RB)^{-\frac{1}{2}}]}{[2\pi \times (50 \times 10^{12} + CAP) \times RB \times FR]} \quad ...(1)$$

where *RB* is the gain programming resistor and *FR* is the phase comparison frequency. The value of *CAP* is 0 for the NJ8820/1 and is fixed externally in the NJ8822.

The analog phase comparator has a very high gain and so can only operate over a narrow phase range. This phase window is given by:

$$\Delta\Phi = 4.5/K\Phi \text{ radian}$$

where $K\Phi$ is the phase detector constant (volts/radian).

When the analog phase detector is outside this range, the digital detector operates to provide steering. Inside the analog detector phase range, the digital output is in its 'Tri-State' high impedance condition.

The 2nd order analog loop has a bandwidth and damping factor given by:

$$\omega_n = \sqrt{\frac{K\Phi K_V}{NR_2C}} \quad ...(6)$$

$$D = \frac{R_3C}{2} \cdot \omega_n \quad ...(7)$$

If the loop is slewed at too high a rate by the digital output, then a longer lock up time may result because of overshoot; in extreme cases, the loop will become unstable, because the VCO frequency will sweep too quickly.

$$CR_2 = \frac{2\pi\ K\Phi K_V}{\omega_n^2 N} \quad ...(8)$$

$$\frac{R_2}{R_3} = \frac{\pi\ K\Phi K_V}{DN\omega_n} \quad ...(9)$$

$$R_1 \geqslant 5R_2\ \frac{2D}{\omega_n} + 1 \quad ...(10)$$

where ω_n = loop bandwidth in rads/sec
$K\Phi$ = analog phase detector gain in volts/rad
K_V = VCO sensitivity in Hz/volt
D = loop damping factor
N = divide ratio

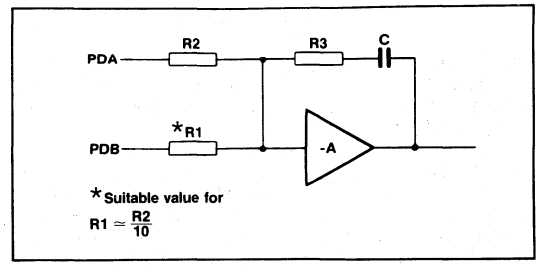


Fig.1 Augmenting integrator for loop filter

VCO Noise

Phase noise of the VCO inside the loop bandwidth will be reduced by the loop, while outside the loop bandwidth it will be unaltered. The phase noise of the reference oscillator will add to the VCO noise at frequencies inside the loop bandwidth and this effect also influences the choice of loop bandwidth. For example, a loop with a 5kHz loop bandwidth operating at 900MHz with a reasonable 5MHz crystal oscillator noise floor (-125dBc/Hz at 1kHz oscillator) would have a noise power of some -80dBc/Hz at 1kHz offset at final frequency. For a further discussion of phase noise and other compromises see Ref. 2.

Where a high phase detector gain is used with a noisy oscillator, or with a high value of K_V, it may well happen that the analog phase detector is driven outside the phase window. This will lead to the digital output becoming active, and instability is likely to result.

Modulation Techniques

Modulation of the PLL may take place inside or outside the loops bandwidth. Modulation outside the loop bandwidth requires the loop bandwidth to be less than the lowest modulating frequency, and the amount of modulation will vary over the frequency range as K_V, the VCO constant varies.

Various techniques may be used to minimise the variation in modulation sensitivity, and probably the easiest in the use of a separate modulation diode. The variation in capacitance is very small for normal NBFM variations and thus the deviation may well remain sensibly constant over a wide range, e.g. +0.75kHz for 5kHz nominal deviation over an 18MHz range at VHF.

Modulation outside the loop bandwidth leads to a signal appearing at the phase detector output corresponding to the phase error between reference frequency and the divided VCO. Should this phase error be such as to lead to the phase detector being driven outside its phase window, then problems may occur, with reference frequency sidebands appearing and possibly even unlocking of the loop.

Avoidance of this condition may be achieved by limiting the phase deviation at the detector such that detector is operating within its linear range. For devices with programmable phase detector gain, such as NJ8820 series, this may be achieved by using a low gain and high deviation ratio.

Modulation index, m, is given by:

$$m = \frac{\text{frequency deviation}}{\text{modulating frequency}} \quad ...(20)$$

For a modulation index of 1 at the VCO, the phase variation is 1 radian. Thus an NBFM transmitter with a deviation of 2.5kHz and modulation frequency of 500Hz has a phase deviation of 5 radians.

In a 25kHz channelled system at 30MHz, the deviation at the detector would be 5/1200 rads or 0.24 degrees. Attempting to operate the NJ8820 at 800 volts/rad would give problems because of limiting in the analog phase detector.

Modulation inside the loop bandwidth avoids this problem, but care must be taken to ensure that the reference frequency sidebands do not become appreciable. In addition, the wideband noise of the phase detector and loop filter can cause problems when K_V, the oscillator constant in MHz/volt, is high.

Modulation of the reference oscillator is another possible technique of modulating inside the loop bandwidth. However, all modulation inside the loop bandwidth produces phase rather than frequency modulation and there are, in addition, limits on the frequency deviation and modulation frequency that can be accepted without the loop becoming unlocked. Generally, the modulation frequency must be much less than the loop bandwidth. Gardner (Ref.4) has derived the equation:

$$\Delta\omega = \frac{\omega_n^2}{\omega_m} \quad ...(21)$$

where $\Delta\omega$ = frequency deviation
ω_n = loop natural frequency (bandwidth)
ω_m = modulating frequency

This equation is only valid for $\omega_m \ll \omega_n$

In general, modulation outside the loop bandwidth is used, because the required bandwidth is greater than the reference frequency. The loop bandwidth is usually 1/5 and 1/10 of the lower modulating frequency.

Note that modulation applied such that

$$\frac{\Delta\omega}{dt} \geqslant \frac{K_\Phi K_V}{R2C} \quad ...(22)$$

will cause the loop to unlock.

In addition, modulation such that the analog phase detector limits is not advisable. This will occur when

$$\Delta_\Phi \geqslant 4.5N/K_\Phi \text{ rads} \quad ...(23)$$

Δ_Φ is equivalent to m, the modulation index: when $m = 1$, $\Delta_\Phi = 1$ radian.

Thus, a synthesiser operating at 145MHz with a 25kHz comparison frequency and a modulation index of 30 for the lowest modulating frequencies would need K_Φ to be less than 870 volts/rad. Operation at lower frequencies are used. However, large amounts of LF phase noise can have appreciable phase deviations and thus low noise oscillators should be used.

Noise from the amplifier used in the loop filter should be minimised: the use of a low noise amplifier such as a Plessey SL562 is suggested. Filtering after the amplifier, such as in Fig.2, is advisable to minimise the noise modulation of the VCO, but care should be taken to ensure that the added phase shift does not cause the loop to become unstable.

Loop Stability

Calculation of loop stability may be carried out in a number of ways. It has been claimed (Ref.4) that a true 2nd order PLL does not exist because of strays. In addition, an extra section (at least) of RC filtering is generally required to minimise the effects of noise in the operational amplifier. Various computer programs exist in which such analysis can be undertaken, but it is possible to evaluate loop stability in a relatively easy manner using a programmable calculator.

For a 2nd order loop such as Fig.2, it may be shown that the transfer function is

$$\frac{AoK_\Phi K_V}{N\omega} \cdot \frac{j\omega T2 + 1}{j(1-\omega^2 E) - \omega(F - \omega^2 D)} \quad ...(24)$$

where $D = T3To(T1 + T2)$
$E = T3(Ao\,T1 + To + T1 + T2) + To(T1 + T2)$
$F = Ao\,T1 + To + T1 + T2 + T3$

and Ao, K_Φ, K_V, N, ω, have the previously assigned definitions.

Ao = open loop amplifier gain
To = $1/fo$, amplifier open loop 3dB bandwidth
$T1$ = $R2C1$
$T2$ = $R3C1$
$T3$ = $R4C2$

The finite modulation bandwidth of the VCO is ignored in this analysis.

Evaluating the equation (24) in terms of gain and angle ($r\angle\theta$) at various frequencies allows the stability to be evaluated. An example of a frequency synthesiser design is given in the following section, where Table 1 lists a suitable program for Hewlett Packard Calculators using Reverse Polish Notation.

Frequency Synthesiser Design

A frequency synthesiser is required for a transmitter covering 144-148MHz. the supply voltage for the synthesiser is 10 volts, pre-emphasised frequency modulation is required with an upper limit of 3kHz, adjacent channel noise is required to be -70dB at 12.5kHz channel spacing and a 'lock-up' time of 25ms is required.

12.5kHz channel spacing systems use an IF bandwidth of 7.5kHz, which gives approximately 39dB more noise than a 1Hz bandwidth. Thus the VCO for this synthesiser must have a phase noise characteristic of -109dBc/Hz at 12.5kHz (see Ref.1) and from Refs. 2 and 3 this may be shown to be practical with a single loop synthesiser using a narrow bandwidth.

The choice of prescaler should be made from a consideration of programming - see the relevant data sheet.

The lowest modulation frequency is 300Hz and the transmitter will attenuate components below this frequency at 12dB/octave or more. Standard pre-emphasis rises at 6dB/octave from 300Hz to 2700Hz: thus the deviation at 300Hz is approximately 18dB down on that at 2.7kHz and at 50Hz will be about -45dB. With a deviation at 2.7kHz of 2.5kHz, the deviation at 50Hz will be about 15Hz.

At 144MHz, the divide ratio is 145000/12.5 = 11600. Thus the 15Hz deviation it caused by the 50Hz modulation becomes

$$15/50 \times 1/11600$$

radians at the phase detector, which is negligible. Thus the analog phase detetor will operate inside its window at low frequencies. Even at 300Hz where the modulation index is 8.33, the phase deviation at the phase detector is only 0.041 degrees.

Since a 10V supply is available, a VCO control line swing of 8 volts may be assumed. Allowing overlap, the VCO will cover 143-149MHz, giving K_V (the VCO constant) as 0.75MHz/volt. This gives a residual deviation caused by the phase detector noise of about 0.75Hz.

A loop bandwidth of 50Hz is well below the lowest modulating frequency and values may be readily calculated. K_Φ, the phase detector gain, is an independent variable; a reasonable mid-range value of 320 volts/rad gives a phase window of 0.89 degrees.

From these constants, values of $R1$, $R2$, $R3$ and C in Fig.1 may be calculated.

$$CR2 = \frac{2\pi K_\Phi K_V}{\omega_n^2 N} \quad ...(25)$$

$$\frac{R2}{R3} = \frac{\pi K_\Phi K_V}{DN\omega_n} \quad ...(26)$$

$$R1 \text{ min} = \frac{6R2}{K_\Phi} \quad ...(27)$$

Thus, at the mid-band frequency of 146MHz, where N = 11680:

$$CR2 = \frac{2\pi \times 320 \times 0.75 \times 10^6}{(2\pi \times 50)^2 \times 11680} = 1.3 \quad ...(28)$$

$$\frac{R2}{R3} = \frac{\pi \times 320 \times 0.75 \times 10^6}{0.7 \times 11680 \times 2\pi \times 50} = 293 \quad ...(29)$$

$$R1 \geqslant \frac{5R2}{K_\Phi}\left(\frac{2D}{\omega_n}\right) + 1 \quad ...(30)$$

The use of high values of resistance leads to greater noise generation in the loop filter because of KTB noise, while low values lead to larger current swings, which can give slew rate limiting in the op-amp. If $R3$ is set to 2200Ω, thus preventing slew rate limiting,

$R2$ = 664kΩ (use 680kΩ)
$C1$ = 1.9μF (use 2.2μF)

From these standard values

$$\omega_n = \sqrt{\frac{K_\Phi K_V}{NCR2}} = 293.3 \text{rads/sec} \equiv 46.7\text{Hz} \quad ...(31)$$

$$\text{and } D = \frac{R3C}{2} \cdot \omega_n = 0.71$$

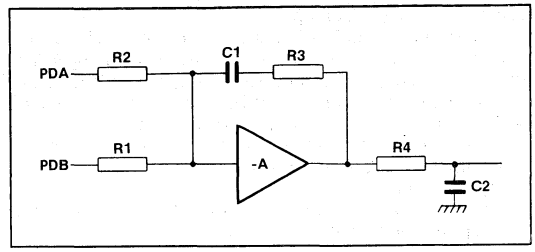


Fig.2 Augmenting integrator amplifier with filtering

$$R1 \text{ min} = \left(\frac{5 \times 680k\Omega}{320}\right)\left(\frac{2 \times 0.71}{2\pi \times 46.7} + 1\right) = 10.7k\Omega \quad ...(32)$$

(use 12kΩ or 15kΩ).

A further section of filtering may be added as in Fig.2, and the cut-off frequency may be arbitrarily set at 500Hz. Again, a reasonable compromise is required on CR values for the same reasons. The added filter section reduces noise from the op-amp and resistors, and so is a useful addition.

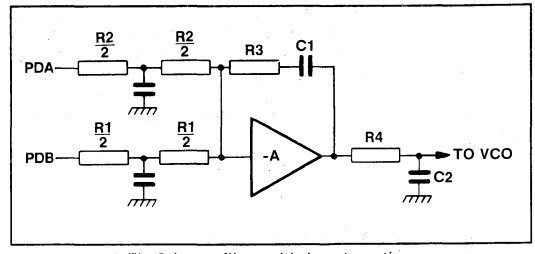


Fig.3 Loop filter with input sections

In cases where the operational amplifier 'locks up' because of overdrive, the circuit of Fig.3 may be used, often with success. The time constants $C3R2/2$ should be about $10/fn$ where fn is the loop bandwidth. It should be noted that the capacitor $C1$ *must* be of the non-polarised variety, as the voltage across it can reverse. Similarly, the external capacitor provided in the phase detector of the NJ8820 should be a low leakage type, such as polystyrene: ceramic capacitors are not generally good enough.

Bypassing the gain setting resistor of the NJ8820 series with a large capacitor may reduce noise derived from this resistor.

Multimodulus Division

Phase Locked Loop Frequency Synthesisers of the form shown in Fig.4 suffer from the problems inherent in producing fully programmable dividers required to operate at appreciable frequencies while not consuming excessive power. Although advances in small geometry integrated circuit technology make any figures obsolete, guaranteed operation above about 50MHz requires relatively high power.

The use of fixed prescaling, as in Fig.5, is widely used, but for a division ratio of N in the prescaler and a channel spacing of f kHz, the phase comparison frequency of Fig.4 has been reduced by the factor f/N. This lower frequency necessitates a lower bandwidth in the phase locked loop, and thus a greater susceptibility to microphonics etc., and, generally speaking, a longer lock up time.

The alternatives to fixed division are mixing, as in Fig.6 or 'multimodulus division' ('pulse swallowing') as in Fig.7. The use of mixers requires great care in the choice of frequencies if spurious products are not to be a problem and although widely used, is certainly more complicated than multimodulus division in terms of its physical realisation, requirements for 'adjust-on-test' parts, and its susceptibility to layout problems.

The multimodulus divider system is shown in Fig.7. It is built up from a number of blocks:

1. A two-modulus divider which will divide by one of two numbers N or $N + 1$ (e.g., 10/11, 64/65 etc.).

2. An A counter which is programmable and the output of which controls the modulus of the divider.

3. An M counter which is programmable, is clocked in parallel with the A counter, and the output of which resets both itself and the A counter.

The counters may count 'down' to zero from the programmed input, or count 'up' from zero.

The principle of operation is as follows:

The A counter is programmed to a smaller number than the M counter and assuming the counters to be empty, the system starts with the divider $(N/N + 1)$ dividing by $N + 1$. This continues until the A counter reaches its programmed value, whereupon the divider divides by N until the M counter is full. As the M counter has received A pulses, this counter overflows after (M - A) pulses, corresponding to $N(M - A)$ input pulses to the divider. Thus the total division ratio P is given by:

$$P = (N + 1)A + N(M - A)$$
$$= NM + A$$

Obviously, A must be equal to or less than M for the system to work, while for every possible channel to be available, the minimum total divide ratio is $N(N - 1)$ while the maximum total divide ratio is $M(N + 1)$. A_{max} should be equal to or greater than N.

Although deceptively simple in theory, there are a few points which require consideration in the design of such a divider system. Of these probably the most important is Loop Delay.

Consider the counter chain at the instant that the $(N + 1)$th pulse appears at the two modulus divider input. After some time $tp1$ the output produces a pulse, which clocks the A and M counters. Assume that the A counter is filled by the pulse, and so after a time $tp2$ (determined by the propagation delay of the A counter) an output is produced to set the dual modulus divider ratio to N. After a set-up time ts, the dual modulus divider will divide by N. But if $tp1 + tp2 + ts$ is greater than N cycles of input frequency, the divider will not be set to divide by N until after N pulses have appeared, and the system will fail. Thus

$$\frac{N}{fin} > \text{total loop delay}$$

Design in this region is critical: worst case tolerances *MUST* be used if the reproducibility and reliability of the design under temperature and voltage extremes is not to be compromised.

The value of N must also be large enough that the output frequency from the divider does not exceed the maximum input frequency of the following circuitry. In single chip MOS controllers, this may well be as high as 50MHz under some conditions, but under others, such as high temperature and low voltage, much lower. Generally, however, the limitation on such circuits is the loop delay rather than input frequency.

The loop delay is affected by the edge of the waveform on which the divider and the A and M counters trigger. If the edges are opposite then the loop delay may be increased by large amount, and if in these circumstances, the use of an inverter at the output of the divider is justified.

The minimum value of N is therefore settled by these constraints, but the actual choice of N may be determined by the ease of programming. This may be seen by considering a synthesiser with a 25kHz phase comparison frequency and 25kHz channelling, using a 40/41 divider.

At 156MHz:

$$P = \frac{156}{0.025} = 6240$$

therefore $NM + A = 6240$
therefore $40M + 0 = 6240$ ($A = 0$ for the lowest channel)
therefore $M = 156$

In general, where

$$fN = 1 \text{ or } 10 \text{ or } 100$$

$$M = f, \frac{f}{10}, \frac{f}{100} \text{ etc.}$$

and similarly for binary divide ratios.

The choice of prescaler is therefore fixed by

1. Total allowable loop delay.

$$\frac{N}{fin} > \text{controller delays}$$

2. Output frequency within the controller input frequency band.

3. Programming ease.

REFERENCE FREQUENCY DIVISION RATIO (R)

The value of R is set by the input frequency and the phase comparison frequency. Higher input frequencies require greater power and offer lower stability, while lower frequencies (below 4MHz) generally require larger physical crystal case sizes. Normally, a frequency between 4 and 10.7MHz is used, especially as in double conversion equipments commonality of oscillators may be possible.
e.g. for a 2.5kHz comparison frequency and 10.245MHz 2nd local oscillator frequency,

$$R = \frac{10.245 \times 10^6}{2.5 \times 10^3} = 4098$$

Note that R is *always* an even number.

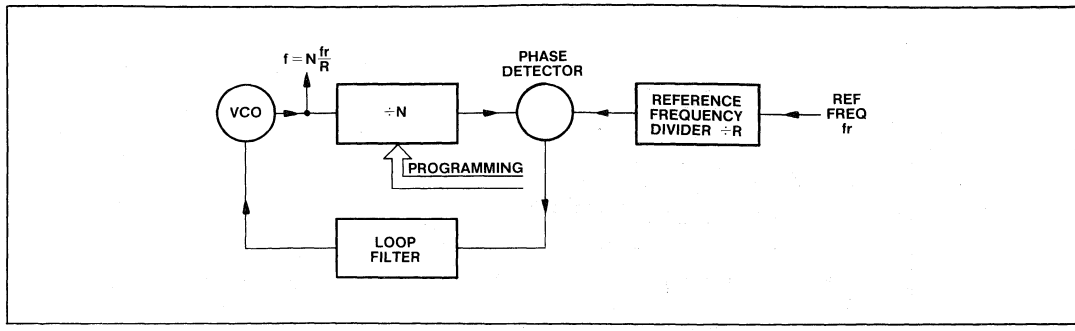


Fig.4 Direct division

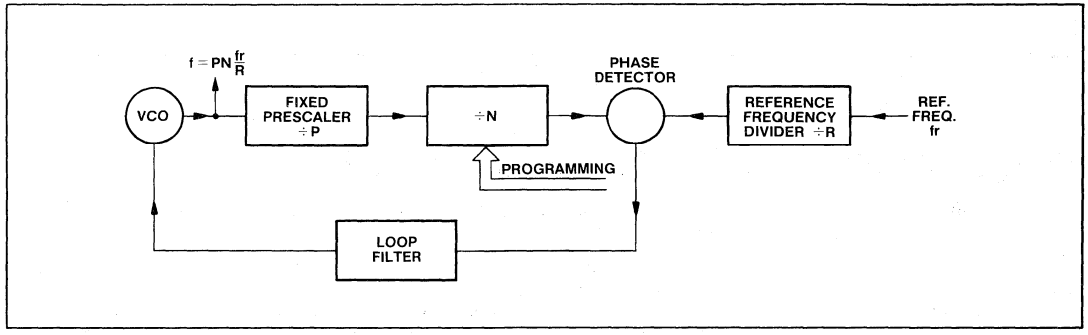


Fig.5 Fixed prescaling

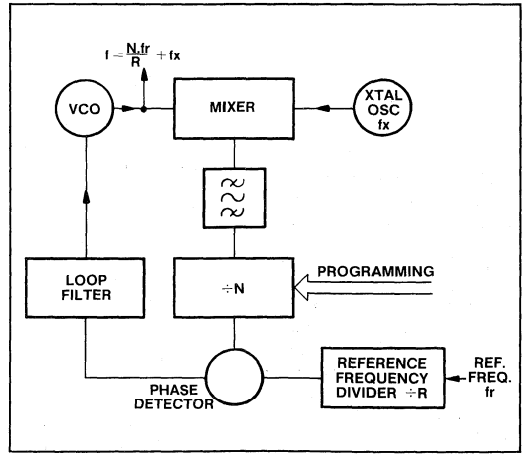


Fig.6 Mixing in the loop

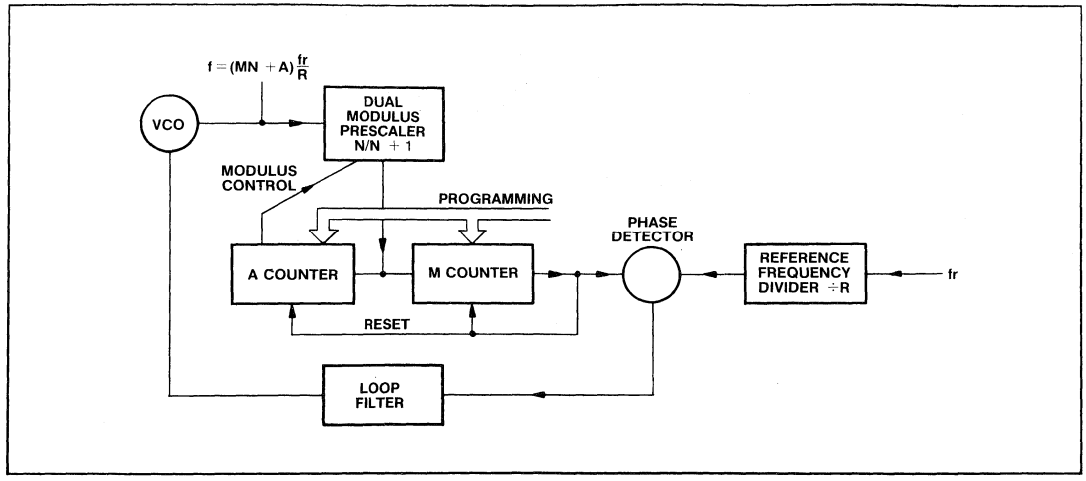


Fig.7 Dual modulus prescaling

Programming the NJ8820 and NJ8821/23

The NJ8820 and NJ8821/23 are versatile high performance CMOS frequency synthesiser controllers. The differences between devices lies in hardware programming methods.

The basic system of a single loop frequency synthesiser is shown in Fig.8, where a 2-modulus prescaler is used to divide the VCO frequency down to a suitable range for use in the CMOS device. The NJ8820/1/3 is programmed by 8 of 4 bit words on the data inputs: the addresses for these words may be obtained internally or externally and appear on the Data Select inputs/outputs. To program any frequency, it is necessary to program the *A* counter, the *M* counter and the reference or *R* counter: these counters are respectively, 7, 10, and 11 bits long.

ADDRESSING

Addressing is by one of three modes: These are:

A. Self Programming Internal Mode

Here the reference oscillator (either an internal crystal oscillator or from an external source) signal is divided in the reference counter by 64 and a DATA READ cycle commences every 1024/fosc seconds.

In this DATA READ cycle, the MEMORY ENABLE pin is pulled low, and the DATA SELECT outputs DS0, 1 and 2 count in binary from 0 to 7. This provides addresses for the DATA on D0, 1, 2 and 3, the data being transferred to internal latches on the trailing edge of the DATA SELECT pulses -see Fig.9. Note that the Program Clock is internally derived and is at a frequency of fosc/64. The PE (Program enable) pin is grounded, and the cycle continuously repeats. This mode is not recommended, as noise may be picked up by the phase locked loop.

B. Single Shot Internal Mode

In this mode, the PE pin is provided with a pulse input. This pulse initiates a data read cycle as outlined above, and at the end of the cycle, the ME (Memory Enable - NJ8820 and NJ8820HG only) pin goes high and thus system power consumption is minimised. 'Power-on' initiation is used, in which the application of power to the device is sensed and a programming cycle initiated. In order to avoid corruption of the data, a delay of 53248 cycles of reference oscillator frequency is provided before the programming cycle occurs. This delay is approximately 5ms for a 10MHz reference frequency.

C. External Mode

The address is presented to DS0, 1 and 2, and a pulse is applied to the PE pin to transfer data to the internal latches. The data is transferred from the latches to the counters simultaneously with the transfer of data into Latch 1: thus this word should be the last one entered.

WORD VALUES

For any particular set of conditions, viz operating frequency, prescaler ratio, comparison frequency and input frequency from the reference oscillator, a unique set of programming words exist.

Reference Divider

This divider produces the comparison frequency required by the synthesiser. It is programmable from 6 to 4094 in steps of 2. The division ratio is twice the programmed number. Therefore, if for example a 10MHz crystal is used, and a 12.5kHz reference required, this counter would be programmed to give a ratio of 100000/12.5 = 800. The actual programming would then be 400, which would be entered in binary according to the data map, Table 3.

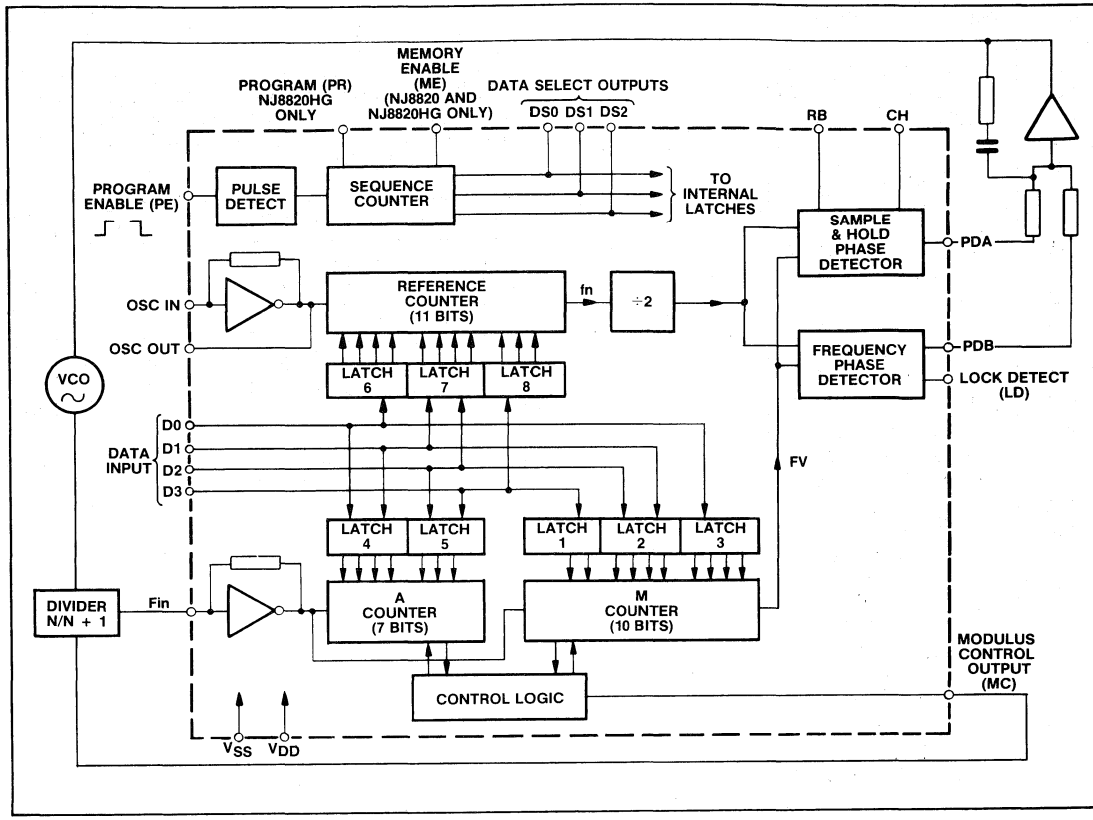


Fig.8 The phase lock loop

A and N Dividers

The *A* counter is a 7-bit counter and the *M* counter is a 10-bit counter. The programming calculations are as follows:

1. The *A* counter should contain *x* bits such that $2^x = M$.

2. If more bits are included in the *A* counter, these should be programmed to zero.

e.g. $M = 64 = 6$ bits
$A = 10$ bits
then the 4 MSB are programmed to zero.

3. The *M* and *A* counters are treated as being combined so that the MSB of the *M* counter is the MSB of the total and LSB of the *A* counter is the LSB of the total.

e.g. A synthesiser operating from 430-440MHz in 25kHz steps uses a 64/65 divider, and the control circuit uses binary counters.
P = f/fref and fref = channel spacing = 25kHz
$Pmin = 430/0.025 = 17200$
$Pmax = 440/0.025 = 17600$

Minimum possible divide ratio is $N^2 - N = 4032$
where N is two modulus divider ratio

$$\text{maximum allowable loop delay} = \frac{64}{440 \times 106} = 145\text{ns}$$

Total divide ratio, P, is given by
$P = NM + A$
$N = 64$, as a 64/65 divider is used
Pmin from above is 17200

Therefore $17200 = 64M + A$
And $M \geqslant A$
Let $A = 0$ Then $Mmin = \frac{17200}{64} = 268.75$

$= 268$
and $Mmax = \frac{17600}{64} = 275.0$

Thus the *M* counter must be programmable from 268 to 275 as required: the *M* counter must have at least 9 bits.
For a frequency of 433.975MHz

$P = 433.97/0.025 = 17359$

$$\text{therefore} \quad M = \frac{17359}{64} = 271.2343$$

The *A* counter is programmed for the remainder i.e.

$$0.2343 \times 64 = 15$$

From this, the *A* counter is programmed to 15 and the *M* counter to 271. The output frequency can bow be checked.

$P = NM + A$
$= 271 \times 64 + 15 = 17359$
and this is the required divider ratio.

Repeated calculations for memory programming may be easily evaluated using a programmable calculator. The program listed in Table 2 is suitable for most Hewlett Packard calculators.

Line	Function	Display
001	hLBLA	25 13 11
002	ENTER	31
003	RCL0	24 0
004	-	71
005	STO2	23 2
006	RCL1	24 1
007	-	71
008	STO3	23 3
009	hFRAC	25 33
010	ENTER	31
011	RCL1	24 1
012	X	61
013	STO4	23 4
014	RCL3	24 3
015	ENTER	31
016	RCL3	24 3
017	hFRAC	25 33
018	-	41
019	STO3	23 3
020	hPSE	25 74
021	hPSE	25 74
022	RCL4	25 4
023	hRTN	25 12

Table 2 Calculator program for values of M and A

To use the program, enter the comparison frequency in STO0, and the dual-modulus prescaler ratio in STO1 (this is the value of N in an $N/N + 1$ divider).

Enter the frequency to be synthesised in Hz and press the R/S button. The calculator will flash twice and display the decimal value of M: pressing R/S again will display the value for the A counter. The M counter value is in STO3: the A counter value is in STO4.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Table 3 Data map

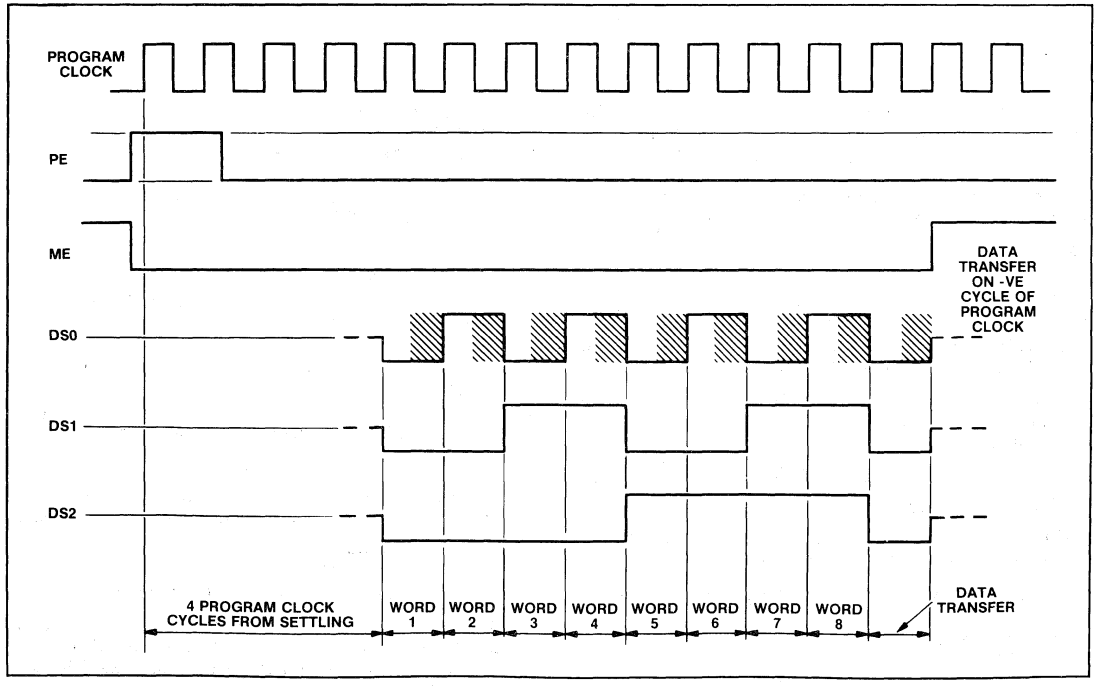


Fig.9 Data selection

NJ8820/1 SYNTHESISER DESIGN SUMMARY

1. Choose a suitable prescaler

- Check that input frequency range is suitable.
- $\frac{fin}{N} < 10.7\text{MHz}$
- $\frac{N}{fin} > 50\text{ns} + tr + tp$

  (tr is 'set-up' or 'release' time - whichever is longer; tp is propagation delay).
- Minimum division ratio is $N^2 - N$.

2. Choose the crystal frequency and value of R

- The phase comparison frequency should be as high as possible - usually the channel spacing.
- Higher crystal frequencies use more current and are less stable, but frequencies below 4MHz need larger case styles.
- R *must* be an even number.

3. Set values for A and M

- A is between 0 and 127.
- A is always equal to or less than M.
- Total division ratio is $NM + A$.
- M is between 3 and 1023.

4. Set loop values

- Choose the loop bandwidth ω_n rads/sec - normally less than $\frac{fx \,.\, 2\pi}{10R}$ (fx = crystal frequency)
- Choose the Damping Factor D - normally 0.7.
- Choose phase comparator gain such that at the lowest modulation frequency the phase deviation

$$\frac{\text{Modulation index}}{(MN + A)} < \frac{4.5}{K_\Phi} \text{ rads}$$

5. Calculate the values:

- $CR2 = \frac{2\pi K_\Phi K_V}{\omega_n^2 \,.\, (NM + A)}$

  (K_Φ in volts/rad)
  (K_V in rads/volt-sec)
  (ω_n in rads/sec)
- $\frac{R2}{R3} = \frac{\pi K_\Phi K_V}{D(NM + A)\ \omega_n}$
- $R1 > \frac{6R2}{K_\Phi}$
- $\frac{1}{R4C2} \geqslant \frac{10\ \omega_n}{2\pi}$

6. Check the time to reach a new frequency

- $t = \frac{\Delta\omega}{2.5K_V} \left(\frac{1}{R1R3} + CR1\right)$

  ($\Delta\omega$ is the frequency step in rads/sec).

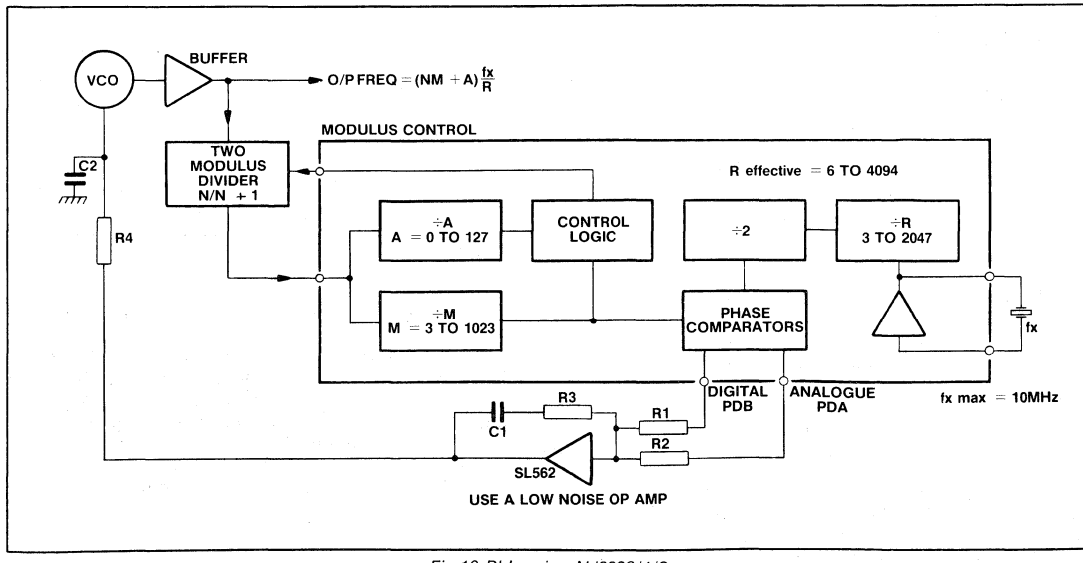


Fig.10 PLL using NJ8820/1/3

7. Check the loop stability using Bode or Nyquist plots - or use the calculator program listed in Table 1. (Page 4).

8. Derive the program numbers for the *A* and *M* counters - or use the calculator program listed in Table 2. (Page 9).

9. An example

A synthesiser is to operate from 430 to 440MHz in 25kHz steps (the channel spacing is 25kHz):

- **Choose the divider** The SP8718 is one choice. Since it divides by 64/65 then $N = 64$.
- **Choose the reference frequency** 25kHz is the channel spacing and is the best choice in this case.
- **Choose the crystal frequency** 2.5MHz is one possibility. The value of *R* can now be calculated:

  Crystal frequency = Reference frequency x *R* x 2
  So $R = 50$
- **Calculate the division ratio** (the ratio between the VCO output frequency and reference frequency)
  This is 17200 to 17600 in steps of 1.
- **Calculate values for A and M** The division ratio $NM + A$ is 17200 to 17600.

  So for the **minimum** frequency: $64M + A = 17200$
  If $A = 0$, $M = 268.75$
  This is not possible (it must be an integer) so this must be **decreased** to make $Mmin = 268$.
- **Draw up a table** for the required values of *A* and *M*

  Division ratio $(P) = NM + A$
  $= 64M + A$

  or use tne calculator program listed in Table 2.

M	A	Division ratio	Output frequency (MHz)
268	48	17200	430.000
..	49	17201	430.025
..	50	17202	430.050
..	..	..	..
..	..	..	..
..	..	..	..
268	63	17215	430.375
269	0	17216	430.400
..	..	..	..
..	..	..	..
..	..	..	..
..	..	..	..
274	63	17599	439.975
275	0	17600	440.000

Table 4 Decimal values of A and M

These figures are acceptable:

$$N \geqslant A$$
$$P > M^2 - M$$

The values of *M*, *A* and *R* must be fed into the NJ8820/1 for each value of frequency required. (In this example the value of *R* is constant). The values must first be converted into BINARY format as shown in Table 5.

M (decimal	M (10 bit binary)									
	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0
268	0	1	0	0	0	0	1	1	0	0
268										
268										
..										
..										
..										
..										
..										
..										
..										
274	0	1	0	0	0	1	0	0	1	0
275	0	1	0	0	0	1	0	0	1	1

Table 5a Binary values for M

A (decimal)	A (7 bit binary)						
	A6	A5	A4	A3	A2	A1	A0
48	0	1	1	0	0	0	0
49	0	1	1	0	0	0	1
50	0	1	1	0	0	1	0
..							
..							
..							
..							
..							
..							
..							
..							
63	0	1	1	1	1	1	1
0	1	0	0	0	0	0	0

Table 5b Binary values for A

R (decimal)	R (11 bit binary)										
	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
50	0	0	0	0	0	1	1	0	0	1	0
50											
50											
..											
..											
..											
..											
..											
..											
..											
50											
50											

Table 5c Binary values for R

In each case the LSB is identified by the heading *M*0, *A*0 or *R*0.

The NJ8820 and NJ8821/23 require 32 bits of data to be transferred for each value of frequency. These 32 bits are composed of the 28 bits above (10 + 7 + 11) plus 4 redundant bits. The method of transferring this data is different for the two device types.

NJ8820 - data obtained from a PROM

NJ8821/23 - data obtained from a Microprocessor.

USING THE NJ8820

The NJ8820 operates with an external 4 bit wide PROM. Information is transferred automatically from the PROM to the NJ8820 when the *PE* pin is activated. A 1024 bit PROM (256 x 4) will store 32 channels because each channel requires the transfer of 8 words (32 bits) of data. A 256 x 4 PROM has 8 address lines (*A*0 to *A*7) of which the NJ8820 can address 3 (*A*0 to A2, connected to *DS*0 to *DS*2). The remaining 5 address lines allow the unique identification of the channel required (32 channels in this case) as shown in Table 6, so for each channel number there are 8 words, each of four bits. The composition of these words is as shown in Table 7. The '-' symbol indicates that this is not read - normally the 8 bit value is 0.

The value of the bits *D*3, *M*1, etc. can be either 0 or 1 and can be found from the tables in the previous section. For example, when $M = 268$ then $M1 = 0$, $M0 = 0$ and WORD 1 is 0000.

USING THE NJ8821/23 IN A PARALLEL MODE

The NJ8821/23 operates with an asynchronous stream of data supplied from a microprocessor. When used in a 4-bit parallel mode it requires the transfer of 8 words (32 bits) of data. Word numbers 1 to 3 control the '*M*' counter, 4 and 5 the '*A*' counter, 6 to 8 the '*R*' counter. It is not necessary to transfer all the words every time; WORD 1 indicates to the NJ8821/23 that the data should be transferred from all latches to counters and so WORD 1 must always be sent last. There are 8 data connections between the microprocessor and NJ8821/23:

- *DS*0, *DS*1 and *DS*2 to select the correct word
- *D*0, *D*1, *D*2 and *D*3 are the input data for *A*, *M* and *R* counters
- *PE* is the strobe

To enter channel information follow the sequence listed below:

1. Ensure the *PE* (strobe) is 0.
2. Select any word (except word 1)...(*DS*0 to *DS*2) and the relevant input data (*D*0 to *D*3).
3. Wait for 1 microsecond or more.
4. Pulse the strobe (to 1) for 2 microseconds or more and return to 0.
5. Wait for 1 microsecond or more.
6. Repeat (2) to (5) as required.
7. Repeat (2) to (5) for word 1.

The composition of the data words is identical to that for the NJ8820.

USING THE NJ8821/23 IN A SERIAL MODE

When used in a serial mode (using a single external shift register) the NJ8821/23 requires the transfer of 8 words, each of 7 bits (56 bits) of data to program the *A*, *M* and *R* counters but only 5 words (35 bits) subsequently to reprogram the *A* and *M* counters. There are thus only 3 data inputs from the microprocessor: DATA, CLOCK and STROBE, as shown in Fig.11.

	ADDRESS LINES								
	A7	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	
CHANNEL NUMBER 0					0	0	0	0	word 1
					0	0	0	1	word 2
					0	0	1	0	word 3
					0				..
					0				..
					0	1	1	1	word 8
CHANNEL NUMBER 1	0	0	0	0	1	0	0	0	word 1
					1	0	0	1	word 2
					1	0	1	0	word 3
					1				..
					1				..
					1	1	1	1	word 8

Table 6 Channel identification

ADDRESS LINES					DATA LINES				WORD
-	-	**A2**	**A1**	**A0**	**D3**	**D2**	**D1**	**D0**	
		0	0	0	M1	M0	-	-	1
		0	0	1	M5	M4	M3	M2	2
		0	1	0	M9	M8	M7	M6	3
		0	1	1	A3	A2	A1	A0	4
		1	0	0	-	A6	A5	A4	5
		1	0	1	R3	R2	R1	R0	6
		1	1	0	R7	R6	R5	R4	7
		1	1	1	-	R10	R9	R8	8

Table 7 Channel number composition

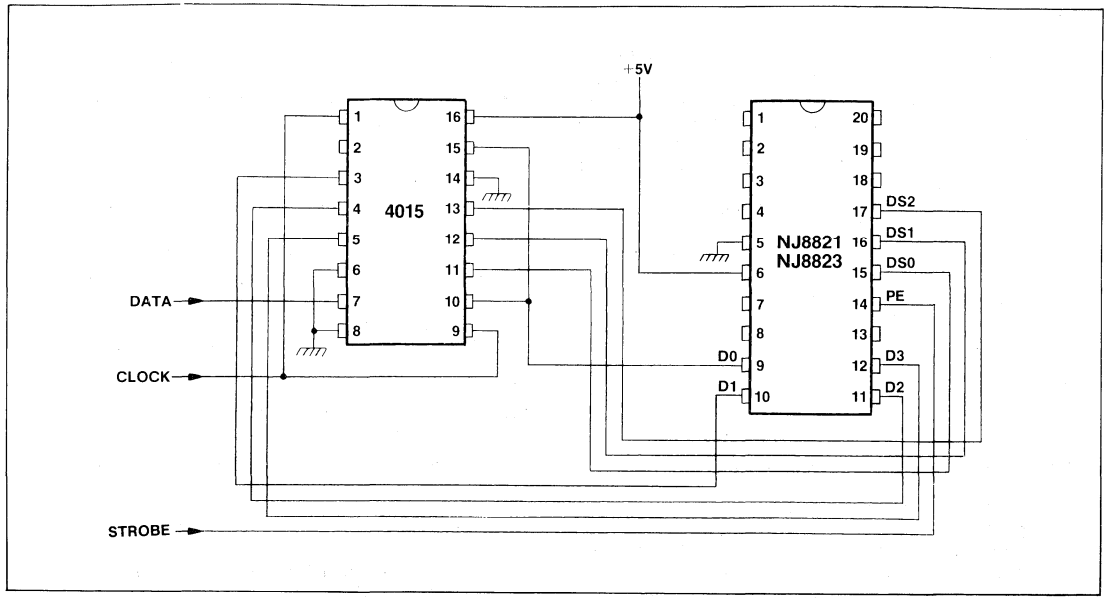


Fig.11 NJ8821/23 serial mode connections

The composition and entry sequence of the data words is identical to that of the NJ8820 except that the data is transmitted serially.

Once again, there is no need to transfer all the words every time provided that WORD 1 is always sent last.

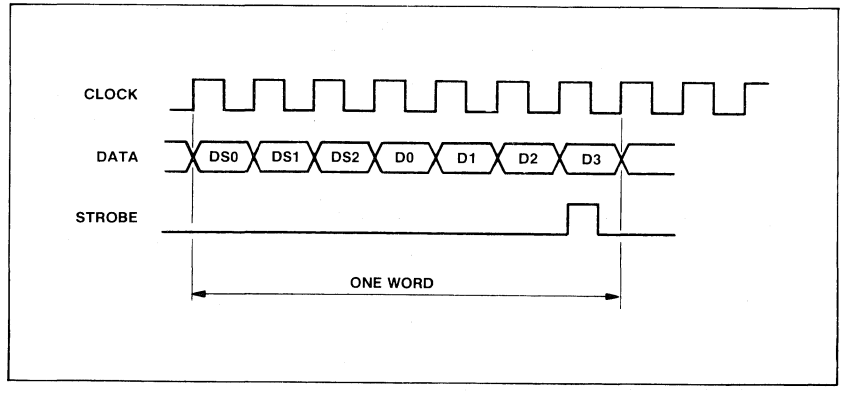


Fig.12 Serial data timing

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2. Frequency Synthesisers, Theory and Design, V. Manassewitsch, Wiley, 1980, ISBN 0-471-07917-0
3. Digital PLL Frequency Synthesisers, U.L. Rohde, Prentice Hall, 1983, ISBN 0-13-214239-2
4. Phaselock Techniques, F.M. Gardner, Wiley 1979, ISBN 0-471-04294-3

A Serially Programmable VHF Frequency Synthesiser

This demonstration circuit uses three Plessey Devices - the NJ8822 single chip synthesiser, the SP8793 dual-modulus prescaler and the SL562 low noise op-amp in the configuration shown in Fig.1. The NJ8822 is programmed via a serial microprocessor interface.

The VCO is a FJET oscillator using a transmission line as the resonator. This VCO is modulated by applying the audio signal to the cathode of a reversed biased PIN diode as shown in the circuit diagram. The loop filter uses the SL562 which with the values shown has a loop bandwidth of 60Hz and a damping factor of 0.6. This filter is followed by a low pass pole at 3.7kHz to attenuate the 12.5kHz reference sidebands. The lock up time for a 1MHz change in frequency is 80ms (determined empirically). The output frequency range is 144-146MHz and the level is +3dBm into 50Ω.

The output spectra at 12.5kHz reference frequency is shown in Fig.2, and Fig.3 is a graph of modulating frequency against percentage distortion at several values of deviation. The circuit performs normally at a supply voltage of 5V ± 0.5V and within a temperature range of -30°C to +70°C. the only observable effect of varying the temperature was a frequency drift of 3kHz between the temperature extremes due to the uncompensated reference oscillator.

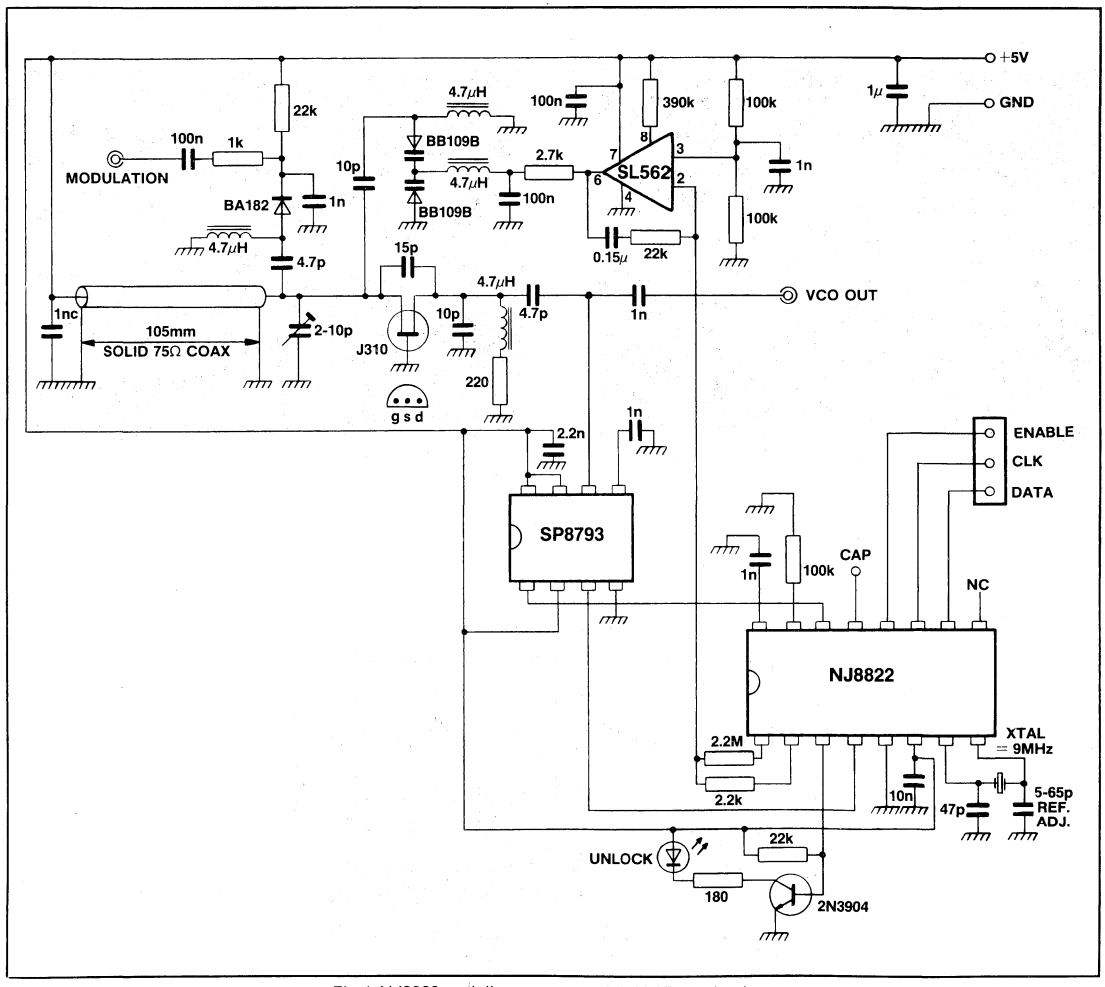
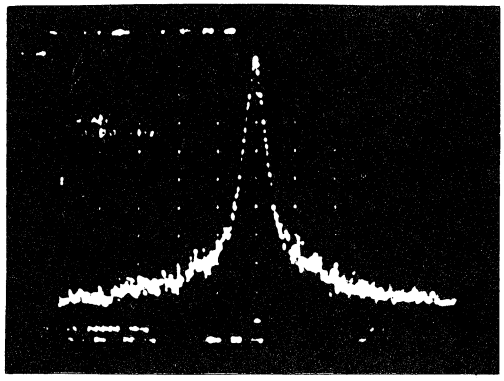
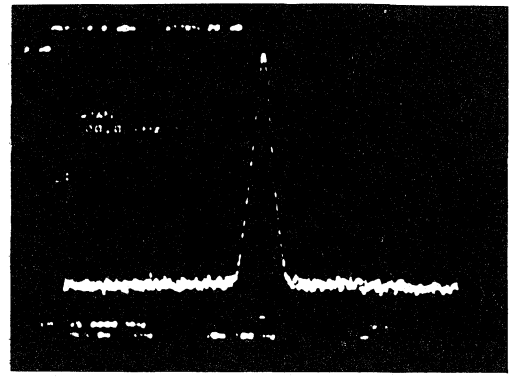


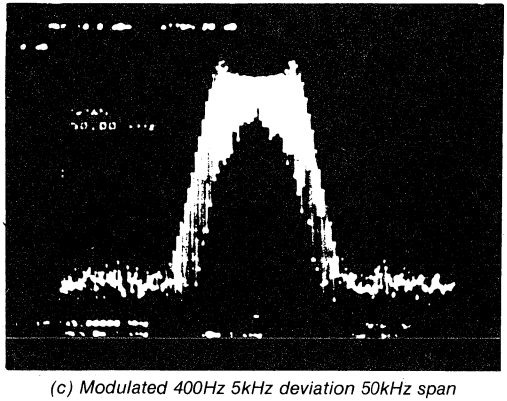
Fig.1 NJ8822 serially programmable VHF synthesiser



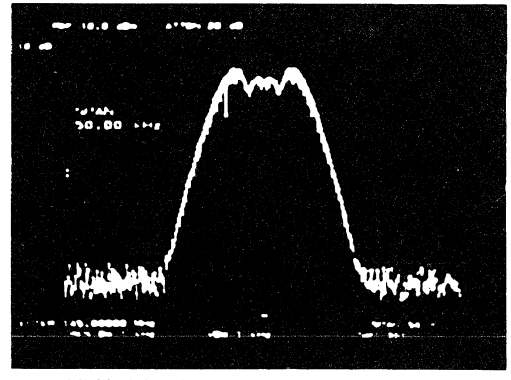
(a) Unmodulated 10kHz span



(b) Unmodulated 100kHz span



(c) Modulated 400Hz 5kHz deviation 50kHz span



(d) Modulated 1kHz 5kHz deviation 50kHz span

Fig.2 NJ8822 frequency synthesiser spectral performance

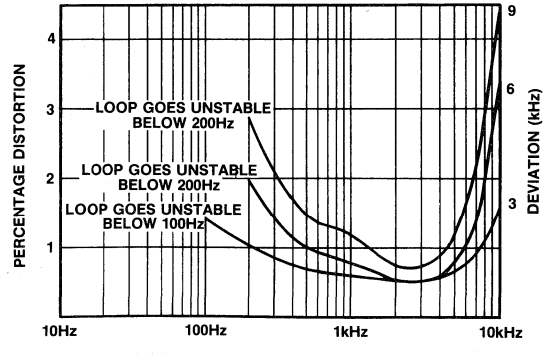


Fig.3 Graph of distortion against modulating frequency at various deviations for the NJ8822 VHF frequency synthesiser

Phase Noise Intermodulation and Dynamic Range

The radio receiver operates in a non-benign environment. It needs to pick out a very weak wanted signal from a background of noise at the same time as it rejects a large number of much stronger unwanted signals. These may be present either fortuitously, as in the case of the overcrowded radio spectrum, or because of deliberate action, as in the case of Electronic Warfare. In either case, the use of suitable devices may considerably influence the job of the equipment designer.

Dynamic range is a 'catch all' term, applied to limitations of intermodulation or phase noise: it has many definitions depending upon the application. Firstly, however, it is advisable to define those terms which limit the dynamic range of a receiver.

INTERMODULATION

This is described as the *'result of a non linear transfer characteristic'*. The mathematics have been exhaustively treated, and Ref.1 is recommended to those interested.

The effects of intermodulation are similar to those produced by mixing and harmonic production, insofar as the application of two signals of frequencies f_1 and f_2 produce outputs of $2f_2 - f_1$, $2f_1 - f_2$, $2f_1$, $2f_2$ etc. The levels of these signals are dependent upon the actual transfer function of the device and thus vary with device type. For example, a truly square law device, such as a perfect FET, produces no third order products ($2f_2 - f_1$, $2f_1 - f_2$). Intermodulation products are additional to the harmonics $2f_1$, $2f_2$, $3f_1$, $3f_2$ etc. Fig.1 shows intermodulation products diagrammatically.

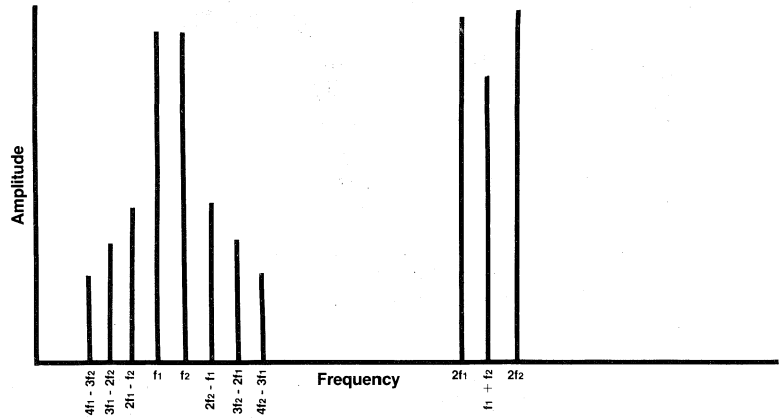


Fig.1 Intermodulation products

The effects of intermodulation are to produce unwanted signals, and these degrade the effective signal to noise ratio of the wanted signal. Consider firstly the discrete case of a weak wanted signal on 7.010MHz and two large unwanted signals on 7.020 and 7.030MHz. A third order product (2 x 7.02 - 7.03) falls on the wanted signal, and may completely drown it out. Fig.2 shows the total HF spectrum from 1.5 to 41.5MHz and Fig.3 shows the integrated power at the front end of a receiver tuned to 7MHz. It may be seen that just as white light is made up from all the colours of the spectrum, so the total power produced by so many signals approximates to a large wide band noise signal. Now, it has already been shown that two signals, f_1 and f_2, produce third order intermodulation products of $2f_1 - f_2$ and $2f_2 - f_1$. The signals will produce third order products somewhat greater in number, viz: $2f_1 - f_2$, $2f_1 - f_3$, $2f_2 - f_1$, $2f_2 - f_3$, $2f_3 - f_1$ and $2f_3 - f_2$. An increase in the number of input signals will multiply greatly the effects of intermodulation, and will manifest as a rise in the noise floor of the receiver.

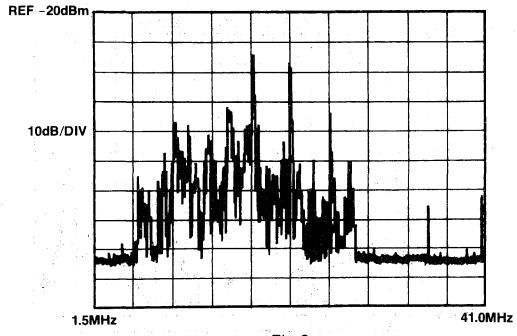


Fig.2

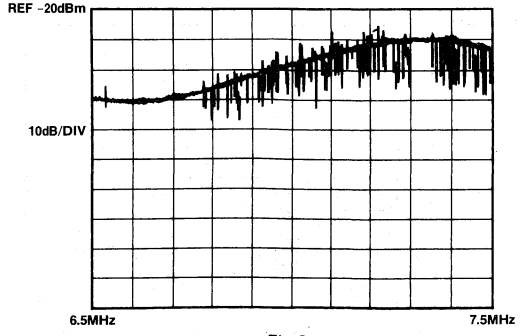


Fig.3

The amplitude relationships of the third order intermodulation products and the fundamental tones may be derived from Ref.1, where it is shown that the intermodulation product amplitude is proportional to the cube of the input signal level. Thus an increase of 3dB in input level will produce an increase of 9dB in the levels of the intermodulation products. Fig.4 shows this in graphic form, and the point where the graphs of fundamental power and intermodulation power cross is the *Third Order Intercept Point*.

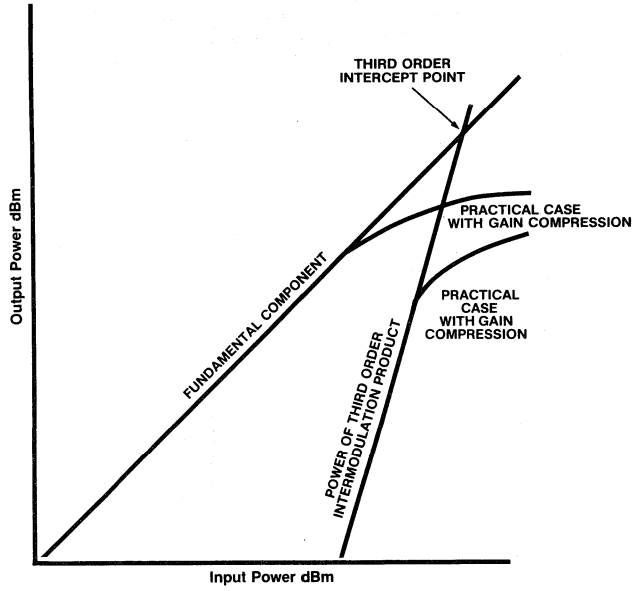


Fig.4 3rd order intercept

The third order intercept point is, however, a purely theoretical concept. This is because the worst possible intermodulation ratio is 13dB (Ref.2), so that in fact the two graphs never cross. In addition, the finite output power capability of the device leads to *Gain Compression*.

Thus, it is apparent that the intermodulation produced noise floor in a receiver is related to the intercept point. Figs.5, 6 and 7 show the noise floor produced by various intercept points, in a receiver fed from an antenna - a realistic test! Fig.5 shows that a large number of signals are below the noise floor and are thus lost; this represents a 0dBm intercept point. Fig.7 shows a +20dBm intercept noise floor, and it is obvious that many more signals may be received.

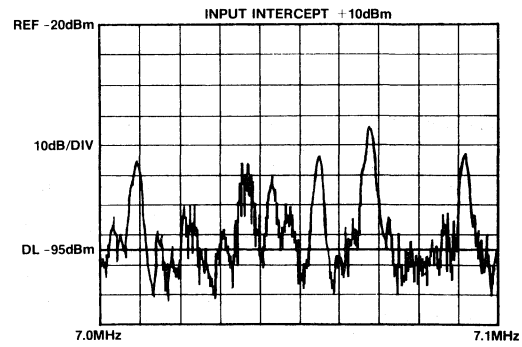


Fig.6

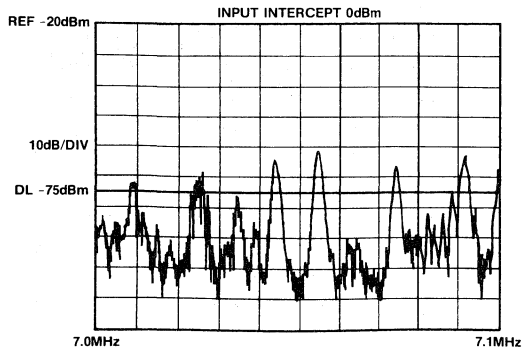


Fig.5

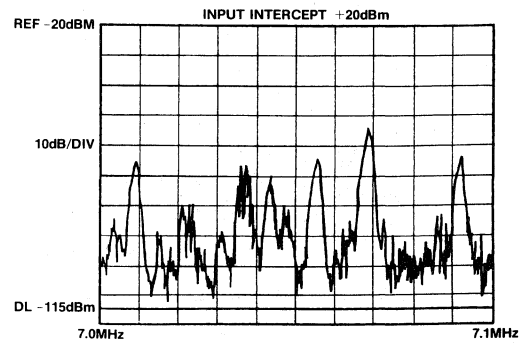


Fig.7

Because of the rate at which intermodulation products increase with input level (3dB on the intermodulation products for 1dB on the fundamental), the addition of an attenuator at the front end can improve the signal to noise ratio, as an increase in attenuation of 3dB will reduce the wanted signal by 3dB, but the intermodulation will decrease by 9dB. However, it is a fair comment that aerial attenuators are an admission of defeat, as suitable design does not require them!

The concept of dynamic range is often used when discussing intermodulation. Fig.8 shows total receiver dynamic range, which is defined as the spurious Free Dynamic Range. Obviously an intermodulation product lying below the receiver noise floor may be ignored. Thus the usable dynamic range is that input range between the noise floor and the input level at which the intermodulation product reaches the noise floor. In fact

$$DR = \frac{2}{3}(I_3 - NF) \quad \ldots (1)$$

Where DR is the dynamic range in dB
I_3 is the intermodulation input intercept point in dBm
NF is the noise floor in dBm.

Note that in any particular receiver, the noise floor is related to the bandwidth; dynamic range is similarly so related.

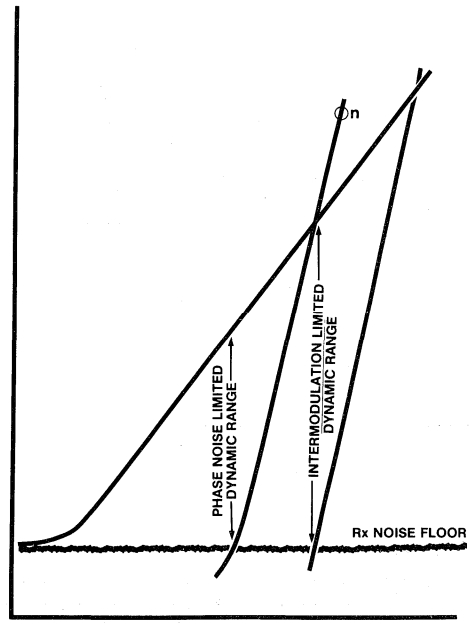


Fig.8

HF receivers will often require input intercept points of +20dBm or more. The usable noise factor of HF receivers is normally 10-12dB: exceptionally 7 or 8dB may be required when small whip antennas are used. An SSB bandwidth would have a dynamic range from (1) of 105.3dB. The same receiver with a 100Hz CW bandwidth would have a dynamic range of 114.6dB and thus dynamic range is quite often a confusing and imprecise term.

Appendix A defines a quantitive method of Intermodulation Noise Floor assessment, developed later than the data in Figs.5 to 7.

VHF receivers require noise figures of 1 or 2dB for most critical applications, and where co-sited transmitters are concerned, signals at 0dBm or more are not uncommon. However, such signals are usually separated by at least 5 % in frequency and filters can be provided. Close-in signals at levels of -20dBm are not uncommon, and dynamic ranges in SSB bandwidths of about 98dB are required.

The achievement of high input intercept points and low noise factors is not necessarily easy. The usual superhet architecture follows the mixer with some sort of filter, frequently a crystal filter, and the performance of this filter may well limit the performance. Crystal filters are not the linear reciprocal two-port networks that theory suggests, being neither linear nor reciprocal. It has been suggested that the IMD is produced by ferrite cored transformers, but experiments have shown that ladder filters with no transformers suffer similarly. Thus, although ferrite cored transformers can contribute, other mechanisms dominate in these components. The most probable is the failure of the piezo-electric material to follow Hooke's Law at high input levels, and possibly the use of crystal cuts other than AT could help insofar as the relative mechanical crystal distortion is reduced. The use of SAW filters is attractive, since they are not bulk wave devices and do not suffer to such an extent from IMD; however, it is necessary to use a resonant SAW filter to achieve the necessary bandwidths and low insertion losses.

The design of active components such as amplifiers is relatively straightforward. Amplifiers of low noise and high dynamic range are fairly easy to produce, especially with transformer feedback, although where high reverse isolation is required, care must be taken. Mixers are however, another matter.

Probably the most popular mixer is the diode ring (Fig.9). Although popular, this mixer does have some drawbacks, which have been well documented. These are:

Insertion loss (normally about 7dB)
High LO drive power (up to +27dBm)
Termination sensitive (needs a wideband 50Ω)
Poor interport isolation (40dB)

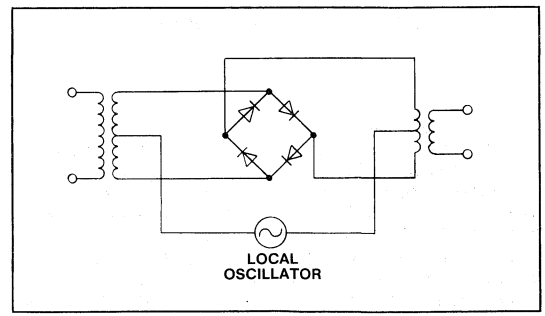


Fig.9 Diode ring

The insertion loss is a parameter which may be classed merely as annoying, although it does limit the overall noise figure of the receiving system. The high LO drive power means a large amount of DC is required, affecting power budgets in a disastrous way, while termination sensitivity may mean the full potential of the mixer cannot be realised.

For the diode ring to perform adequately, a good termination 'from DC to daylight' is required - definitely at the image frequency (LO ± sig. freq.) - and preferably at the harmonics as well. Finally, interport isolation of 40dB with a +27dBm LO still leaves -13dBm of LO radiation to be filtered or otherwise suppressed before reaching the antenna.

A further problem with the simple diode ring of this form is that the 'OFF' diodes are only off by the forward voltage drop of the ON diodes. Thus the application of an input which exceeds this OFF voltage leads to the diodes trying to turn ON, giving gain compression and reduced IMD performance.

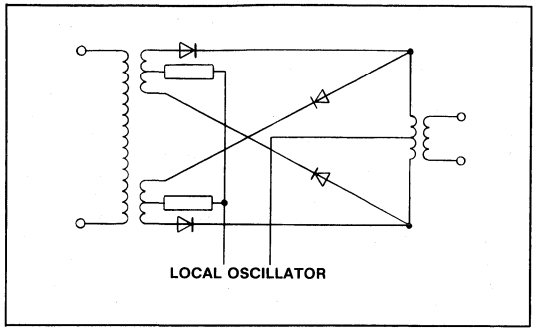


Fig.10 Resistive loaded high intercept point mixer

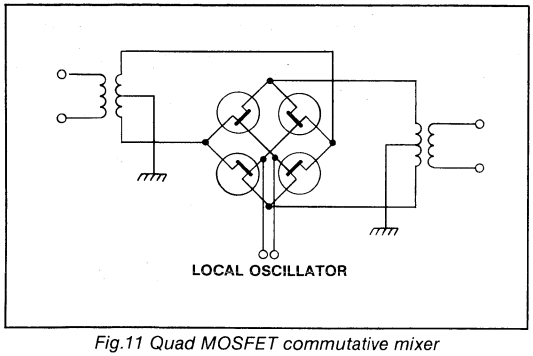


Fig.11 Quad MOSFET commutative mixer

Fig.10 shows a variation of this in which series resistors are added. The current flow through these resistors increases the reverse bias on the OFF diodes which gives a higher gain compression point: such a mixer can give +36dBm intercept points with a +30dBm of LO drive. Nevertheless, as is common to all commutative mixers, the intermodulation performance is related to the termination, and the LO radiation from the input port is relatively high.

Variations of this form of mixer include the Rafuse Quad MOSFET mixer of Fig.11, which suffers with many of the same problems. Fig.12 shows a dual VMOS mixer capable of good performance, but requiring a large amount of DC power and with limited isolation of the LO injection.

Many advantages accrue to the choice of the transistor tree type of approach (Fig.13). Here the input signal produces a current in the collectors of the lower transistors and this current is commutated by the upper set of switching transistors. Because the current is to a first order approximation independent of collector voltage, the transistor tree does not exhibit the sensitivity to load impedance that the diode ring does, and indeed, by the use of suitable load impedances, gain may be achieved. The non-linearity of the voltage to current conversion in the base emitter junctions of the bottom transistors is the major cause of intermodulation, but by using suitably large transistors and emitter degeneration, very high performances (+32dBm input intercept) can be achieved. The Plessey SL6440 has been described (Refs.3, 4, 5) and uses these techniques to achieve a high standard of performance (see Fig.16).

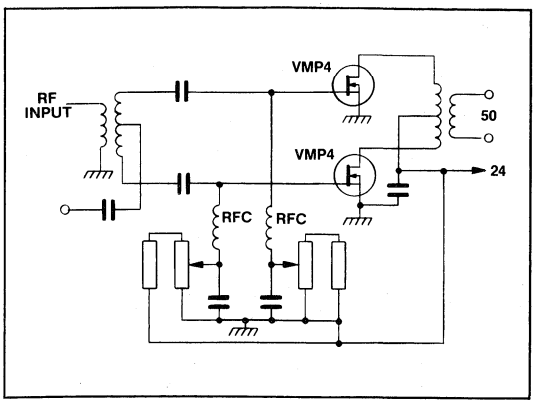


Fig.12 VMOS mixer

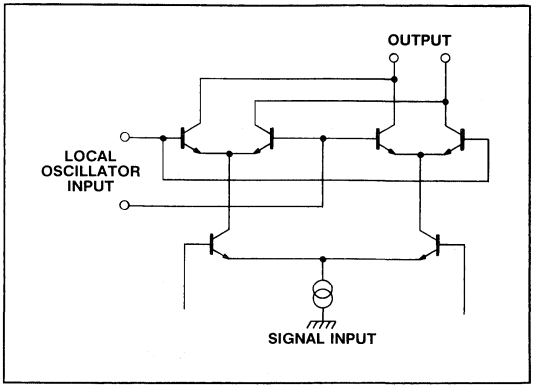


Fig.13 The transistor tree

PHASE NOISE

The mixing process for the superhet receiver is shown in Fig.14, where an incoming signal mixes with the local oscillator to produce the intermediate frequency. Fig.15 shows the effect of noise modulation on the LO, where the noise sidebands of the LO mix with a strong, off channel signal to produce the IF. This means that the phase noise performance of the LO affects the capability of the receiver to reject off channel signals, and thus the receiver selectivity is not necessarily defined by the signal path filters. This phenomena is referred to as *Reciprocal Mixing*, and has tended to become more prominent with the increased use of frequency synthesisers in equipments.

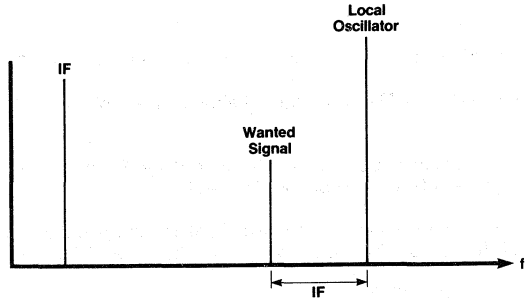


Fig.14 Superhet mixing

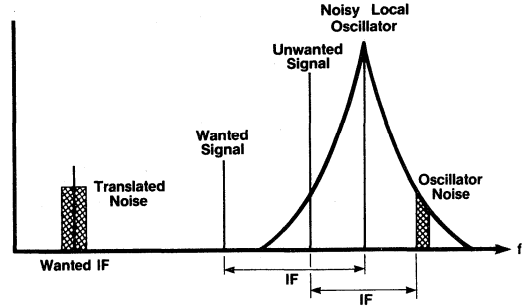


Fig.15 Reciprocal mixing

The performance level requirements of receivers is dependent upon the application. Some European mobile radio specifications call for 70dB of adjacent channel rejection, equating to some -122dBc/Hz, while an HF receiver requiring 60dB rejection in the adjacent sideband needs -94dBc/Hz at a 500Hz offset. The use of extremely high performance filters in the receiver can be completely negated if the phase noise is poor. For example, a receiver using a KVG XF9B filter with a rejection in the unwanted sideband of 80dB at 1.2kHz, would require a local oscillator with -114dBc/Hz phase noise at 1.2kHz if the filter performance was not to be degraded.

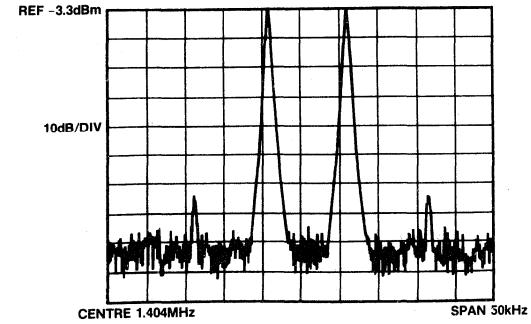


Fig.16 SL6440 intermodulation performance

To put these levels in perspective, relatively few signals generators are adequate to the task of being the LO in such a system. For example, 'Industry Standards' like the HP8640B are not specified to be good enough: neither are the HP8642, Marconi 2017/2018, or Racal 9082, all of which are modern, high performance signal generators.

All this suggests that it is very easy to over-specify a receiver in terms of selectivity, and simple synthesisers are not necessarily ideal in all situations.

The ability of the receiver to receive weak wanted signals in the presence of strong unwanted signals is therefore determined not only by the intermodulation capabilities of the receiver, but by phase noise and filter selectivity.

The usual approach to high performance synthesis has used multiple loops for good close-in performance. Notable exceptions are those equipments using fractional N techniques with a single loop. Nevertheless, such equipments not generally specified as highly as multi-loop synthesisers. A vital part of the synthesiser is still the low noise VCO, for which many approaches are possible. This VCO performance should not be degraded by the addition of the synthesiser: careful choice of technologies is therefore essential. For example, Gallium Arsenide dividers are much worse in phase noise production than silicon, and amongst the silicon technologies, TTL is better than ECL.

From equation (1)

$$DR = \frac{2}{3}(I_{p3} - NF) \text{ dB}$$

where I_{p3} = input intercept point dBm
NF = noise floor dBm

The phase noise governed dynamic range is given by

$$DR_{\Phi} = P_n + 10 \log_{10} B \; Db \qquad (2)$$

Where P_n is the phase noise spectral density in dBc/Hz at any offset and B is the IF bandwidth in Hz.

(N.B. This is not quite correct if B is large enough such that noise floor is not effectively flat inside the IF bandwidth).

Ideally the ratio

$$\frac{DR_{IM}}{DR_{\Phi}}$$

should be 1 in a well designed receiver - i.e. the dynamic range limited by phase noise is equal to the dynamic range limited by intermodulation.

Certain aspects of low noise synthesiser design have been touched upon and Ref.6 provides further information.

The performance of a receiver in terms of its capabilities to handle input signals widely ranging in input level is dependent upon the receiver capability in terms of intermodulation and phase noise. Neglect of either of these parameters leads to performance degradation, and it has been shown that specifications are not only often difficult to meet, but sometimes contradictory in their requirements.

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P.E. Chadwick

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APPENDIX A

Intermodulation is caused by odd order curvature in the transfer characteristic of a device. If two signals f_1 and f_2 are applied to a device with third order term in its transfer characteristic, the products are given by:

$(\text{Cos}f_1 + \text{Cos}f_2)^3 = \text{Cos}^3f_1 + 3\text{Cos}^2f_1\,\text{Cos}f_2 + 3\text{Cos}f^2f_2\,\text{Cos}f_1 + \text{Cos}^3f_2$

from the trig identities Cos^3A, Cos^2A and CosACosB, this is

$\frac{1}{4}\text{Cos}^3f_1 + \frac{3}{4}\text{Cos}f_1 + \frac{3}{2}\text{Cos}^2f_1\text{Cos}f_2 + \frac{3}{2}\text{Cos}f_1\text{Cos}^2f_2 + \frac{3}{4}\text{Cos}f_2 + \frac{1}{4}\text{Cos}^3f_2 + \frac{3}{4}\text{Cos}f_2$

(where $f_1 = A$ and $f_2 = B$). Neglecting coefficients, the terms $\text{Cos}^2f_1\,\text{Cos}f_2$ and $\text{Cos}f_1\,\text{Cos}^2f_2$ are equal to

$\text{Cos}(2f_1 + f_2) + \text{Cos}(2f_1 - f_2)$ and
$\text{Cos}(2f_2 + f_1) + \text{Cos}(2f_2 - f_1)$

By inspection, it may be seen that frequencies of f_1, f_2, $3f_1$,$3f_2$, $(2f_1 \pm f_2)$ and $(2f_2 \pm f_1)$ are present in the output. Of these, only $2f_2 - f_1$, and $2f_1 - f_2$ are close to wanted frequencies f_1 and f_2.
The application of three signals f_1, f_2 and f_3, produces a similar answer, in that the resulting products are:

$3f_1$, $3f_2$, $3f_3$, $f_1 + f_2 + f_3$, $f_1 + f_2 - f_3$, $f_1 - f_2 + f_3$, $f_1 - t_2 - f_3$, $f_2 - f_1 + f_3$, $f_2 - f_1 - f_3$, $-f_1 - f_2 - f_3$, $-f_1 - f_2 + f_3$

in addition to the products

$2f_1 \pm f_2$, $2f_2 \pm f_1$, $2f_2 \pm f_3$, $2f_3 \pm f_2$, $2f_1 \pm f_3$, $2f_3 \pm f_1$

if a greater number of signals are applied such that the input may be represented by:

$\text{Cos}f_1 + \text{Cos}f_2 + \text{Cos}f_3 + \text{Cos}f_4 \ldots \text{Cos}f_n$

The result from third order curvature can be calculated from:

$(\text{Cos}f_1 + \text{Cos}f_2 + \text{Cos}f_3 + \text{Cos}f_4 \ldots \text{Cos}f_n)^3$

This expansion produces terms of

$\text{Cos}(f_1 \pm f_2 \pm f_3)$, $\text{Cos}(f_1 \pm f_2 \pm f_4)$, $\text{Cos}(f_1 \pm f_2 \pm f_n)$ etc from which it can be seen that the total number of products is:

$$\frac{n!}{3!(n-3)!} = 4 \times \tfrac{1}{6}n\,(n-1)(n-2)$$

(The factor of 4 appears because each term has four possible sign configuratons i.e. $\text{Cos}(f_1 + f_2 + f_3)$, $\text{Cos}(f_1 + f_2 - f_3)$ etc). This agrees with Ref A1.
By a similar reasoning, n signals produce:

$2n(n-1)$ products of the form $(2f_1 \pm f_2)$ $(2f_2 \pm f_1)$ etc and n 3rd harmonics.

Thus the total number of intermodulation products produced by third order distortion is:

$$n + 2n(n-) + \tfrac{2}{3}n\,(n-1)(n-2) \qquad (1)$$

Reduction of the input bandwidth of the receiver modifies this. Consider, for example, a receiver with sub-octave filters, rather than the 'wide-open' situation analysed above. In this case, the third harmonics produced by any input signals will not fall within the tune band, as will some of the products such as $f_1 + f_2 + f_3$, $f_1 - f_2 - f_3$, etc. In this case, the total number of intermoduation products is reduced. There are only three possible sets of products of the form f_1 $f_1 \pm f_2 \pm f_3$, i.e. $f_1 + f_2 - f_3$, $f_1 - f_2 + f_3$ and $f_3 - f_1 - f_2$ which can give products within the band. Note that for products to be considered, they must have an effective input frequency at the receiver mixer equivalent to an on-tune desired signal. In addition, products of the form $2f_1 + f_2$, $2f_2 + f_1$ etc are again out of band. Thus half of the $2n\,(n-1)$ products of this class are not able to cause problems and the total number of products to be considered is now:

$$n\,(n-1) + \tfrac{1}{2}n\,(n-1)(n-2) \qquad (2)$$

This result does not agree with Barrs (Ref A2) who uses the results in (1). The results in (2) are an absolute worst case, insofar as a number of the intermodulation products are out of band.

(For the purposes of this analysis, IMD in a mixer is assumed to produce an 'on tune' signal. Thus not all the possible intermodulation frequencies appearing in a half octave bandwidth will be able to interfere).

The same arguments apply to narrower front end bandwidths. However, the narrower the front end bandwidth, the higher is the probability that the distribution of signals will produce IMD products outside the band. For example, a receiver with ±2.5% front end bandwidth tuned to 10MHz will accept signals in a band from 9.75 to 10.25MHz. Signals capable of producing a product of the form $2f_1 - f_2$ must have one of the signals (f_1 or f_2) in the band 9.875 - 10.25 for a product to appear on tune. Thus the two signal apparent bandwidth is less than would be expected. Similar constraints apply to the $f_1 + f_2 - f_3$ product.

Similar arguments apply to other orders of curvature. Second order curvature, for example, will not produce any products in band for input bandwidths of less than 2:1 in frequency ratio.

The actual levels of intermodulation produced can be predicted from reference A1. In practice, the situation is that the input signals to a receiver are rarely all of equal unvarying amplitude and assumptions are made from the input intercept points and the input signal density.

If a series of amplitude cells are established for given frequency ranges, such as that in Table 1, then a prediction of the number of intermodulation products for any given number of input signals and amplitudes may be obtained, either from equation (1) or (2) (as applicable) or from Ref A1 (for higher orders). Where the input bandwidth of the receiver is deliberately minimised, the maximum cell size in the frequency domain should be equal to the input bandwidth.

The total input power in each cell is

$nPav$

where n is the number of signals and Pav is the average power of each signal.

A worst case situation is to assume that all signals in the cell are equal to the cell upper power limit boundary, e.g. if the cell amplitude range is from -40 to -30dBm, then an assumption that all signals in this cell are at -30dBm is a worst case.

If, however, it is assumed that signals will have a Gaussian distribution of input levels within a cell, then the total input power becomes:

$Pt = 0.55nP$

where Pt is the total power
n is the number of signals
P is the power level at the upper boundary of the cell

Because the total IMD power is the sum of all the IMD powers, the average input power is

$$Pav = \frac{0.55nP}{n}$$

The IMD power produced by third order curvature is:

$10 \log_{10} [\frac{1}{3}n(2n^2 + 1)]$ Antilog $\frac{1}{10}[Pav - 3(I_3 - Pav)]$dBm

where P_{IM} is the total power of the intermodulation products
I_3 is the third order input intercept point

Because the coefficients of the amplitudes of the intermodulation products are (depending on product)

$a^3, a^2b, ab^2, abc, b^3$

where a, b and c are approximately equal, the use of a^3 as the general coefficient is justified.

From equations (1) or (2) and (3), the total IMD power and number of products may be calculated. As 'n' increase in number, the number of products will mean that the resultant IMD tends more to a noise floor increase in the receiver, thus reducing the effective sensitivity.

The amount of this degradation is such that the noise floor is:

$$\frac{\frac{2}{3}(0.55nP)^3}{I_3} \times \frac{I_3}{(f_{max} - f_{min})} \times \Delta f$$

where $(f_{max} - f_{min})$ is the bandwidth prior to the first intermodulating stage. Δf is signal bandwidth in a linear system. The Gaussian Factor of 0.55 is somewhat arbitrary, since errors in this assumption are cubed.

The intermodulation Limited Dynamic Range is

$\frac{2}{3}(I_3 + 174 - 10 \log_{10} \Delta f - NF)$

where NF is the Noise Figure in dB.

The effects of Reciprocal Mixing are similar, except that signals may be taken one at a time. The performance is affected by the frequency separation between an 'off-tune' interfering signal and an 'on-tune' wanted signal unless the separation is such that the oscillator noise floor has been reached. Here again, reduction of front end bandwidth reduces the number of signals.

Generally speaking, the effects of reciprocal mixing are limited to close in effects - say within $\pm$50kHz, unless very poor synthesisers are used.

The response at some separation f_0 from the tune frequency is: $(L - 10 \log_{10} 10\Delta f)$dB where L is phase noise spectral density in dBc/Hz and Δf is the IF bandwidth.

This assumes that the spectral density does not change within the receiver bandwidth: Ref A1 shows this to be generally applicable for narrow bandwidths.

The intermodulation free dynamic range is defined as:

$\frac{2}{3}[I_3 - \text{noise floor}] = \frac{2}{3}[I_3 + 174 - 10 \log_{10} \Delta f - NF]$dB

where I_3 is the input 3rd order intercept point in dBm
NF is the noise figure in dB
Δf is the IF bandwidth in Hz

It has been claimed that there is 6dB rejection of phase noise in diode commutative mixers. Thus the relationship between IMD and phase noise can be expressed as:

IMD dynamic range = phase noise dynamic range +6dB = $(L - 10 \log_{10} \Delta f) + 6dB$

Thus at any offset, it is important to ensure that the two dynamic ranges are approximately equal if performance is not be be compromised.

A receiver for example with an input intercept point of +20dBm and input signals of -30dBm will produce an IMD product at -130dBm which, for an HF receiver with a noise factor of 8dB, will be just above the noise floor, in an SSB bandwidth. The noise floor of the LO will need to be such that the noise is at -133dBm if degradation is not to occur, and this will be produced by a noise floor of -137dBc/Hz in the synthesiser at the frequency separation of the signals in question. Thus the high intermodulation performance may well be compromised by poor phase noise.

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Design Compromises in Single Loop Frequency Synthesisers

The single loop frequency synthesiser is justly popular as an approach to frequency synthesis. It has the merit of simplicity, and because of this, low cost, especially as a large amount of the circuitry is easily produced in monolithic integrated circuit form.

Certain performance parameters of the synthesiser are defined by the equipment performance. For example, a marine VHF radio frequency synthesiser has requirements for phase noise and discrete spurious outputs defined by the adjacent channel specification, and the phase noise performance may well need to be several dB better than would at first be expected. If the adjacent channel rejection is 70dB for example, then a single sideband phase noise level in the receiver bandwidth must be more than 70dB, see Fig.1. In fact, the translated noise level should be reduced by an amount dependent upon the performance of other areas of the equipment and these specification levels are typically determined by the system architect. Frequently, however, during design of a project, some modifications in architecture become apparent, but an understanding of practical limitations is vital at an early stage if delay and consequent expense is to be avoided. For further details on the effects of phase noise on receiver performance, see Ref.1.

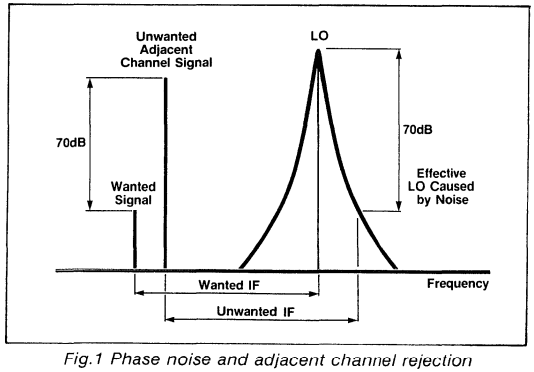

Fig.1 Phase noise and adjacent channel rejection

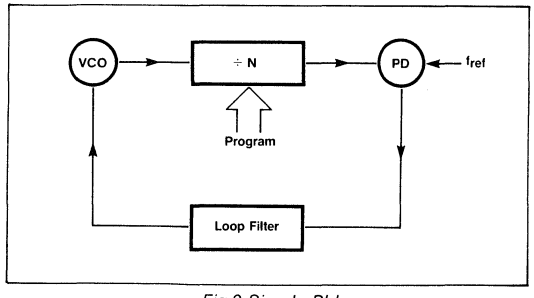

Fig.2 Simple PLL

DIVIDERS

Single loop synthesisers using direct division as in Fig.2 suffer from certain limitations. Fully programmable dividers are not generally available for frequencies above about 50MHz without high power consumptions, and even CMOS dividers currently available are limited in applications at low (5V) supply voltages and extreme temperatures. Newer devices are appearing, however, and experimental 250MHz operation has been observed.

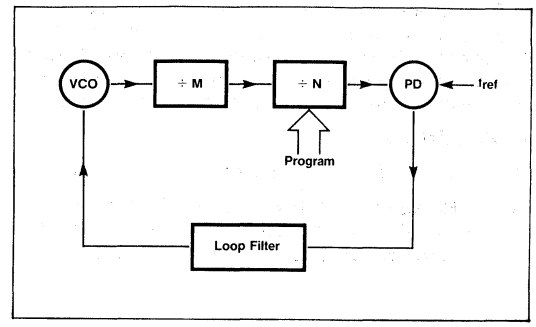

Fig.3 Use of a fixed prescaler

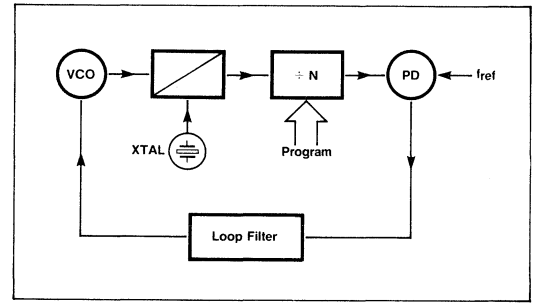

Fig.4 Mixing in the loop

Early synthesisers used fixed prescalers to divide the VCO down to a suitable frequency for the programmable counter as in Fig.3, or used mixing techniques as in Fig.4. Indeed, a large number of CB radios use the mixing technique, but this system can suffer from spurious products unless carefully designed in choice of frequencies, input levels and particular mixers used, see Refs. 2,3,4 and 5. In addition, the large variation in subsequent division ratio may give problems with loop dynamic performance.

A major area of conflict lies in the choice of reference frequency. In synthesisers such as Fig.3, the output frequency step size is *M* times, the reference frequency, where *M* is the prescale ratio. In a system where every channel is used, the problem is then that the reference frequency has to be decreased by a factor of *M*, and as a result, the bandwidth of the feedback loop must decrease. The bandwidth and damping factor of the loop filter are vitally important parameters in determining such loop characteristics as lock up time as well as the phase noise characteristics. (The effects of loop bandwidth on phase noise will be discussed later.) In general, the widest possible loop bandwidth is required to minimise lock up time and to confer the greatest immunity to shock and vibration. However, the loop bandwidth cannot be greater than the reference frequency and so the use of a fixed prescaler is obviously somewhat limited. The alternative is the widely used 'Two Modulus' or 'Pulse Swallowing' prescaler system, illustrated in Fig.5. In this method, the prescaler is able to divide by two integers *N* and *N* + 1. The two counters *A* and

M are programmable and are clocked in parallel, the divider being set initially to the $N + 1$ ratio. When the A counter is full, the divider is set to divide by N until the M counter is full, giving a total division ratio of $MN + A$. This system is limited to a minimum division ratio of $N^2 - N$ if every value of N is to be achieved (no 'skipped' channels) and the M counter must always be programmed to a bigger number than the A counter. Within these limitations, however, a fully programmable divider is achieved and so f_{ref} can now equal the channel spacing.

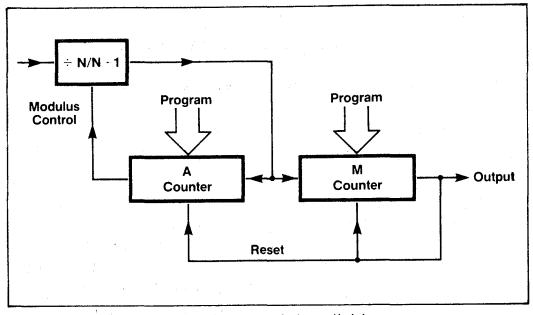

Fig.5 Two modulus divider

Another and more subtle limitation is in the delay times of the various components within the loop. When the circuit (Fig.5) has counted down so that the M counter has been filled, the whole system is reset, and quite obviously, must achieve this in a time equal to $N + 1$ cycles of the input frequency e.g. in a ÷64/65 prescaler, at 1GHz, the reset of the M and A counters must be achieved in 65 cycles or in this case, 65ns. This means that the propagation delays plus set up/release times plus reset delays must not exceed 65ns and it is this area where trouble can often be expected, especially at temperature extremes. Although a 1GHz synthesiser with a 64/65 divider only sees an input frequency of 15MHz for 1GHz input, the set up/release time and delays may well easily reach 85-90ns and the system will thus fail.

If the propagation through the divider $= t_d$
the set up time $= t_s$
the release time $= t_r$
the propagation delay through the A and M counters $= t_c$

then

$$f_{max} = \frac{N}{(t_d + t_s + t_c)} \text{ or } \frac{N}{(t_d + t_r + t_c)}$$

whichever is least.

One of the areas in which an increase in loop delay time can inadvertently occur is if the A and M counters trigger from a different edge to the dual modulus prescaler. This can cause a major diminution in available loop delay, as can an attempt to physically separate the divider and control circuits. Other deleterious affects have been noted, such as radiation of the divider output to the VCO, producing high frequency sidebands, so practical synthesisers are best produced with little physical spacing between divider and control circuit.

The control circuit is a practical device in a number of technologies, although modern devices exclusively use CMOS to minimise power consumption. Prescalers are still mainly exemplified by bipolar technology, advances in which have seen major reductions in power consumptions in recent years - for example from 65mA at 5V for a divide by 10/11 operating at 250MHz in 1976 to 4mA at 5V for a divide by 40/41 operating at 225MHz today. Some equipments still build up the A and M counters from discrete ICs and then add phase detectors, reset circuitry and so on, but such equipments are by now obsolete in design and extremely expensive to manufacture. Nevertheless, the lessons of tolerancing delays necessary in such designs should not be forgotten just because the majority of circuitry is now hidden inside a block of silicon.

The choice of prescaler ratio is governed by a number of factors. Discussed so far have been minimum ratio and loop delay. However, the output frequency of the divider must be low enough for the A and M counters to function. Summarising

1. $f_{in} \leqslant N f_{max\ control}$
   where N is the divider ratio
   $f_{max\ control}$ is control circuit maximum operating frequency.
2. $f_{min} \leqslant \dfrac{N}{\text{total loop delay}}$
3. $P_{min} = N^2 - N$
   where P_{min} is the minimum divide ratio.
   N is the dual modulus divider ratio.

Various values for N exist in proprietary devices. These range from 3/4 to 128/129: binary values (32/33, 64/65, 128/129) are popular for ease of programming from ROMs and microprocessors, while decimal and BCD are used for thumbwheel switch programming.

Programming is a straightforward exercise for binary division and the following method is recommended.

1. The A counter should contain x bits such that
   $$2^x = N$$
2. If more bits are included in the A counter, these should be programmed to zero.

e.g.
$N = 64 = 6$ bits
$A = 10$ bits
then the 4 MSB are programmed to zero.

3. The M and A counters are treated as being combined so that the MSB of the M counter is the MSB of the total and LSB of the A counter is the LSB of the total.

e.g.
A synthesiser operating from 430-440MHz in 25kHz steps uses a 64/65 divider, and the control circuit uses binary counters.
$P = f/f_{ref}$ and f_{ref} = channel spacing = 25kHz
$P_{min} = 430/0.025 = 17200$
$P_{max} = 440/0.025 = 17600$

Minimum possible divide ratio is $N^2 - N = 4032$
where N is two modulus divider ratio

Maximum allowable loop delay $= \dfrac{64}{440 \times 106} = 145\text{ns}$

Total divide ratio, P, is given by
$P = NM + A$
$N = 64$, as a 64/65 divider is used
P_{min} from above is 17200
Therefore $17200 = 64M + A$
And $M \geqslant A$

Let $A = 0$ Then $M_{min} = \dfrac{17200}{64} = 268.75$

$= 268$

and $M_{max} = \dfrac{17600}{64} = 275.0$

Thus the M counter must be programmable from 268 to 275 as required: the M counter must have at least 9 bits.

For a frequency of 433.975MHz

$$P = 433.97/0.025 = 17359$$

therefore

$$M = \frac{17359}{64} = 271.2343$$

The A counter is programmed for the remainder i.e.

$$0.2343 \times 64 = 15$$

From this, the A counter is programmed to 15 and the N counter to 271. The output frequency can now be checked.

$P = NM + A$
$= 271 \times 64 + 15 = 17359$
and this is the required divider ratio.

The two modulus prescaler is therefore able to offer the advantages of producing a programmable divider operating at a very high frequency, but consuming a fraction of the power of such a divider. This enables the reference frequency to equal the channel spacing, thus allowing maximisation of loop bandwidth with its concomitant faster lock up time. It is limited by total loop delay, maximum operating frequencies of dividers and counters, and in minimum count values, but is nevertheless a powerful tool for the synthesiser designer.

The limitation on the value of P_{min}, the minimum ratio can be avoided by the use of three and four modulus dividers. The use of a four modulus counter allows a very wide frequency range to be covered with one device, but at the expense of a much higher power dissipation. Typical of such devices are the Plessey SP8901 and SP8906. Power consumptions for 2-modulus dividers typically range from 4mA at 200MHz (Plessey SP8792/3) through 11mA at 520MHz (Plessey SP8716/8/9) to 25mA at 1GHz (Plessey SP8703).

LOOP BANDWIDTH AND PHASE NOISE

As stated earlier, phase noise is a very important parameter in frequency synthesisers. Too many early synthesisers suffered from phase noise problems which manifested themselves as poor equipment performance in such areas as multiple signal selectivity and ultimate signal to noise ratio. The performance of the synthesiser may be degraded or improved by changing the loop bandwidth, depending upon the characteristics and parameters involved.

The general characteristics of a phase locked loop (PLL) are that for signals injected into the loop it acts as a low pass filter for signals inside the loop bandwidth, and as a high pass filter for signals outside the loop bandwidth. To analyse the performance, consider modulation of the VCO at very low frequencies. The output of the phase detector will be a low frequency signal of phase such as to attempt to remove the modulation imposed on the VCO. As the modulation frequency increases, the error component of the phase detector output is not passed by the loop filter, and so the modulation is not removed by the loop. Note that the modulation is phase modulation (PM) up to the filter break point, and frequency modulation (FM) thereafter. In the 'in-between' range, some interesting distortion effects can occur, especially when excessive group delay exists in the loop filter.

The relationship of loop filter bandwidth to phase noise is now apparent. Phase noise from the oscillator corresponding to frequencies below the filter bandwidth will be removed by the loop, while phase noise components outside the loop bandwidth will be unaffected by the loop. Under these circumstances then, the VCO output spectrum will be cleaned up by the loop. However, for frequencies inside the loop bandwidth, other factors enter. Variations in the reference frequency cause variations in output frequency from the synthesiser, and phase noise components at the reference frequency are purely the frequency domain transforms of time domain frequency instability (Refs. 6,7 and 8). These phase noise effects are multiplied in the loop by the divider ratio. An example (admittedly using gross instability for demonstration) is shown.

If the 430MHz synthesiser has an instability of +1Hz in the 25kHz reference frequency, this is multiplied by P.

i.e. for operation at 433MHz
$P = 433/0.025 = 17320$

Therefore IF +1Hz at 25kHz gives +17.32kHz at final frequency.

Phase noise at the reference frequency is derived from two sources:

(a) the system standard oscillator
(b) the reference chain divider

Oscillators for standards are available with very low phase noise characteristics, and -130 to -170dBc/Hz at 1kHz offset covers the usual range. This phase noise is modified by the reference divider and multiplied by the division ratio as explained above. Of course, phase noise at any offset is reduced by division until the phase noise floor of the divider is reached. Little has been published on the causes of phase noise in dividers, although various measurements have been made (Ref. 9). It has been suggested that TTL and CMOS dividers are better than ECL and CMOS is better at low (10-20Hz) offsets. At a 1kHz offset, ECL levels of about -155 to -165dBc/Hz appear usual. The explanations for the occurence of phase noise is intuitively regarded as being jitter in the transition point of the signal: on this basis, one would not expect CMOS to be so good as TTL insofar as the rise and fall times will be somewhat slower. Regrettably, the difficulty and cost of making meaningful measurements is an inhibiting factor: data on the phase noise performance of Gallium Arsenide dividers would be of considerable interest, especially at small frequency offsets.

From the above discussion, a phase noise floor of some -150dBc/Hz can be expected at the end of the reference frequency divider chain if a good frequency standard is used, while a low cost one may well be at about -130dBc/Hz. In our 430MHz synthesiser, a degradation at 1kHz (if the loop is wide enough) of some 84dB will be seen, so inside the loop bandwidth, the noise performance will be limited to -130 + 84 = -46dBc/Hz. At lower offset frequencies, the phase noise of dividers and frequency standards is worse, so the phase noise performance is now being defined by the loop, rather than the VCO. These are worst case figures, but the ultimate signal to noise ratio of an FM receiver can clearly be seen to be easily limited at UHF by multiplied phase noise. Fortunately, the noise enhancement by the loop is such that pre-emphasis of the modulation provides major improvements in signal to noise ratio.

Nevertheless, it is obvious that the choice of loop bandwidth is compromised by the ultimate signal to noise level required by the system and that such factors as reference oscillator noise level and divider noise cannot be totally disregarded. Operation in the usual cellular radio bands at 800 or 900MHz makes the situation some 6dB worse than that analysed above and the use of a psophometric audio weighting in the equipment is advisable. Sub audible tones may well need fairly high deviation if signal to noise performance is not to be severely limited on them, although modern decoders will work with a negative signal to noise ratio (Ref.10).

In the single loop synthesiser, the phase noise in adjacent channels, which determines the adjacent channel performance, is, to a first order, unaffected by the loop and its parameters. Second order effects such as noise modulation

by such loop components as high value resistors and operational amplifiers may be negated by the use of a passive low pass filter prior to the VCO. Phase noise in the oscillator is discussed below.

Even where the effects of multiplied phase noise may be ignored, such as where the reference divider chain noise is sufficiently low, certain other problems occur in the loop filter design. Many of these are associated with the phase detector employed, which in many areas has been a digital phase/frequency detector. Various types of detector have been used over the years, from an OR gate producing a variable mark space ratio to the well known 2 D type detector. The first of these used integration of the variable mark-space ratio to produce the required output, while the latter (Fig.6) produces minimal width pulses on both Φu and ΦD when in the zero phase error condition. Unfortunately, the zero phase error state exists for a degree of phase error dependent upon the propagation of the gates and a phase error/output voltage characteristic such as Fig.7 is achieved. The performance in the central flat portion of the characteristic means that the loop gain falls to zero when the phase error reaches some small but finite value, and this leads to an increase in the low frequency phase noise of the loop. This phenomenon is of course related to the reference frequency of the loop, being worse at high comparison frequencies.

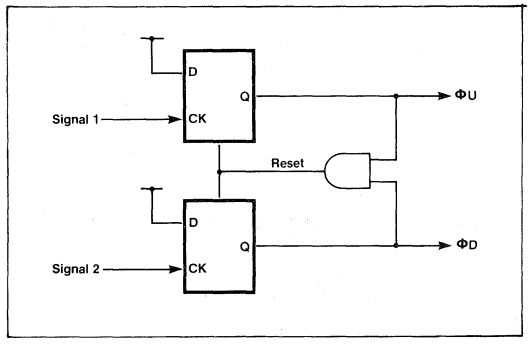

Fig.6 Dual D type phase discriminator

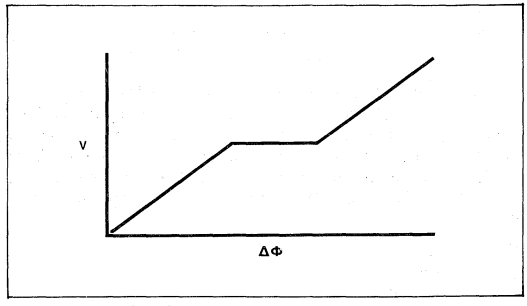

Fig.7 Transfer characteristic of phase discriminator with a charge pump

Although a number of approaches have been made to minimise this problem, including the provision of a leakage path across the VCO control line (Ref. 16), the better approach is to use a linear phase detector of high gain to 'fill in' the gap in the response. An additional benefit of this method is that if the digital phase detector has a 'tri-state' output for the area in which the dead zone occurs and the linear phase detector operates, then the phase detector output at comparison frequency is reduced, allowing either a wider loop bandwidth for the same comparison frequency sideband rejection, or increased rejection, or to some extent, both. The analog phase detector may easily be given a very high gain and narrow range of operation - say a 2 degree range with a gain of 600 volts/radians, but only a limited lock range. It is however, essential to ensure that saturation of this detector, and indeed of the loop filter/amplifier is minimised, as under channel change conditions, the control line and thus the filter amplifiers can be driven hard into saturation. A long recovery time here may well make a mockery of any lock up time calculations. It is this approach which has been adopted in the NJ8820 series of CMOS control circuits from Plessey with a large degree of success.

The choice of loop bandwidth is also governed by the time to change channel, and here again, compromise is often necessary. For example, a lock up time of 1ms and a loop bandwidth of 100Hz are apparently mutually incompatible. By using the two detector approach outlined above however, the loop bandwidth for the digital detector may be made much wider than the analogue detector, thus providing a form of adaptive filtering. The basic loop equation for a type 2 2nd order loop is

$$\omega_n = \sqrt{\frac{K_0 K_v}{N t_1}}$$

where ω_n = loop natural frequency, K_v = VCO gain in Rad/S-v, K_0 = phase detector gain in volts/rad, N = division ratio and t_1 = integrator time constant, shows the dependence of ω_n, the loop natural frequency on N. It should be noted the 3dB bandwidth of the loop and the natural frequency ω_n, are not identical - except for a damping factor, $D = 3.02$.

It was stated earlier that noise caused by the phase detector and loop filter is easily filtered to avoid noise in adjacent channels and the use of low-noise components in loop filters (NOT a 741!) is advisable. Where possible, time constants should use large capacitors and small resistors to minimise KTBR noise. $1/f$ noise can be a problem with operational amplifiers, and where loop bandwidth is high, slew rate is important if the dynamic loop bandwidth is to beary any relationship to the small signal case.

To summarise, the choice of loop bandwidth affects close in phase noise and lock up time. Phase noise is produced by dividers, phase detectors and filters, and when multiplication ratios are high, the reference frequency phase noise can be dominant when multiplied. To minimise this effect, the loop bandwidth can be narrowed, since noise outside the loop bandwidth is determined soley by the VCO. Typical divider phase noises of -150 or -160dBc/Hz can be expected, so low cost reference oscillators can dominate the noise performance.

VOLTAGE CONTROLLED OSCILLATORS

Many engineers consider VCO design to be a black art, and although some art is occasionally involved, VCOs are amenable to analysis.

In the single loop synthesiser, the phase noise performance outside the loop bandwidth is dominated by the VCO, with the noise generation by passive components in the loop filter generally being of lesser importance.

Scherer, Leeson (Ref.12) and Robins (Ref.13) have analysed oscillator phase noise performance and Scherer (Ref.14) has demonstrated the applicability of Leeson's equations and uses the equation

$$L_{(f)} = \tfrac{1}{8} \left[\frac{FkT}{P_s}\right] \frac{(fo)^2}{(f)} \left[\frac{1}{Q} + \frac{P_o}{\tfrac{1}{2}CV^2 2\pi rf.}\right]^2 \quad \text{Eq. 1}$$

where $L_{(f)}$ is the SSB phase noise at an offset F
F is the Noise Figure of the amplifier in the oscillator
k is Boltzmann's Constant
T is the Temperature
P_s is the available signal power
f_o is operating frequency
f is the offset at which the power is to be calculated
Q is working Q of the tuned circuit
C is tank capacity
V is tank current peak voltage
P_o is rf output power

By inspection of Eq. 1, it may be seen that the phase noise is proportional to Q^{-2} and also to (frequency offset)$^{-2}$. This means that for each octave decrease in the offset frequency, the noise power will increase by 4 times or at 6dB/octave. As the frequency offset decreases 1/f or flicker noise becomes important: this 'break' frequency can be as high as 50MHz with GaAs devices. From Eq. 1, it may be determined that a low phase noise oscillator will have a large voltage swing, a high working Q and provide little output power to the load. There is of course a limit as to the level of power required, as the noise of any subsequent buffer amplifiers will degrade the oscillator.

A major compromise in the design of equipment is the choice of VCO frequency. If, for example, a 800MHz cellular radio type of receiver is considered, some fairly straightforward calculations will serve to act as a guide. Starting with the receiver parameters, we will assume that a 70dB rejection of a signal two channels (60kHz) away is required. A numbr of receiver sub system parameters are involved.

(a) Synthesiser phase noise
(b) IF filter performance
(c) Co-channel rejection ratio
(d) Gain compression of stages before the main IF selectivity.

Of these parameters, (c) is the least obvious in its applicability. Ref.1 showed how oscillator noise was mixed onto a wanted signal by a strong unwanted signal. The degradation of a wanted signal by this noise obviously depends upon the relative levels of signal and noise, and because the noise is on the same frequency, the Co-channel rejection. Typically, this means that a noise level within the IF passband of some 8dB less than the signal is required. Thus for the 70dB rejection, oscillator noise at -78dB is required, and 80dB would thus be the design aim.

Conversion of this level to dBc/Hz is not straightforward because of the non linear slope of the phase noise. However, for narrow bandwidths at large offsets, little error is obtained by approximating the phase noise slope to a straight line. This may be illustrated as follows:

From Eq. 1, the power spectrum at an offset beyond the flicker noise knee is given by:

$$P_o = Kf^{-2}$$

where P is the noise power
K is a constant
f is the offset

For a frequency band bounded by f_{lower} and f_{upper}, the noise power is:

$$P_t = \int_{f_L}^{f_U} Kf^{-2}\,df = \left[-Kf^{-1}\right]_{f_L}^{f_U}$$

$$= K(f_L^{-1} - f_U^{-1})$$

Therefore

$$K = \frac{P_t}{(f_L^{-1} - f_U^{-1})}$$

P_t has been defined as the phase noise in the band $= -80$dB therefore

$$K = \frac{10^{-8}}{\left[\frac{1}{53.5 \times 10^3} - \frac{1}{67.5 \times 10^3}\right]} = 2.58 \times 10^{-3}$$

To find the phase noise in a 1Hz bandwidth at an offset f

$$P = Kf^{-2}$$

so at 53.5kHz

$$P = \frac{2.58 \times 10^{-3}}{(53.5 \times 10^3)^2} = 0.901 \times 10^{-15}$$

$$= -120.5\text{dBc/Hz}$$

At 60kHz

$$P = -121.4\text{dBc/Hz}$$

and at 67.5kHz

$$P = -122.5\text{dBc/Hz}$$

If the 'break point' for 1/f noise is above 60kHz, then the spectral density is determined by noise rising at f^{-3}. Similar procedures are followed:

$$P_o = K'f^{-3}$$

$$P_t = \int_{f_L}^{f_U} K'f^{-3}\,df = -K'\left[\frac{f^{-2}}{2}\right]_{f_L}^{f_U}$$

$$= \frac{-K'}{2}(f_U^{-2} - f_L^{-2})$$

$$= \frac{K'}{2}(f_L^{-2} - f_U^{-2})$$

Using similar figures, the performance required is:

53.5kHz	-120.0dBc/Hz
60.0kHz	-121.5dBc/Hz
67.5kHz	-123.0dBc/Hz

The error by assuming a linear relationship is given by:

IF bandwidth = 15kHz
therefore noise power is 10 log $_{10}$ 15 x 10^{3}dB greater than in a 1Hz bandwidth
which is 41.8dB
therefore if the noise power is 80dB down on the signal, total carrier to noise power ratio is -121.8dBc/Hz at 60kHz.

This in fact gives a requirement some 0.4dB higher than previously calculated and in 120dB is obviously negligible.

Having decided upon the level of allowable oscillator noise, it is now possible to calculate the best methods of achieving this level. Using Scherer's figures from Ref.13 for a 400MHz oscillator which will be doubled, using parameters of:

Q = 200
C = 23pF
V = 10V pk
$\frac{FKT}{P}$ = $\left[\frac{6nV}{1V}\right]^2$ where 6nV is the noise voltage and 1V is the input before limiting.

The noise power P at a 30kHz offset is, from Eq. 1, -135dBc/Hz.

So far flicker noise has been ignored. Flicker noise is a low frequency phenomonen which causes problems by intermodulation with the carrier frequency to produce noise sidebands. The 'break point' at which flicker noise becomes dominant varies but a UHF VCO of the type under consideration would probably have a break point at about 50-150kHz offset from the carrier. Eq. 1 needs some

modification to include this factor and a multiplicand of

$$\frac{(1 + f_e)}{f}$$

may be used, where f_e is the $1/f$ noise corner frequency.

The previously calculated noise will now be degraded by about 8dB under these conditions, (assuming f_e = 150kHz) and will now be -127dBc/Hz. This is about 5dB inside the previously calculated requirement. Note that calculations have been made on the basis of a 30kHz offset to allow for doubling the oscillator frequency.

Considering an oscillator with a fundamental frequency of 800MHz, a number of problems appear. Ignoring for the time being the increased noise figure of the device, the available Q of components is considerably less - for example high quality chip capacitors can offer Q's of about 200, leading to working Q of about 100. Calculating noise levels for a 60kHz offset with all other parameters constant except tank capacity which is 12pF (half the 400MHz oscillator) the noise at 60kHz is -105dBc/Hz or about 17dB outside the requirement. Obviously, these figures are no more than a guide, but the suggestion is that the doubled 400MHz oscillator will meet requirements, while the 800MHz oscillator will not (see Fig.8).

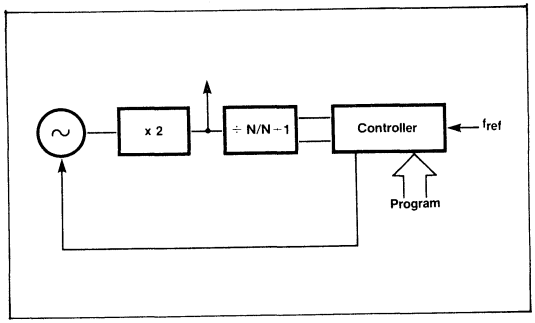

Fig.8 Use of a lower frequency oscillator for improved phase noise

Flicker noise can be reduced by the inclusion of local DC negative feedback, such as an unbypassed emitter resistor, but a major requirement is to choose a suitable device. In general a low phase noise oscillator will run at high power, using a device with both low flicker noise and low high frequency noise, and with high gain and minimum damping on the tuned circuit. In fact, in many applications, the thermionic tube is attractive! Q should be as high as possible, and where VCOs are concerned, the MHz/V should be minimised. This is because of the effects of noise - at 10MHz/V, 1 microvolt of noise will produce 10Hz of FM deviation.

Where relatively wide frequency ranges are concerned, the variation in loop bandwidth may cause problems.

$$\omega_n = \sqrt{\frac{K_o K_v}{N t_1}}$$

where ω_n = natural loop frequency
K_o = VCO constant
K_v = phase detector constant
N = divider ratio
t_1 = integrator time constant

ω_n varies with N, and where desirable to maintain equal lock up times and loop bandwidth, K_v may be designed to vary with N. Several methods exist, but the use of a transmission line VCO can prove useful, as the effective inductance increases with frequency. The use of a suitable length of transmission line can provide an oscillator tuneable from 130 to 190MHz with a coarse tuning trimmer, and electrically tuneable over 6MHz at the bottom of the band to 8.75MHz at the top, thus maintaining ω_n sensibly constant. The use of PIN diodes to switch capacitors is possible, although care must be taken not to degrade Q e.g. a 10pF capacitor at 150MHz has X_c = 106Ω. A PIN diode with an ON resistance of 0.5Ω will give Q_{MAX} = 212, assuming a perfect capacitor, and as considered earlier, this can have disastrous effects on phase noise performance.

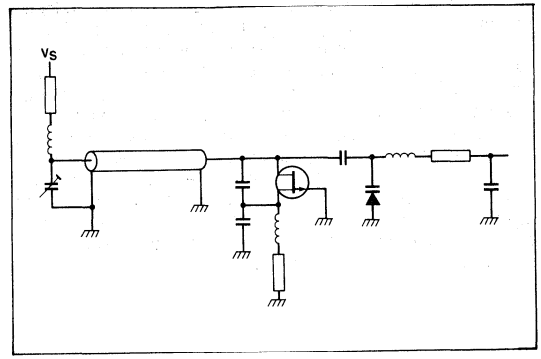

Fig.9 Transmission line VCO using the line as an impedance inverter

An initially attractive method of realising the transmission line VCO is shown in Fig.9, where a length of line is used as a reactance inverter, changing the capacity into an inductance. The use of a Smith Chart will, however, show that the resulting inductance will have a low reactance unless the terminating capacitor is large and the line relatively long (greater than ⅛ wavelength). This leads to a low Q circuit as the resistance of the line is constant, and measurements made using a 16cm rigid coax 75Ω line with a loss of 4dB/100ft at 150MHz gave a Q of less than 100. This line was terminated with an air spaced trimmer. The same line as a shortened capacitively loaded resonator as in Fig.10 had a Q of over 250.

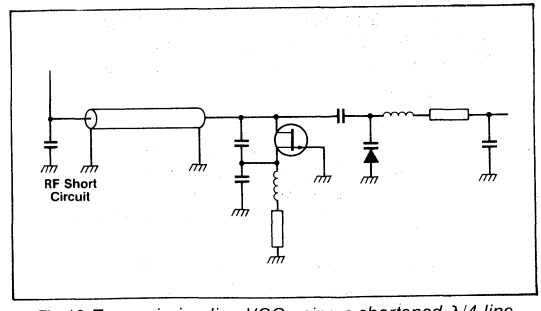

Fig.10 Transmission line VCO using a shortened λ/4 line capacitively loaded

SUMMARY

The compromises in the synthesiser design are now apparent: a narrow bandwidth is required to minimise multiplied reference noise, but a wide bandwidth is needed to minimise lock up time. A high oscillator frequency may be required to avoid spurious outputs and multiplier chains, while a low frequency and multiplier chain give the best performance on system phase noise and possibly power consumption. The classical way to minimise these problems is the two loop synthesiser, but cost is a determining factor effecting the compromise finally reached. Power consumption is always a problem and unfortunately is more demanding at high frequencies while increasing channel occupancy will lead to ever tighter performance requirements in terms of phase noise and switching time.

Modern integrated circuits help the designer by providing better phase detectors and faster lower power dividers. Nevertheless, the single loop synthesiser has been shown to involve a number of compromises in its design, and in some cases, these compromises may limit the final equipment performance level. The single loop synthesiser is very useful, but is not universally applicable.

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A Direct Conversion Paging Receiver using the SL6638

The SL6638 is a lower power direct conversion radio receiver for the reception of frequency shift keyed transmissions. It features the capabilities of 'power down' for battery conservation and control of an external DC-DC converter if single cell operation is required. The device also comes equipped with high current beeper drive and low battery flag indicator.

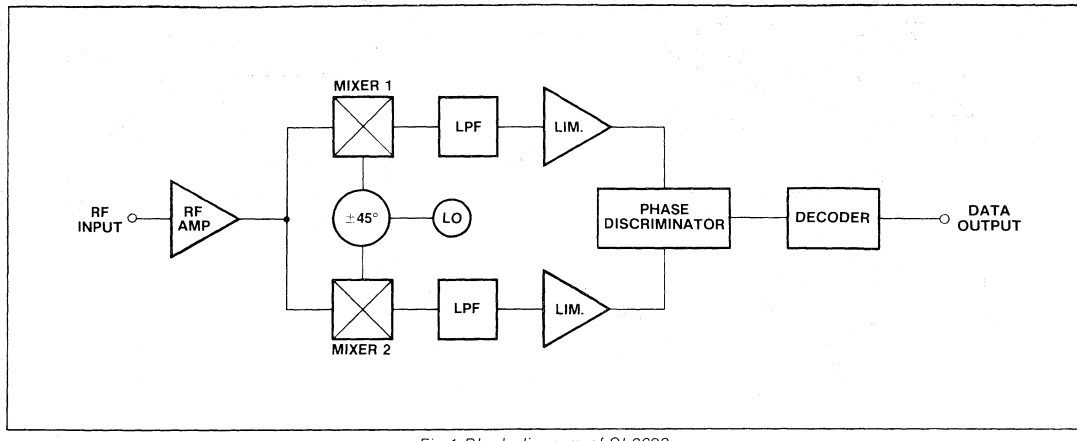


Fig.1 Block diagram of SL6638

PRINCIPLE OF OPERATION

The incoming signal is split into two parts and frequency-converted to base band. The two paths are produced in phase quadrature (see Fig.1) and detected in a phase detector which provides a digital output. The quadrature network may be in either the signal path or the local oscillator path.

The input to the system is an FSK data modulated signal with a modulation index of 18. This gives a spectrum as in Fig.2. f_1 and f_0 represent the 'steady state' frequencies (i.e. modulated with continuous '1' and '0' respectively). The spectrum in Fig.2 is for reversals (a 0-1-0-1-0-1 etc. pattern) at the system bit rate; f_c is the nominal carrier frequency.

When the LO is at the nominal carrier frequency, then a continuous '0' or '1' will produce an audio frequency, at the output of the mixers corresponding to the difference between f_0 and f_c or f_1 and f_c. If the LO is precisely at f_c, then the resultant output signal will be at the same frequency regardless of the data state; nevertheless, the relative phases of the two paths will reverse between '0' and '1' states.

By applying the amplified outputs of the mixers to a phase discriminator, therefore, the digital data is reproduced.

If the waveform at limiter '1' input leads the waveform at the limiter '2' input by 90°, output at detector output will be a high level and low at the Data Output.

If the waveform at limiter '1' input lags the waveform at the limiter '2' input by 90°, output at the detector output will be a low level and high at the Data Output.

The receiver design described in this application uses mainly surface mounted components and employs a ferrite antenna for maximum sensitivity and compactness. The receiver requires two supplies, $V_{CC}1$ and $V_{CC}2$ of 1.3V and 2.2V respectively. Single cell operation is possible using an inverter, a suitable circuit is shown in Fig.9. Alternatively $V_{CC}1$ may be derived from $V_{CC}2$, but $V_{CC}1$ must be at least 1 diode volt-drop down from $V_{CC}2$.

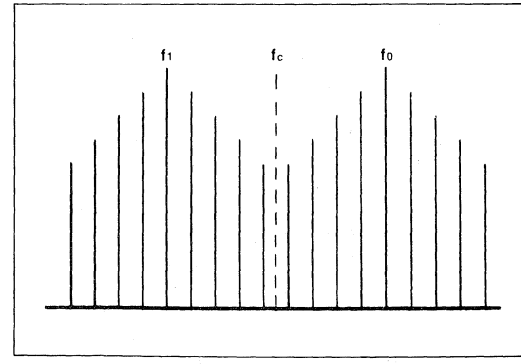


Fig.2 Spectrum diagram

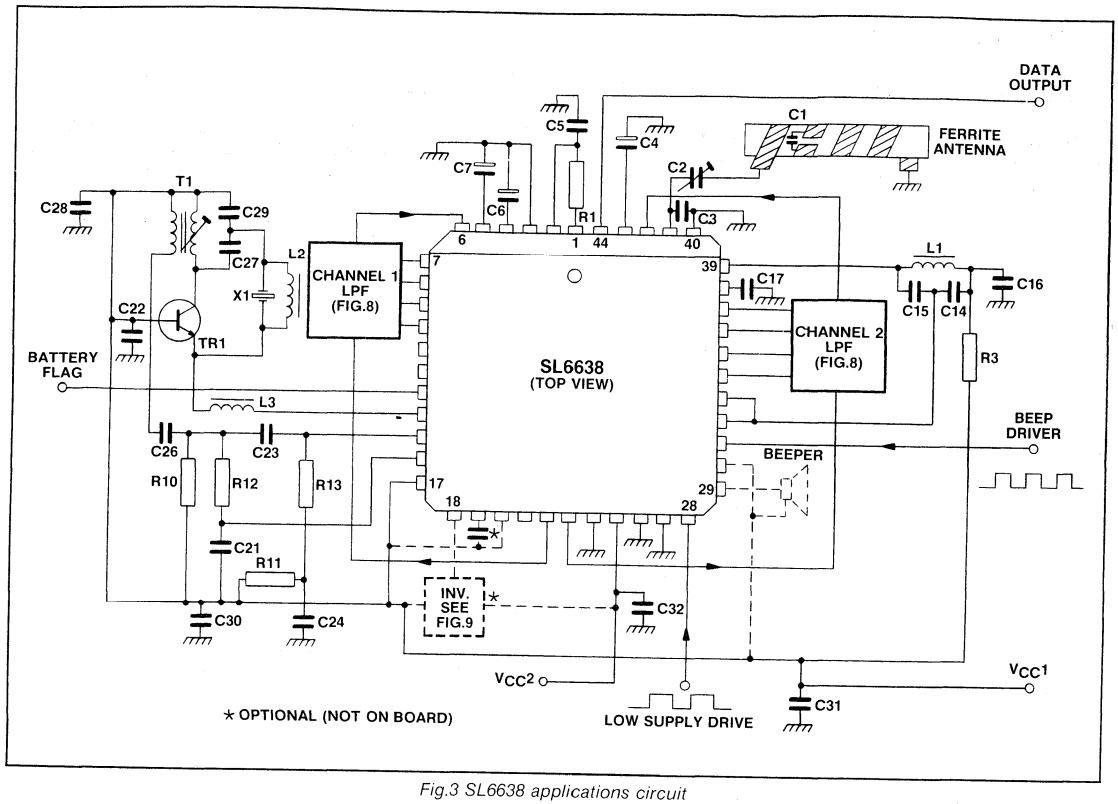


Fig.3 SL6638 applications circuit

R1	220k	C1	8.2p	C21	8.2p	IC1	SL6638
R2	15k	C2	2-10p	C22	1n		
R3	100	C3	22p	C23	8.2p	L1	3 turns of 0.45 dia. enamelled wire on 3.5mm dia. form (available from Wainwright Instruments, type VCF-1)
R4	39k	C4	10μ	C24	1n		
R5	22k	C5	1n	C26	22n		
R6	2.7k	C6	10μ	C26	1n		
R7	22k	C7	10μ	C27	15p		
R8	15k//180k	C8	8.2n (5%)	C28	1n		
R9	6.8k//100k	C9	2.2n (5%)	C29	22p	L2	220nH choke
R10	100	C10	2.2n	C30	1n		
R11	100	C11	1.2n	C31	1μ	L3	10μH choke
R12	100	C12	2.2n	C32	1μ		
R13	100	C13	2.2n (5%)	C33	10n (5%)	T1	as L1 but with an axial winding of 4 turns
R14	6.8k//100k	C14	27p	C34	8.2n (5%)		
R15	22k	C15	8.2p	C35	22n		
R16	15k//180k	C16	1n	C36	180 (5%)	X1	153MHz 7th/9th overtone crystal
R17	2.7k	C17	1n	C37	1.2n		
R18	22k	C18	470 (5%)	C38	470p (5%)		
R19	39k	C19	180 (5%)				
R20	15k	C20	10n (5%)	TR1	BFY90		

Table 1 Component values for Fig.3

CIRCUIT DESCRIPTION See Figs.1 and 3

The RF input, which is an FSK signal, is applied to the RF amplifier, and from the output of this stage to the mixers. The local oscillator inputs of these mixers are driven in phase quadrature from the crystal controlled oscillator, phase shift being produced by a resistor-capacitor network. The frequency of the local oscillator is equal to the nominal carrier frequency, and the mixer outputs at baseband are filtered in the active filters, which provide selectivity. In theory, a receiver using 'zero IF' has infinite adjacent channel rejection. The AF outputs of the LPF's are in turn fed to the inputs of two limiting amplifiers which provide most of the receiver gain, and the outputs of which feed the detector. This consists of a number of phase detectors arranged to provide phase comparison on four pairs of signal edges, thus maximising sensitivity. The detected output is now filtered in the Bit Rate Filter, and applied to a further limiter, providing the received data at the output.

The RF Amplifier

This is a single NPN transistor whose bias is provided internally and whose terminals are available on pins 39, 40 and 41.

There is a collector tuned load and the input tuned circuit consists of the ferrite antenna and capacitors C2 and C3//Ci.

The ferrite antenna (Fig.6(a)) consists of a length of F29 ferrite rod on which is wound four turns of 0.2in copper tape. The tape is cut near the centre of the coil and an 8.2pF ceramic capacitor inserted. This capacitor effectively reduces the inductance of the coil allowing more turns to be used thus increasing the efficiency of the antenna.

The input circuit is shown in Fig.6(b). It will be seen that the antenna is resonated with the series combination of C2 and C3 in parallel with the input capacitance of the device. The resultant capacitive tap provides a 10:1 impedance transformation, thus keeping the Q of the tuned circuit fairly high.

A set of 'S' parameters is included (see Fig.15) to facilitate the optimum design of input and output networks for the RF amplifier.

The Mixers and Quadrature Network

The two mixers are fed with local oscillator energy via an RC network which provides 90° phase shift between the two LO inputs on pins 15 and 16. The signal inputs are on pins 33 and 32 respectively and the mixer outputs are on pins 23 and 22.

It is also possible to include the quadrature network in the RF signal path in which case pins 15 and 16 are fed directly from the LO.

A plot of S_{11} measurements is included to enable optimum matching of the quadrature network to pins 15 and 16 (see Fig.16).

The RC network employed in this application is shown in Fig.4.

The Local Oscillator

The circuit employed in this application uses a BFY90 transistor and a 7th or 9th overtone crystal and is illustrated in Fig.5. The 220nH inductor L2 in parallel with the crystal suppresses oscillation at the crystal fundamental.

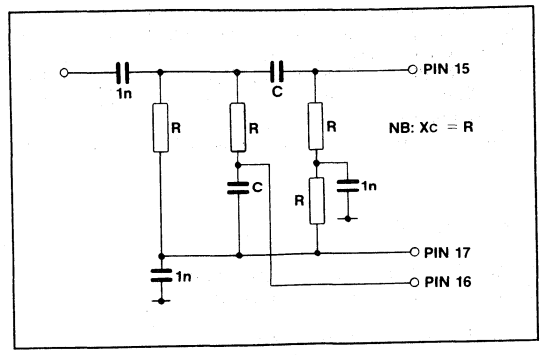


Fig.4

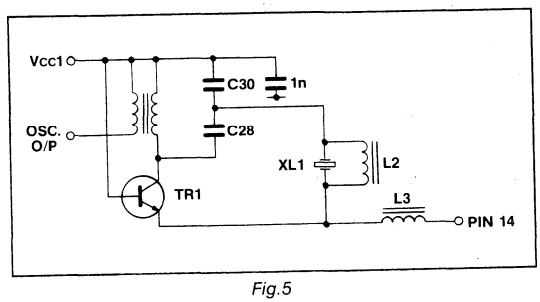


Fig.5

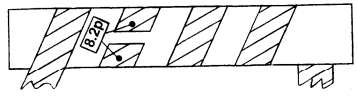


Fig.6(a) Construction

Antenna design by courtesy of Multitone Electronics plc, UK Patent No. 2110851B.

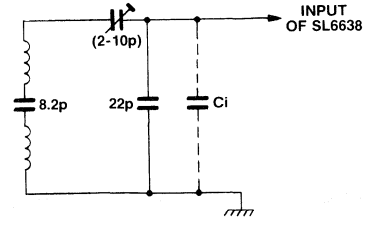


Fig.6(b) Antenna circuit

Fig.6 Ferrite antenna details

The Active Filters

These are 4-pole low-pass filters utilising the high gain inverting amplifier and the unity gain emitter follower available on the device. These amplifiers are configured as a multiple feedback LP filter and a Salen and Key LP filter respectively. There are two passive RC networks which provide a further two poles.

The following equations may be used to design the filters.

MFB low pass filter (Fig.7(a))

1. Select C_1 and C_2 such that $C_2 = 10/fc\ \mu F$ and $C_1 =$ or $C_{2/2}$ $(K + 1)$ where K is the required gain.

2. Resistance values are found by:

$$R_2 = \frac{2(K+1)}{\left[\sqrt{2C_2} + \sqrt{2C_2^2 - 4C_1C_2(K+1)}\right]\omega_c}$$

$$R_1 = R_2/K$$

$$R_3 = \frac{1}{C_1C_2\omega_c^2R_2}$$

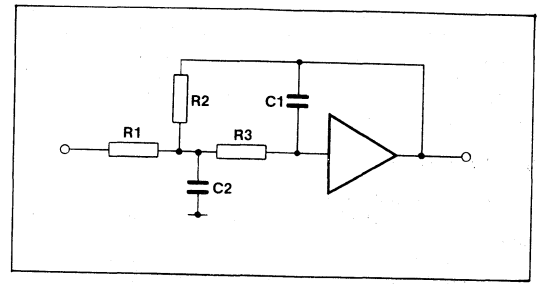


Fig.7(a)

Salen & Key low pass filter (Fig.7(b))

1. Select $C_2 = 10/fc\ \mu F$ and $C_1 = C_{2/2}$.

2. Resistance values are found by:

$$R_1 = \frac{2}{\left[C_2\sqrt{2} + \sqrt{2C_2^2 - 4C_1C_2}\right]\omega_c}$$

$$R_2 = \frac{1}{C_1C_2R_1\omega_c^2}$$

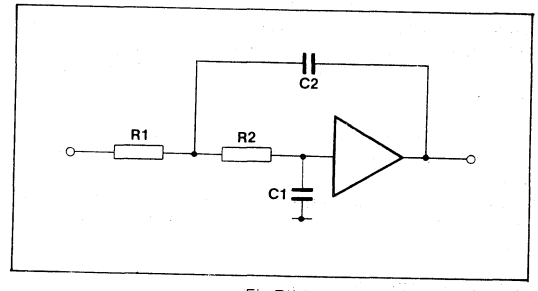


Fig.7(b)

RC single pole filter (Fig.6(c))

$C = 10/fc\ \mu F$

$R = 1/\omega_c C$

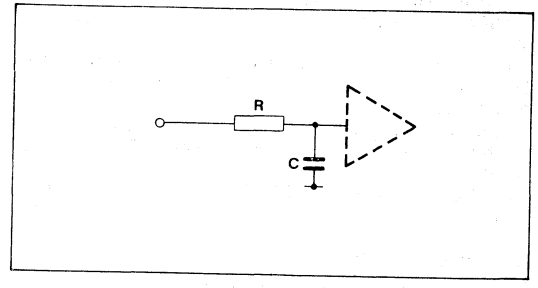


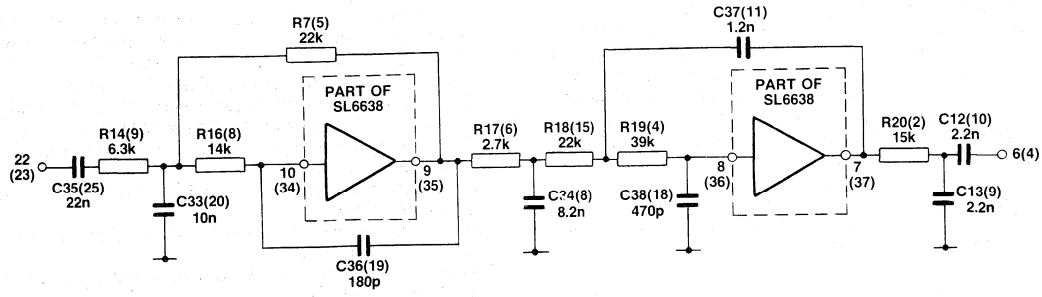
Fig.7(c)

NB. These equations are for 2nd order Butterworth LP filters.

The actual component values used in this application and a plot of the frequency response are illustrated in Fig.8.

The filters provide an adjacent channel rejection of 70dB at 25kHz separation with a 250Hz square wave modulated signal at 4.5kHz deviation.

It is possible to obtain similar performance at 12.5kHz separation with 2kHz deviation if all capacitance values shown above are doubled.



NB: ALL CAPACITOR VALUES ARE ±5% EXCEPT COUPLING CAPACITORS

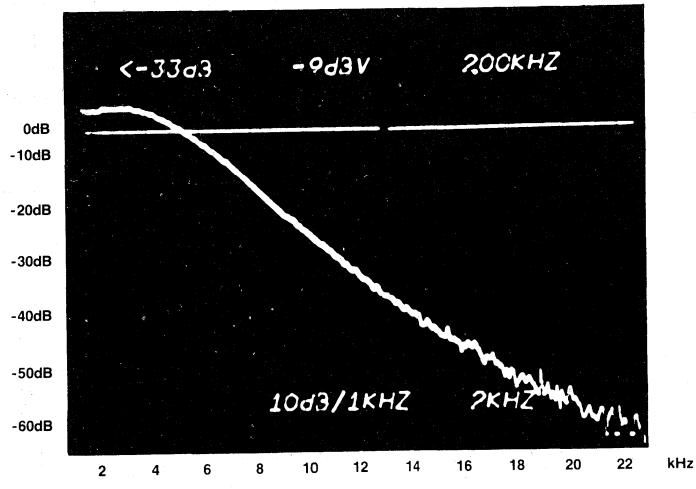


Fig.8 Active filter component values and frequency response for SL6638 DC pager

Limiting Amplifiers and Phase Discriminator

The limiting amplifiers limit with inputs of about 6μV on pins 6 and 42. Pins 4,5 and 43 are bypassed to ground by 10μF capacitors.

The outputs of the limiting amplifiers go directly to the phase discriminator and are not accessible externally. The discriminator output is at pin 1.

Decoder

This is a limiting amplifier which is internally slew-rate limited to prevent fast output edges being radiated back to the antenna.

The connection of a 1nF capacitor from pin 2 to ground is adequate as a LPF to the modulation frequency.

A 220kΩ resistor is connected between pin 1 and pin 2 to suppress feedback. The data output is available at pin 44.

Inverter Circuit

This inverter is used to provide $V_{CC}2$ which is 2.3V from a single supply $V_{CC}1$ which is 1.3V.

The inverter control output on pin 18 is derived from the ratio of the internal reference to the $V_{CC}2$ line and moves in phase with changes in the $V_{CC}2$ line. Pin 21 allows the value of $V_{CC}2$ to be adjusted.

Pin 13 is a battery flag which is activated when $V_{CC}1$ falls below about 1V. The inverter circuit is shown in Fig.9.

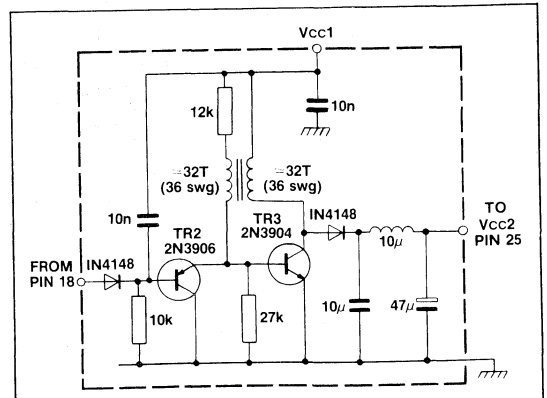


Fig.9 Inverter circuit for SL6638 pager

Beeper Drive

This stage accepts an input from an external source and provides a high current drive to the beeper. This current drive can be as high as 200mA and the arrangement is such that the output waveform may be modified when the battery is low. This modified waveform is generated externally and applied to pin 28. When the battery is low pin 28 will override the beep input on pin 31. A logic high will remove beep drive and a logic low will connect beep drive.

The internal band-vap reference is 1.2V and this is divided down to a suitable voltage.

An internal diode connects pin 29 to pin 30 to protect the driver transistor when used with inductive loads.

Battery Economy

The following functions will have their bias removed during power down (high on pin 24):

RF amplifier
Oscillator current sources
Mixers
Active filters
Phase discriminator
Bit-rate filter and decoder

RECEIVER PERFORMANCE

The performance of the paper circuit is measured using a quasi bit-error detector which is illustrated schematically in Fig.10. Errors on the +ve or -ve half cycles of the recovered data (depending on the setting of SW1) are examined.

A reading of 8Hz on the frequency counter corresponds to a bit-error rate (b.e.r.) of 1 in 30. The sensitivity at a b.e.r. of 1 in 30 with a square wave modulated signal and a deviation of 4.5kHz is of the order of 10μV/m.

Adjacent channel rejection = 70dB (for 6dB degradation 25kHz separation)
Co-channel rejection = 1dB (wanted signal 6dB above level for 1 in 30 b.e.r.)
Co-channel rejection = 0dB (wanted signal 12dB above level for 1 in 30 b.e.r.)
Co-channel rejection = 0dB (wanted signal 20dB above level for 1 in 30 b.e.r.)
Co-channel rejection = 1dB (wanted signal 30dB above level for 1 in 30 b.e.r.)
3rd order input intercept = -6.5dBm

The above measurements are all made using a wanted signal of 153MHz modulated by a 250Hz square wave at a deviation of ±4.5kHz

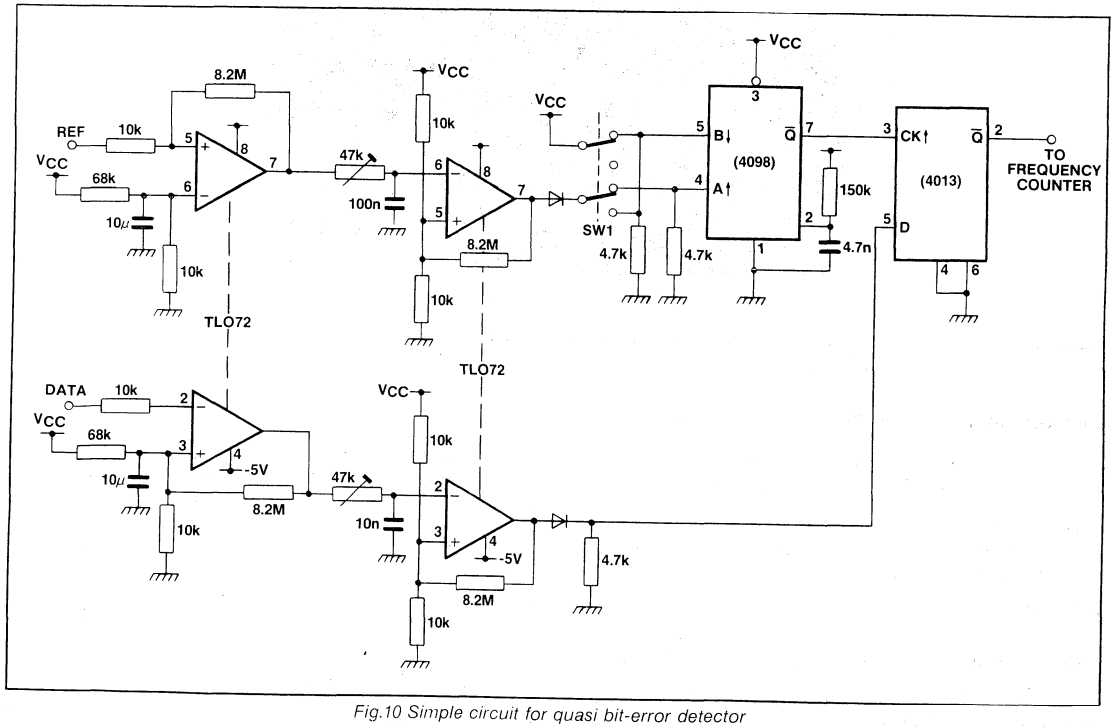


Fig.10 Simple circuit for quasi bit-error detector

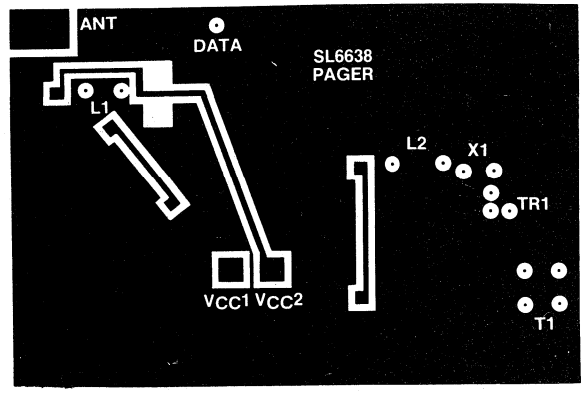


Fig.11 PCB ground plane (1:1)

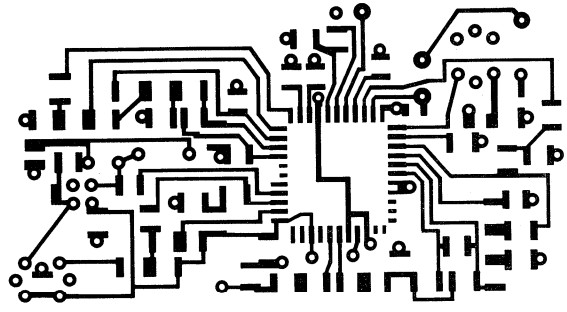


Fig.12 PCB track side (1:1)

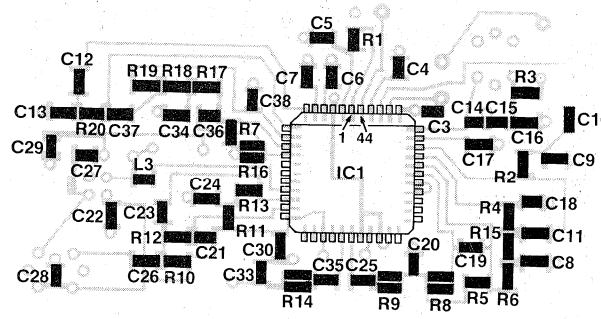


Fig.13 PCB surface mounted component overlay (1:1)
NOTE: R8, R9, R14 and R16 each comprise two chip resistors connected in parallel (see Table 1)

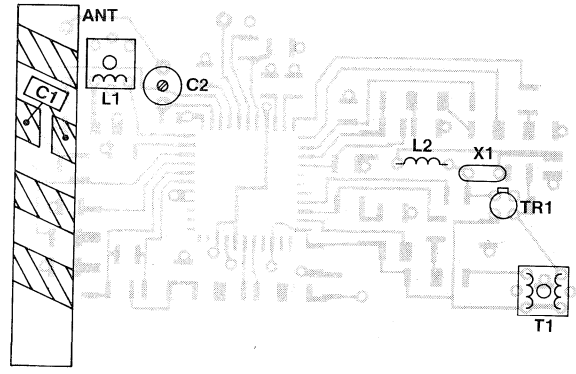


Fig.14 PCB component layout for ground plane side (1:1)

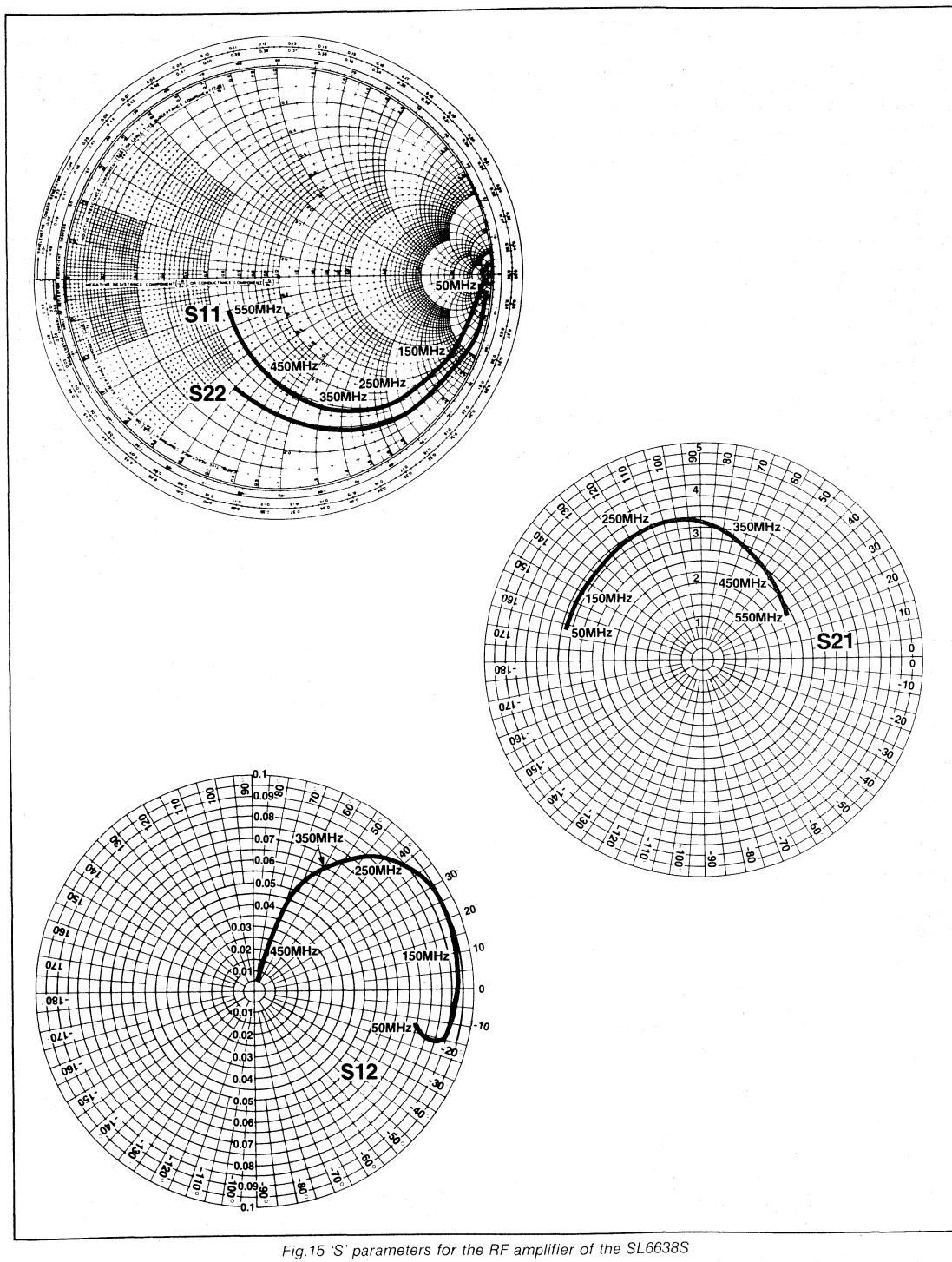


Fig.15 'S' parameters for the RF amplifier of the SL6638S

The care and feeding of High Speed Dividers

Circuit design and layout for high speed dividers operating at frequencies up to 2GHz owe much more to analog RF design techniques than normal digital ones and the limitations on flexibility and component choice inherent in UHF RF design are of paramount importance in successful designs.

PRACTICAL DESIGN CONSIDERATIONS

High speed divider applications require the printed circuit boards to be mechanically designed with two considerations in mind:

(1) Electrical performance
(2) Mechanical and thermal performance.

These two considerations are inter-related; for example, the use of 1/16 inch thick fibreglass PC board may be desirable mechanically, but a 50Ω stripline on this thickness of board is about 5/32 inch wide, and is thus too wide to pass between the pins of an IC.

Most of the heat conducted from a dual-in-line IC package is removed from the bottom of the package. Less than 10 % is conducted out by the leads, and because of the cavity between the chip and lid, relatively little through the top of the package.

For this reason, the use of a double-layer PC board layout is recommended, with a ground plane top surface. Where 1/32 inch thick material is used, a top surface ground plane will add substantially to the heat dissipation capabilities of the board.

For use at very high frequencies, consideration must be given to the type of component used. Carbon composition resistors are more nearly resistive at high frequencies than either carbon or metal film types, and are available in very small sizes. Bypass capacitors need to be chosen carefully if they are to act as low impedances, as series inductance leads to an increasing impedance with frequency above the series resonant frequency of the device. As a guide, a 1000pF disc ceramic capacitor with 1/4 inch leads will be self resonant at about 75MHz, and will appear as an inductive impedance of about 22Ω at 800MHz. The use of chip capacitors is recommended above 500MHz, although leaded monolithic ceramic capacitors with suitably short leads are often acceptable.

The use of a ground plane for RF decoupling purposes is often recommended, and can be helpful. However, the danger is that the ground current paths in the plane are not defined very well, and because of this lack of definition, the ground plane can cause unsatisfactory operation. Probably the best method is to return all the bypass capacitors to a single point (as in Fig.1) and return this point to the ground plane.

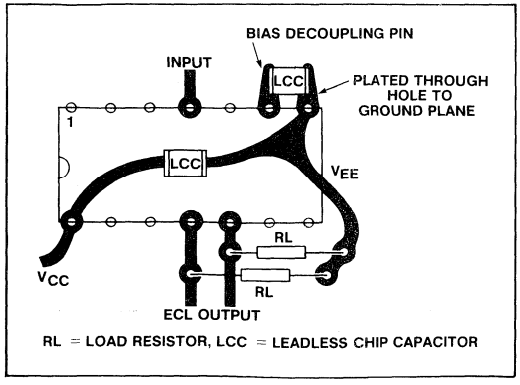


Fig.1 Single point grounding

Also note that in Fig.1 the output load resistors have their grounded ends connected together and a common return used. Because the currents in the resistors are in antiphase, cancellation of the inductive effects taken place, and the path followed by the relatively large output currents is controlled. Defining the ground current path is more important in applications like frequency synthesis, where a relatively large part of the system may be on one PCB.

It is well known that the effect of mismatching a transmission line is to cause variations in the voltage along the line. Standard practice at Plessey Semiconductors has been to use a 5:1 attenuator manufactured from 'microdot' resistors as an attenuator feeding a 50Ω sampling oscilloscope or a power meter. Although a high VSWR will exist on the line from the generator to the test fixture, the theory is that the line from the power meter to the attenuator will be a matched line, and so the power measured is 14dB lower than the power at the device input pin. This method has been proved very successful, even if simple, and offers some advantages over the use of hybrids or directional couplers.

The use of a matched 50Ω system can help, and using microstrip techniques, a track with a defined impedance is reasonably practical. The impedance of a microstrip line is given by:

$$Zo = 377\ (L/w)\ (1/\varepsilon_r)$$

Where L = dielectric thickness, w = width of track and ε_r is the relative permeability of the board material.

Some correction factors have to be applied, and typically, on 1/16 inch glass fibre epoxy board, the following sizes provide a guide to track width

100Ω - 1mm
75Ω - 2mm
50Ω - 4mm

These impedances rely on the ground plane on the obverse of the board being complete, and where boards are wave soldered, it may be necessary to make arrangements to prevent blistering.

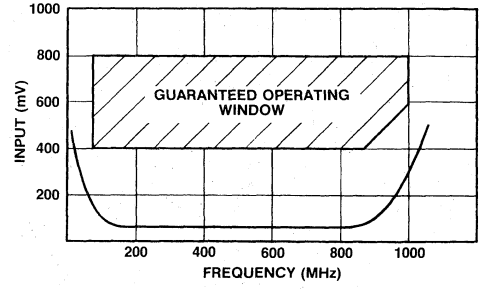


Fig.2 Example of input sensitivity curves

The input level of a divider should be maintained within the guaranteed operating window shown on its data sheet (Fig.2). Excessive input can vary in its effects, from causing permanent damage to miscounting, especially when cold. Running the device at too low a level can cause problems, even though the level is within the 'typical' performance line of the device. An ECL output signal on pin 6 of the device in

Fig.3 can couple 60mV of signal to the input shown on Fig.2 at 500MHz. Such a level of coupling can lead to divider jitter if the input signal is low, and it becomes very necessary to keep the inputs and outputs well separated at the higher frequencies. This includes ECL lines to modulus control pins on two modulus dividers.

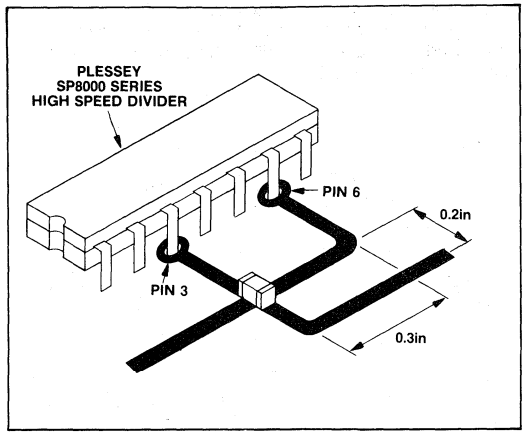


Fig.3 Coupling between parallel tracks

Most dividers are edge triggered, and although they are specified over a frequency range with sine wave input, they will operate to lower frequencies provided a suitably high slew rate is provided on the input signal. This is generally of the order of 100 to 200 volts/microsecond. This should be achieved by shaping of the input signal, for example by limiting, rather than by overdriving the device.

The outputs of devices may be of the following forms:

(1) ECL
(2) Open collector TTL
(3) TTL
(4) CMOS

Of these, the ECL output is well defined; some devices require external load resistors and the data sheet should be consulted. Where these external resistors are required, suitable interconnection techniques should be used between them and the device; the resistors should be carefully chosen for their non-inductive properties when output frequencies are very high. Where an ECL output divider drives another divider it is best to AC couple, since few dividers are strictly ECL-compatible on their inputs.

Open collector TTL outputs are relatively slow. Although the negative edge is limited in speed by the turn-on time of the output transistor, the rising edge is limited by the external load resistor and capacitance to ground. In practice this means that short narrow tracks are required to the following device, and a minimum 'fan-in' load provided. In addition, open collector TTL should not be used above about 10MHz output frequency.

True TTL outputs are not so limited, because of the active pull-up. Nevertheless, the use of such outputs at frequencies above about 25-30MHz is not recommended, especially into capactive loads. Loads of more than 30pF should not be driven faster than about 15MHz. Note that the current drawn by true TTL outputs increases with increasing load capacitance.

CMOS outputs are, on the face of it, TTL-compatible. However, investigation will show that the outputs are not guaranteed to meet TTL levels at TTL currents and it is not recommended that CMOS output devices be used to directly drive TTL. Where an interface of this sort is required, an active transistor interface should be used.

Fig.4 shows a circuit for an ECL-TTL interface, using a line receiver. Simple circuits using one or two transistors cannot be guaranteed to work over all the tolerances of ECL output voltages and temperature ranges.

Interfacing to dividers is not difficult if a few simple rules are obeyed. These are:

(1) Observe the input requirements - guaranteed input operating area, and slew rate.
(2) Do not use open collector outputs above 10MHz.
(3) Do not use CMOS outputs to drive TTL.
(4) Use a sensible layout with good components, and sensible values - 0.1 microfarad ceramic capacitors are NOT bypasses at 1.5GHz.

Treating dividers as RF linear devices is probably the best way to ensure successful applications at high frequencies. There is no magic in HF design, only intelligent layout and sensible component choice.

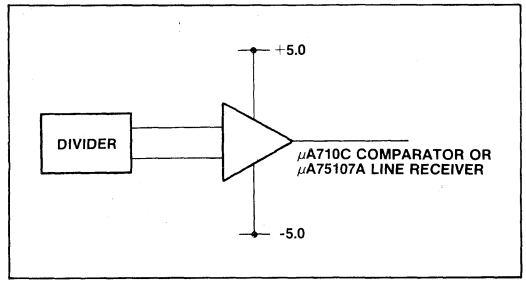


Fig.4 ECL/TTL interface

Impedance Matching

The use of microstrip techniques has been mentioned already. However, in itself this will not produce a matched network and various possibilities exist to improve the matching at the input of a device. These include Tchebycheff impedance transforming networks, narrow band 'L' matching networks, and at high enough frequencies, the use of transmission lines. Wideband matching is often difficult, and attempts should be made to use networks that have the lowest possible working Q. This is for two reasons: firstly a high Q network will not only be narrow band, but will have the capability of increasing the losses, and secondly, a low Q network is generally more tolerant of component variations.

The greater losses in high Q circuits occur because of the greater circulating current: the loss power is I^2R, so that if the Q is doubled with all else constant, the power loss is increased by 4 times.

The easiest method of determining matching components is by means of the Smith Chart.

THE SMITH CHART

The input impedance of SP8000-series high speed dividers varies as a function of frequency and is therefore specified on the datasheets by means of Smith Charts. The following information is included in this handbook as a guide to their interpretation and use.

Construction of the chart

The chart is constructed with two sets of circles, one set comprising circles of CONSTANT RESISTANCE (Fig. 5) and the other circles of CONSTANT REACTANCE (Fig. 6). The values on these circles are normalised to the characteristic impedances of the system by dividing the actual value of resistance or reactance by the characteristic impedance e.g. in a 50Ω system, a resistance of 100Ω is normalised to a value of 2.0.

By combining Figs. 5 and 6 to form Fig. 7, a chart is produced in which any normalised impedance has a unique position on the chart, and the variation of this impedance with frequency or other parameters may be plotted.

A further series of circles may be plotted on the chart: these are circles of constant VSWR, and represent the degree of mismatch in a system. The VSWR is the ratio of the device impedance to the characteristic impedance, and is always expressed as a ratio greater than 1: thus a 25Ω device in a 50Ω system gives rise to a 2:1 VSWR. These circles of constant VSWR have been added in Fig. 7.

Any point can be represented on the Smith Chart: for example an impedance of 150-*j*75Ω can be represented by a normalised impedance (in a 50 Ω system) of 3-*j*1.5 and this point is plotted in Fig. 7 as point A.

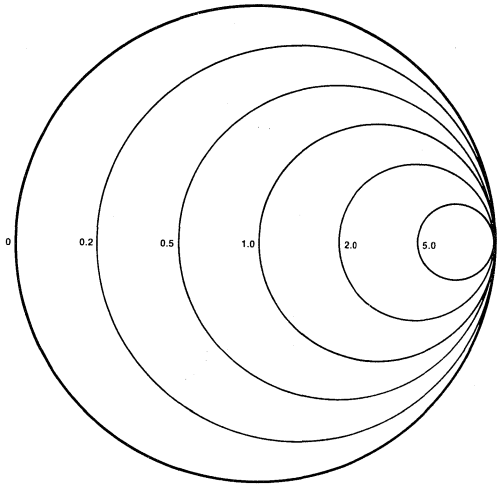


Fig.5 Constant resistance circles

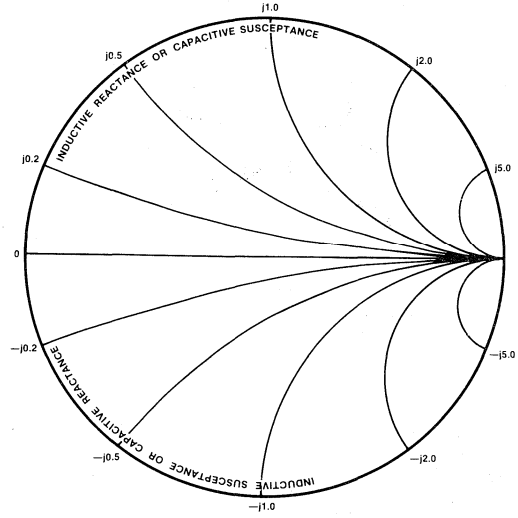


Fig.6 Constant reactance circles

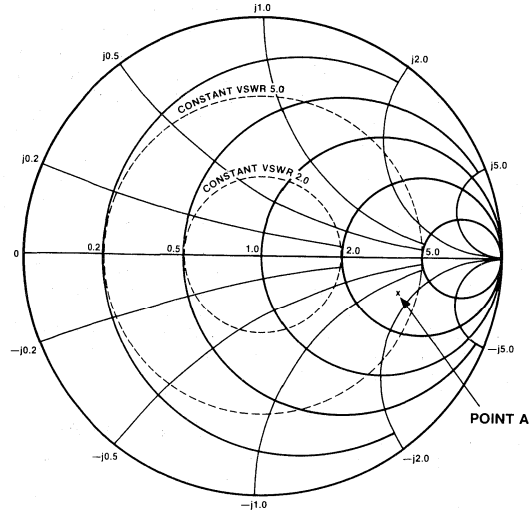


Fig.7 The complete chart

Network calculations

The main application for Smith Charts with integrated circuits is in the design of matching networks. Although these can be calculated by use of the series to parallel (and vice-versa) transforms, followed by the application of Kirchoff's Laws, the method can be laborious. Although the Smith Chart as a graphical method cannot necessarily compete in terms of overall accuracy, it is nevertheless more than adequate for the majority of problems, especially when the errors inherent in practical components are taken into account.

Any impedance can be represented at a fixed frequency by a shunt conductance and susceptance (impedances as series reactance and resistance in this context). By transferring a point on the Smith Chart to a point at the same diameter but 180° away, this transformation is automatically made (see Fig. 8) where A and B are the series and parallel equivalents.

It is often easier to change a series RC network to its equivalent parallel network for calculation purposes. This is because as a parallel network of admittances, a shunt admittance can be directly added, rather than the tortuous calculations necessary if the series form is used. Similar arguments apply to parallel networks, so in general it is best to deal with admittances for shunt components and reactances for series components.

Admittances and impedances can be easily added on the Smith Chart (see Fig. 9). Where a series inductance is to be added to an admittance (i.e. parallel R and C), the admittance should be turned into a series impedance by the method outlined above and in Fig. 8. The series inductance can then be added as in Fig. 9 (see also Fig. 10).

Point A is the starting admittance consisting of a shunt capacitance and resistance. The equivalent capacitive impedance is shown at point B. The addition of a series inductor moves the impedance to point C. The value of this inductor is defined by the length of the arc BC, and in Fig. 10 is $-j0.5$ to $j0.43$ i.e. a total of $j0.93$. This reactance must of course be denormalised before evaluation. Point C represents an inductive impedance which is equivalent to the admittance shown at Point D. The addition of shunt reactance moves the input admittance to the centre of the chart, and has a value of $-j2.0$. Point D should be chosen such that it lies on unity impedance/conductance circle: thus a locus of points for point C exists.

This procedure allows for design of the matching at any one frequency. Wide band matching is more difficult and other techniques are needed. Of these, one of the most powerful is to absorb the reactance into a low pass filter form of ladder network: if the values are suitably chosen, the resulting input impedance is dependent upon the reflection coefficient of the filter.

At frequencies above about 400MHz, it becomes practical to use sections of transmission line to provide the necessary reactances, and reference to one of the standard works on the subject is recommended.

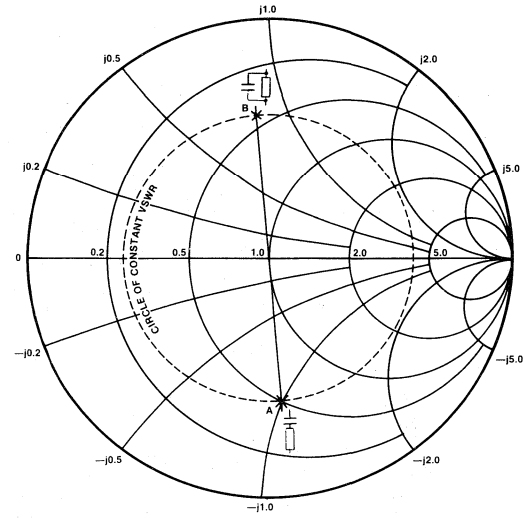


Fig.8 Series reactance to parallel admittance conversion

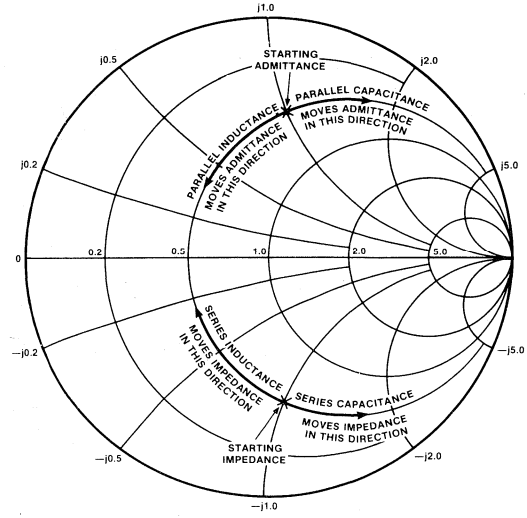


Fig.9 Effects of series and shunt reactance

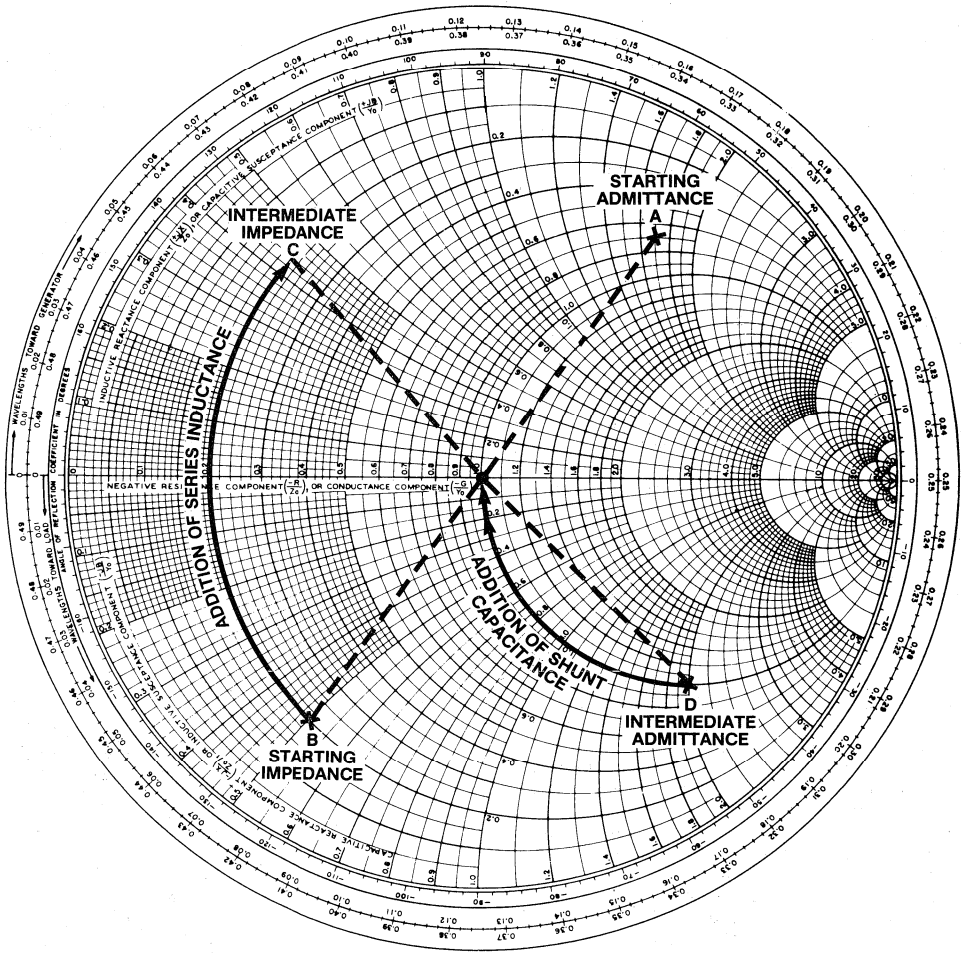


Fig.10 Matching design using the Smith Chart

PHASE NOISE AND DIVIDERS

Phase noise is becoming increasingly important in systems and it is necessary to minimise its effects. First, however, phase noise must be defined.

A spectrally pure signal of a given frequency would appear on a perfect spectrum analyser display as a single straight line as in Fig.11. If the signal is frequency modulated with a discrete modulation frequency, the result will be a comb of frequencies as in Fig.12, while modulation with noise will produce an output spectrum as in Fig.13. Note that the noise density decreases as the offset from the carrier increases. This effect is the result of the effectively lower modulation index *m*. In the case of a Voltage Controlled Oscillator modulated by white noise, a similar effect will be seen, because for a given deviation *f*, the modulation index *m*, (= 1/*fmod*) is greater for lower frequencies than for higher frequencies. Thus the number of sidebands is greater for lower frequencies, and the noise spectral density increases as the carrier is approached.

The causes of phase noise in dividers are not well understood, but the effects of internal noise on the switching point of the various flip-flops cannot be ignored. The 1/*f* noise will obviously inter-relate to the phase noise if this is so, and it is interesting to note that various measurements of Gallium Arsenide dividers suggest performances 20 to 30dB worse than for ECL dividers. Rohde (ref. 4) suggests that TTL and CMOS are much better than ECL, although little work has been published in this field, possibly because of the measurement difficulties.

The non-saturating nature of ECL, the fact that the transistors are designed and processed for high speed rather than low noise, and the smaller signal swings than TTL or CMOS, lead intuitively to the conclusion that ECL should be worse than either of these other two logic families. This appears to be the case, while the high 1/*f* noise knee of Gallium Arsenide devices leads to the high relatively close in phase noise.

Devices with slow output edges, such as open collector TTL output stages may also be expected to be worse, which is again born out in practice.

Minimisation of phase noise requires the use of well-filtered supplies, correct input levels and minimisation of noise in level changing circuitry.

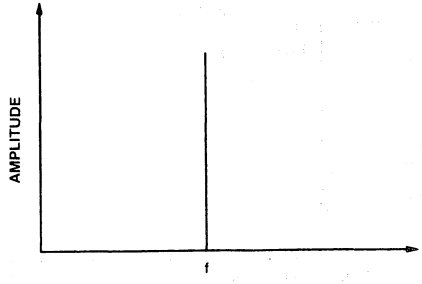


Fig.11 Spectrally pure signal

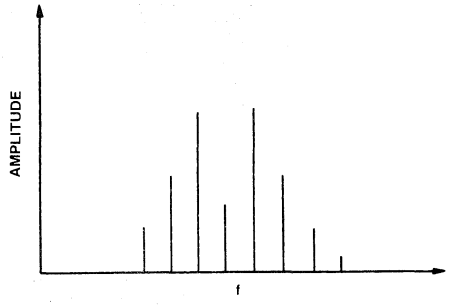


Fig.12 Spectrally pure signal, frequency modulated with single tone

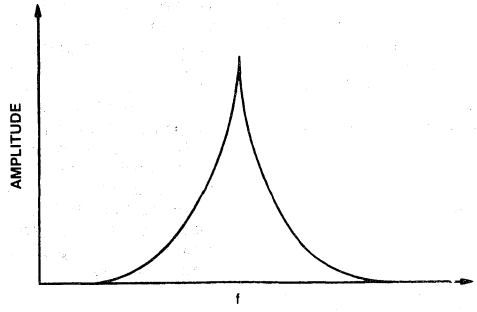


Fig.13 Spectrally pure signal, frequency modulated by noise

REFERENCES

1. Electronic Applications of the Smith Chart, Philip H. Smith, McGraw Hill, 1969.
2. Microwave Filters, Impedance - Matching Networks and Coupling Structures, Matthei, Young, Jones, Artech House 1980. SBN 0890060991.
3. Tables of Chebyshev Impedance Transforming Networks of Low Pass Filter Form, Matthei G.L., Proc IEEE August 1964 pp 939 - 963.
4. Digital PLL Frequency Synthesis Theory and Design V.L. Rohde, Prentice Hall 1983 ISBN 0-13-214239-2.

Tuned Amplifier Application for the SL6140

AN45

The SL6140 wideband AGC amplifier, when used in a 50Ω system, has a gain of 15dB. By tuning, or matching, the inputs and outputs of the device the gain can be increased. This produces a higher gain amplifier that will work over a limited bandwidth. The bandwidth of the amplifier depends on the Q factor of the tuned/matching circuits used.

Fig. 1 shows a single ended amplifier with a tuned input and output network.

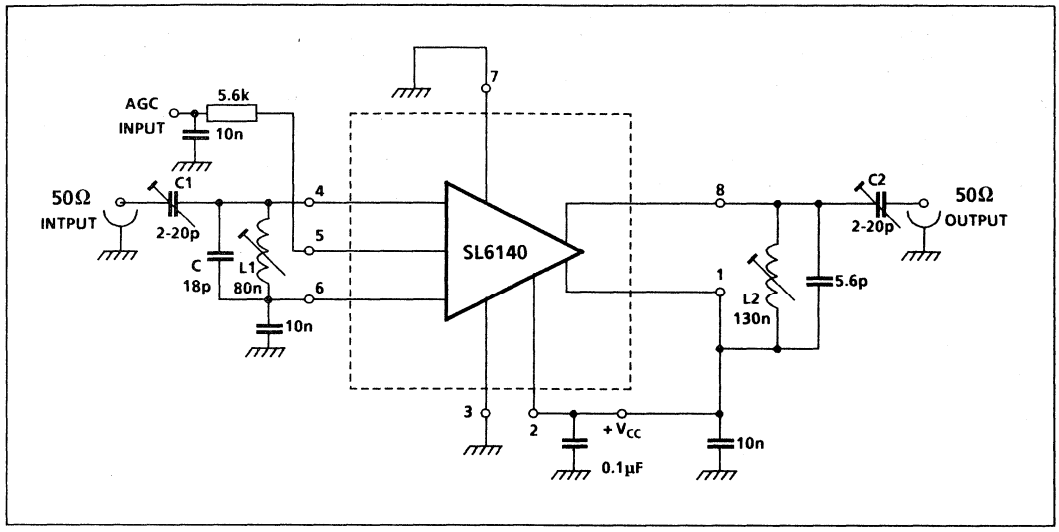


Fig. 1 A 100MHz tuned amplifier application with 35dB power gain

The input circuit consists of a parallel LC network connected across the differential inputs. The input signal is applied to one input, via a coupling capacitor (C1), the other input being decoupled. The coupling capacitor also forms part of the impedance matching network, matching a 50Ω source with the high input impedance of the device (see Smith chart, Fig. 7 of data sheet) .

The tuned frequency is given by the following equation:;

$$f = \frac{1}{2\Pi \frac{\sqrt{L \times C \times C1}}{\sqrt{(C + C1)}}}$$

The output circuit consists of a parallel LC network connected from one of the open collector outputs of the device to Vcc. The other output is connected directly to Vcc. The coupling capacitor (C2) and LC network transforms the 50Ω load to a high impedance load for the open collector outputs of the device, hence improving the gain.

By adjusting C1 and C2 the gain can be optimised, but if too high an impedance is seen by the input or output of the device the circuit may oscillate. LI and L2 are adjusted to set the tuned frequency.

The high gain is achieved at the expense of bandwidth, so for maximum gain the matching network should be adjusted to provide the minimum bandwidth necessary for the particular application.

An alternative method of tuning the output of the device is to transformer-couple to the 50Ω load. The primary winding is connected across the outputs (a centre tap providing Vcc) and resonated, at the required frequency, with a capacitor, see Fig 2. This circuit has a 6dB improvement in gain over the previous circuit as both outputs are used.

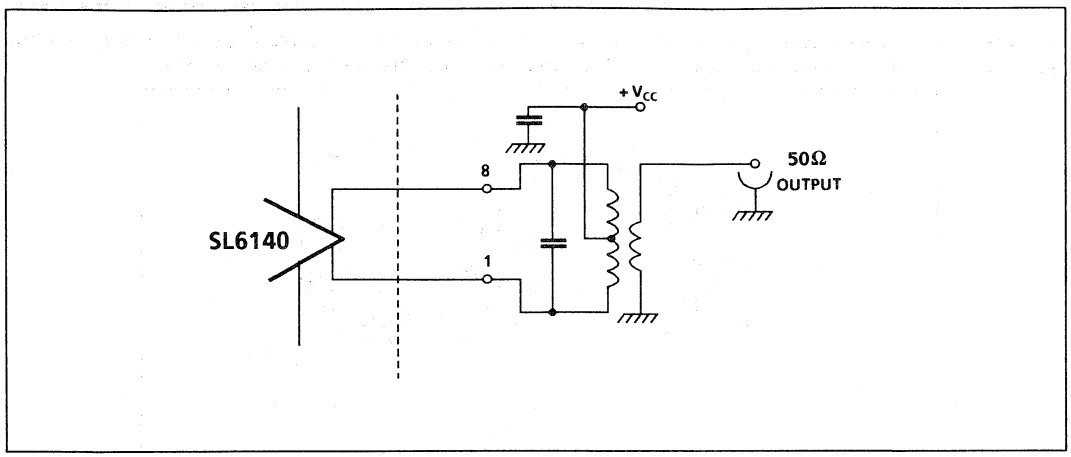


Fig2, Differential tuned output

For best performance a ground plane should be used with 50Ω track from the matching networks to the 50Ω source and load. Also the matching network and decoupling capacitors should be positioned as close to the device as possible.

If a very high gain low bandwidth amplifier is required the addition of some shielding between input and output may be necessary to prevent oscillation.

SL6639 Demonstration Board

This application note describes a demonstration board using the SL6639 at 153MHz and a data rate of 512 bps. Modifications to the board for applications at other frequencies and data rates are also described.

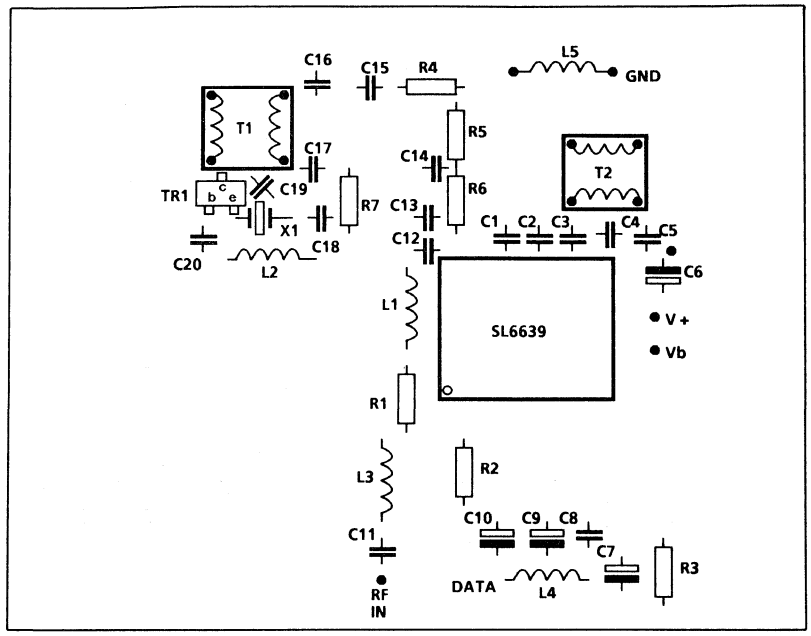


Fig. 1 Component layout - not to scale, for reference purposes only

COMPONENT LIST FOR FIG.1

Capacitors				Resistors	Inductors	Transformers
C1	1nF	C11	1nF	R1 2.2kΩ	L1 10μH	T1 1:1 transformer
C2	1nF	C12	1nF	R2 180kΩ *	L2 220nH	T2 Primary/secondary inductance = 200nH
C3	1nF	C13	10pF	R3 12kΩ	L3 180nH	
C4	5.6pF	C14	1nF	R4 100Ω	L4 470μH (optional)	
C5	1nF	C15	10pF	R5 100Ω	L5 10μH (optional)	**Miscellaneous**
C6	2.2μF	C16	1nF	R6 100Ω		IC1 SL6639
C7	2.2μF	C17	5.6pF	R7 100Ω		TR1 SOT-23 transistor with $f_t \geq 1.3$GHz
C8	1nF	C18	4.7pF	* Selected to give required filter cut off frequency.		X1 153MHz 7th overtone crystal
C9	2.2μF	C19	10pF			
C10	2.2μF	C20	1nF			

OPERATION AT OTHER FREQUENCIES AND DATA RATES

The values given in the components list are appropriate for frequencies norminally around 153MHz. In order to use the receiver at other frequencies it is necessary to change the capacitors which are resonant with the transformers T1 and T2. These are C18 in series with C19, and C4, respectivley. The ratio of C18 to C19 should be kept approximately the same as specified for 153MHz operation.

It is also necessary to change the values of capacitors C13 and C15 such that the reactance of these is equal to 100Ω at the required frequency. It is of course necessary to use a crystal of the required frequency and stability.

In order to use the receiver at higher data rates it is only necessary to reduce the value of C8. For example, at 1200 bps, C8 = 470pF.

NB. This PCB has been designed specifically to demonstrate terminal sensitivity. It is possible to connect an antenna to the board with suitable matching but no guarantee can be given regarding field strength sensitivity. However, with a suitably designed combination of PCB and antenna, a sensitivity of 5μV/M should be attainable.

NJ88C30 VHF Frequency Synthesiser

The NJ88C30 is a low power CMOS integrated circuit which contains all the logic required for a VHF PLL synthesiser. The circuit contains a reference oscillator and divider, a two-modulus prescaler and 4-bit control register, a 12-bit programmable divider, a phase comparator and the necessary data input and control logic. The functional block diagram is shown in Fig.1.

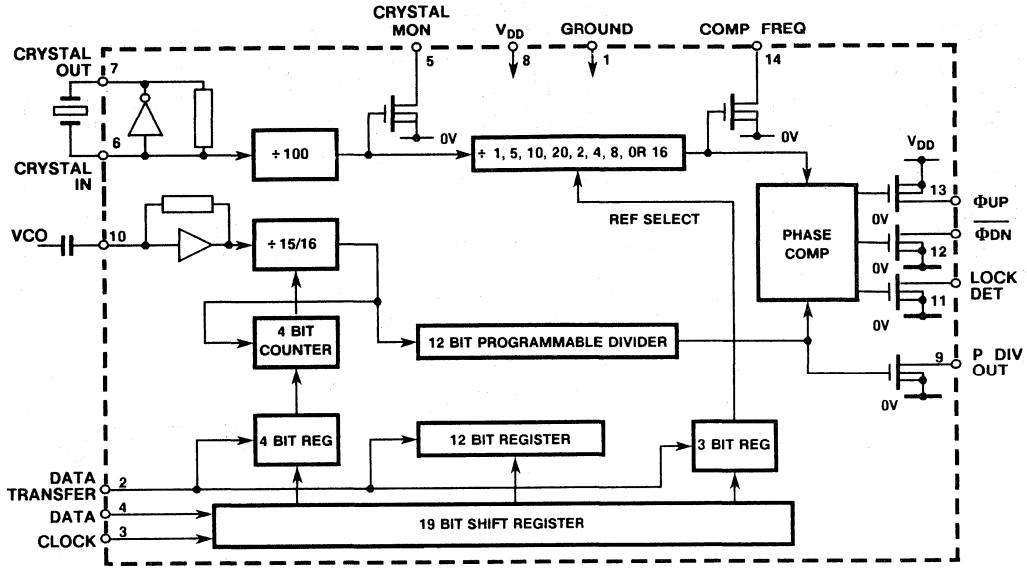


Fig.1 NJ88C30 block diagram

In this application, the NJ88C30 is configured as part of a high band VHF synthesiser, as shown in Fig.2. The loop filter, which comprises IC2a, R3, R4 and C4, is designed using the following equations:

$$R3C4 = K/\omega_n^2$$
$$R4C4 = 2\delta/\omega_n$$
$$K = GKOV_{CC}/2\pi N$$

where

ω_n = Natural loop bandwidth = 440rad/s
δ = Damping factor = 0.7
KO = VCO gain = 6.3×10^6 rad/Vs
V_{CC} = Charge pump supply voltage = 5V
N = Division ratio (f_{out}/f_{comp}) = 14400 (12.5kHz ref)

$$G = \frac{\text{Buffer supply voltage}}{\text{Charge pump supply voltage}} = 3$$

CONSTRUCTION

A PCB layout is illustrated in Fig.3. It will be noticed that the ground plane is split between the VCO and synthesiser control sections of the PCB. DC connection is made via narrow tracks on either side of the board. This construction prevents ground currents from the synthesiser causing spurious sidebands in the VCO output.

The VCO may be modulated externally by the addition of three components: L5, D3 and VC2 (not included). Some adjustment of L1 is necessary to compensate for the additional capacitance. The modulating signal is AC coupled to the MOD pin.

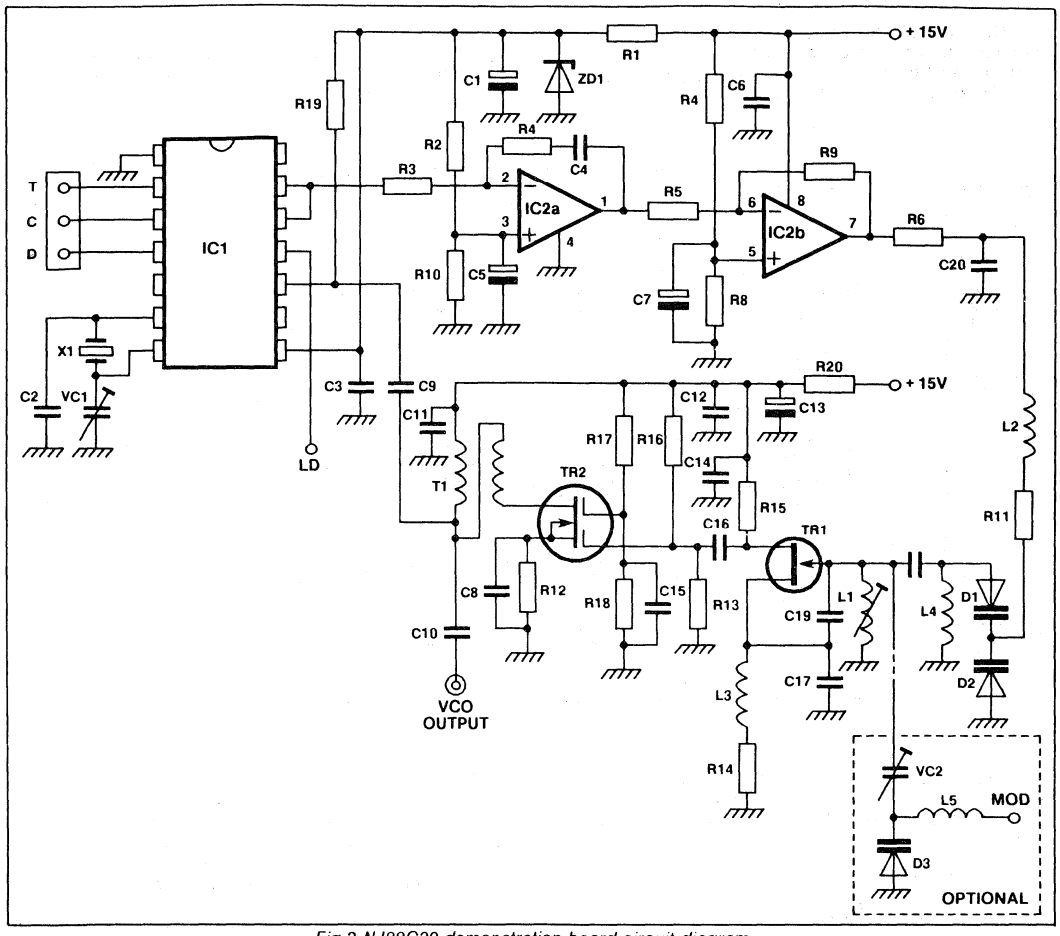


Fig.2 NJ88C30 demonstration board circuit diagram

COMPONENTS LIST

R1	1k	C1	10µ	L1	3.5 turns on Toko S18 former (alloy core)
R2	100k	C2	47p	L2	4.7µH
R3	5.6k	C3	100n	L3	1µH
R4	3.3k	C4	1µ (non-polar)	L4	4.7µH
R5	10k	C5	10µ	L5	4.7µH*
R6	22k	C6	100n	T1	3 turns 36 SWG enamelled wire, bifilar wound on B62152A7X1 (LF) 2-hole Ferrite bead
R7	100k	C7	10µ		
R8	100k	C8	1n		
R9	10k	C9	22p	TR1	J310
R10	100k	C10	33p	TR2	BF961
R11	100Ω	C11	1n	D1	BB109B (Varicap)
R12	100Ω	C12	100n	D2	BB109B
R13	27k	C13	33µ	D3	BB109B*
R14	470Ω	C14	10n	ZD1	5.1V Zener diode
R15	100Ω	C15	1n	X1	10MHz series resonant crystal, 50ppm
R16	220k	C16	22p	IC1	NJ88C30
R17	220k	C17	18p	IC2	TL072
R18	100k	C18	4.7p		
R19	22k	C19	3,9p		
R20	100Ω	C20	47n		
		VC1	5-65p		
		VC2	2-10p*		

*Optional components for modulation input

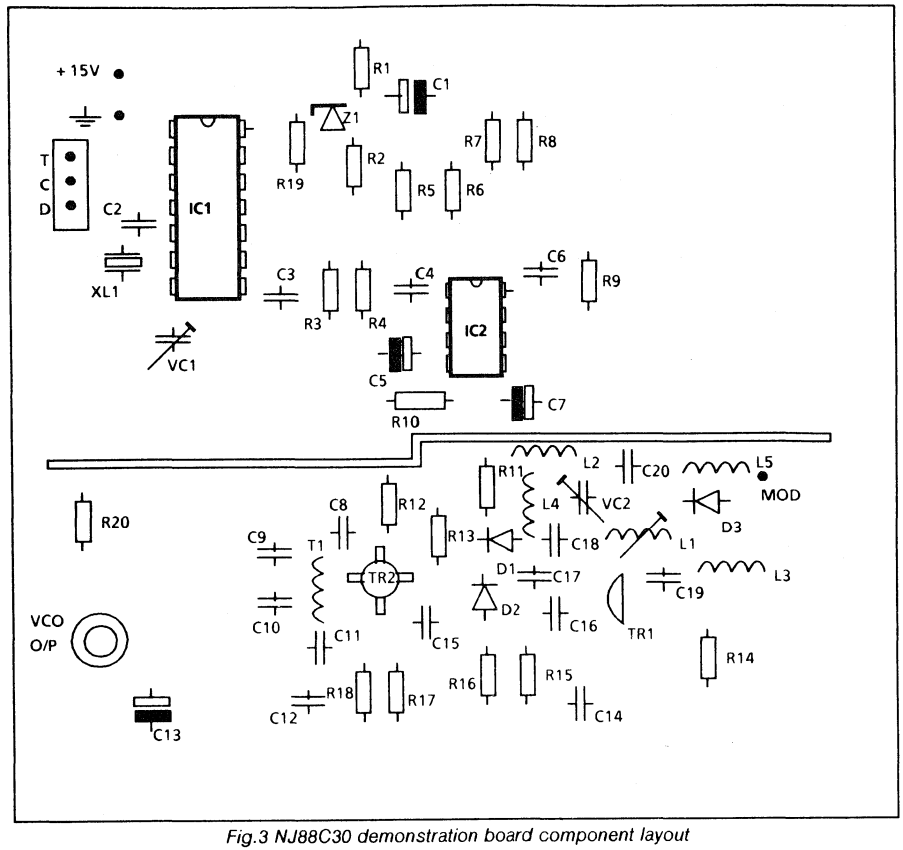


Fig.3 NJ88C30 demonstration board component layout

PERFORMANCE

The output spectrum of the synthesiser is shown in Fig.4. It will be seen that the reference sidebands are very low (≤-80dBc). The output power is 9.4dBm into 50Ω and the frequency swing is about 10MHz, i.e. between 170MHz and 180MHz in this application.

With modulation applied to the VCO and the deviation held constant at 5kHz, the demodulated audio is undistorted at all modulation frequencies above 100Hz.

The lock-up time for a single channel step (12.5kHz is of the order of 10ms and the worst-case lock-up time for a large frequency change is less than 100ms.

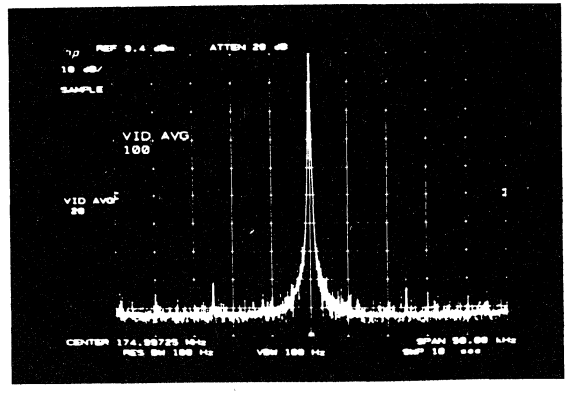
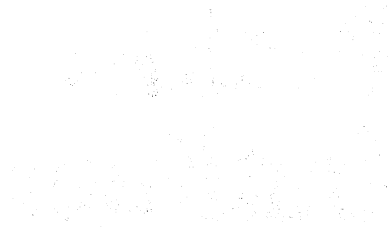
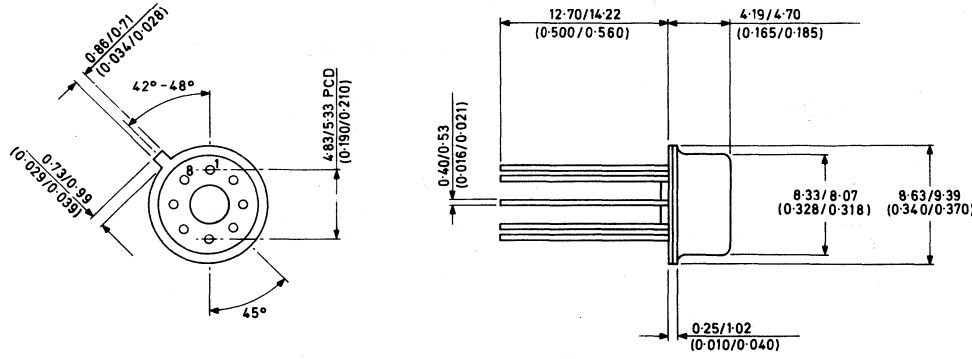


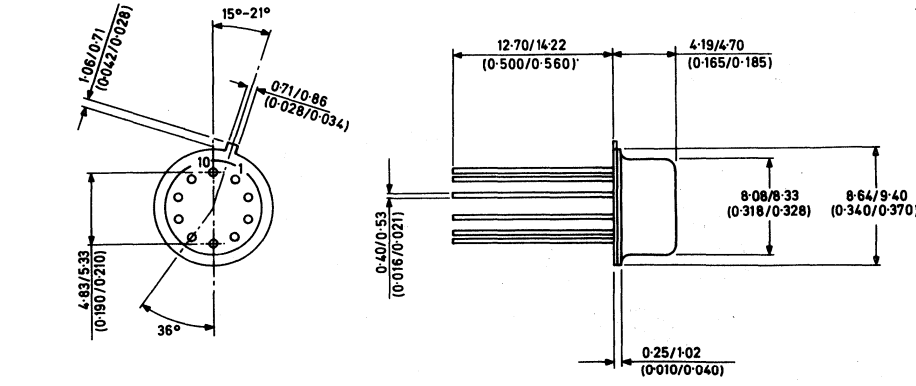
Fig.4

Package Outlines

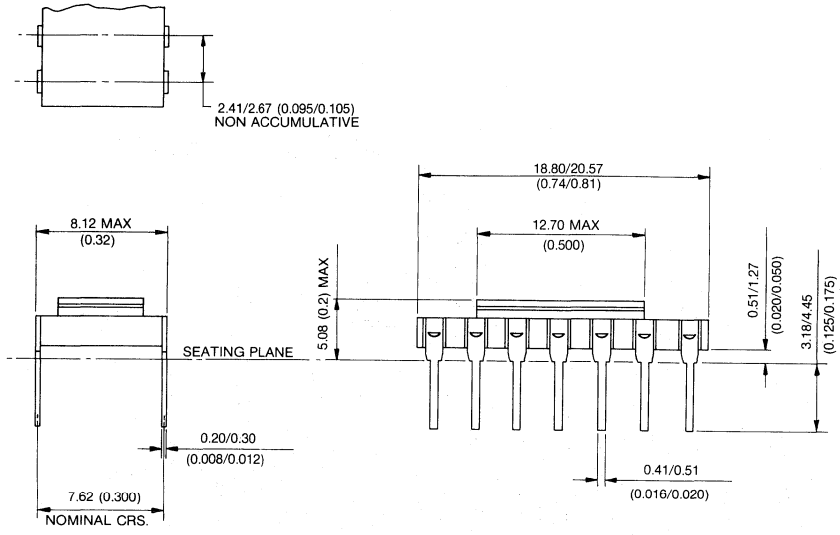




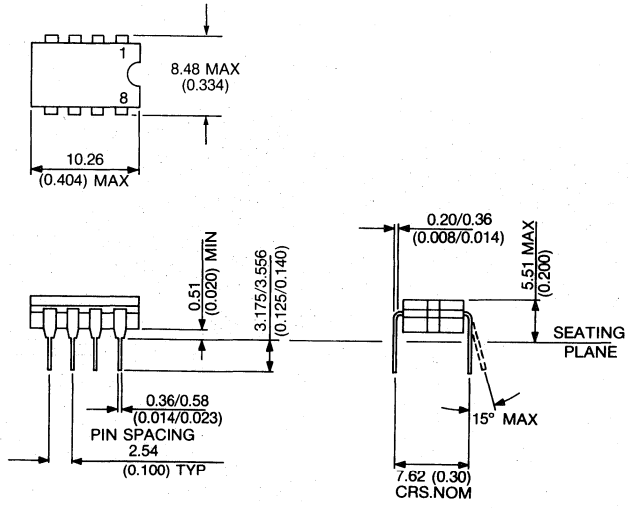
8 LEAD TO-5 (5.08mm PCD) WITH STANDOFF - CM8/S



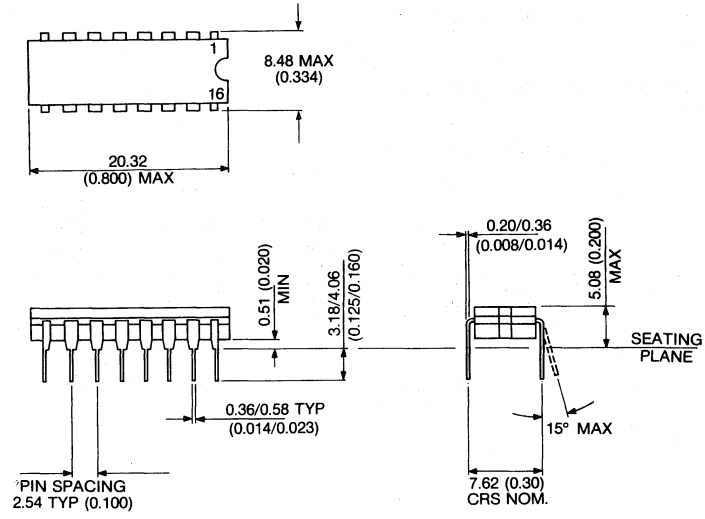
10-LEAD METAL CAN - CM10



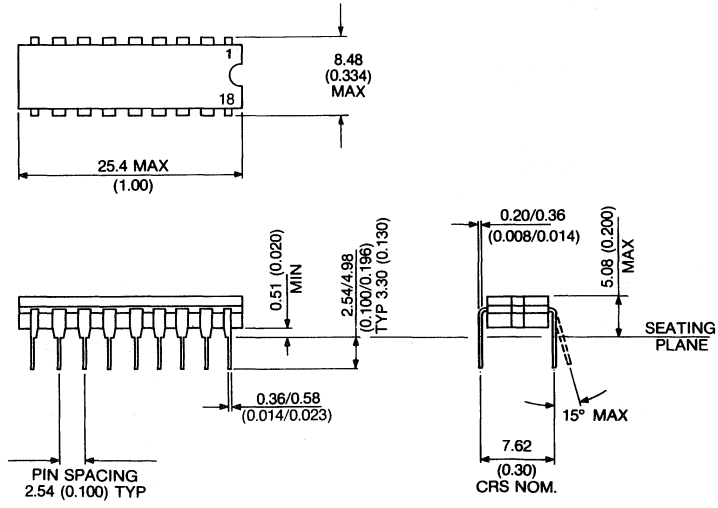
14-LEAD SIDEBRAZED CERAMIC DIL - DC14



8-LEAD CERAMIC DIL - DG8



16-LEAD CERAMIC DIL - DG16



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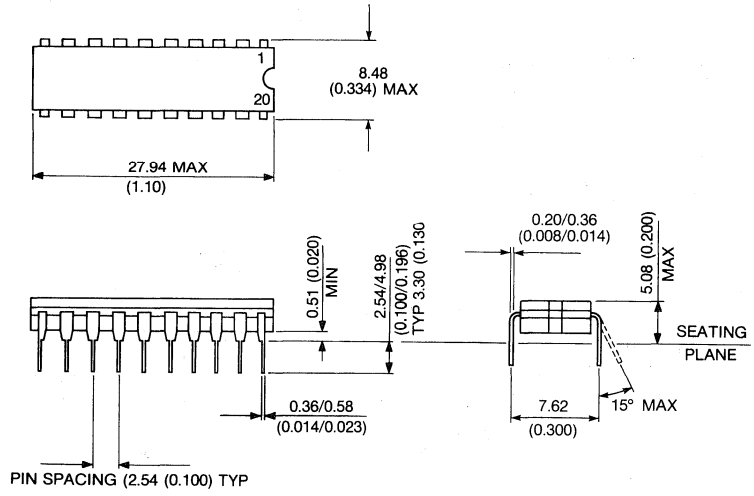
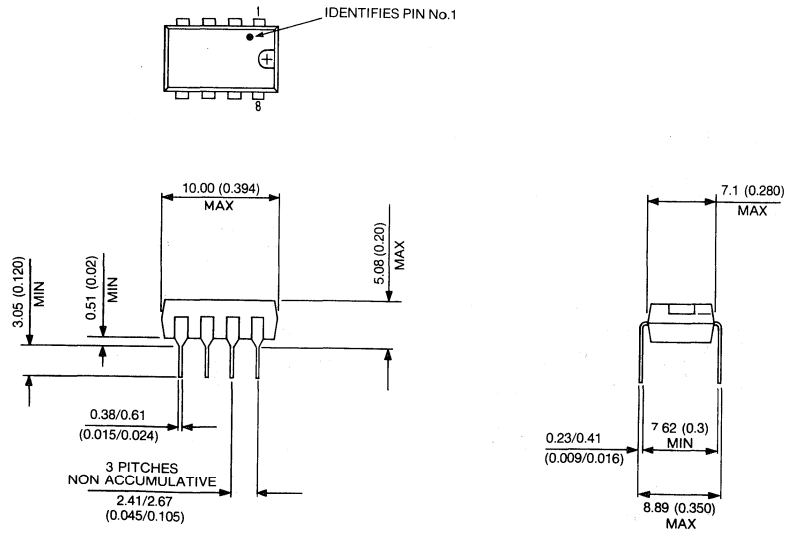
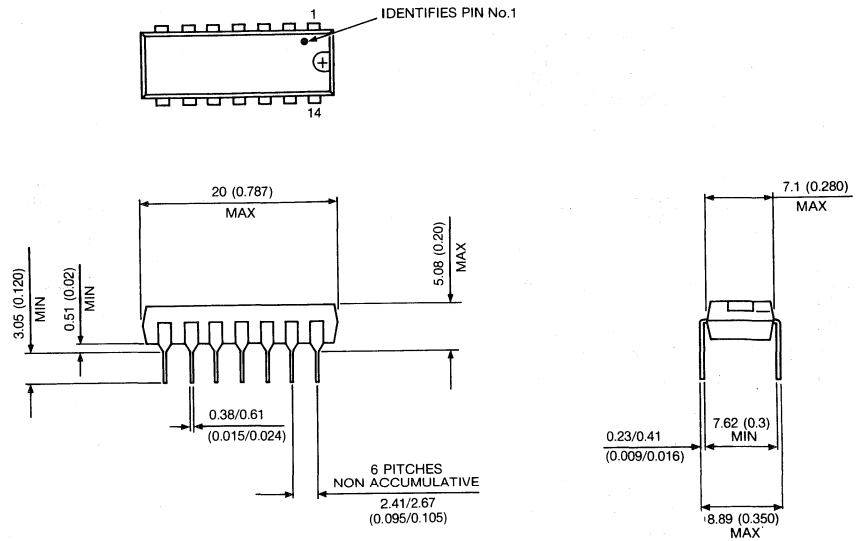


20 LEAD CERAMIC DIL
CERDIP - DG20



8-LEAD PLASTIC DIL - DP8



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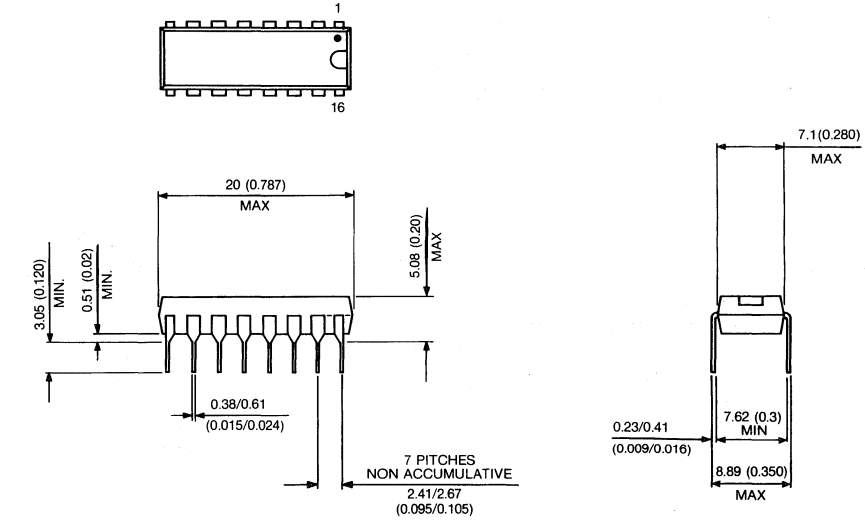

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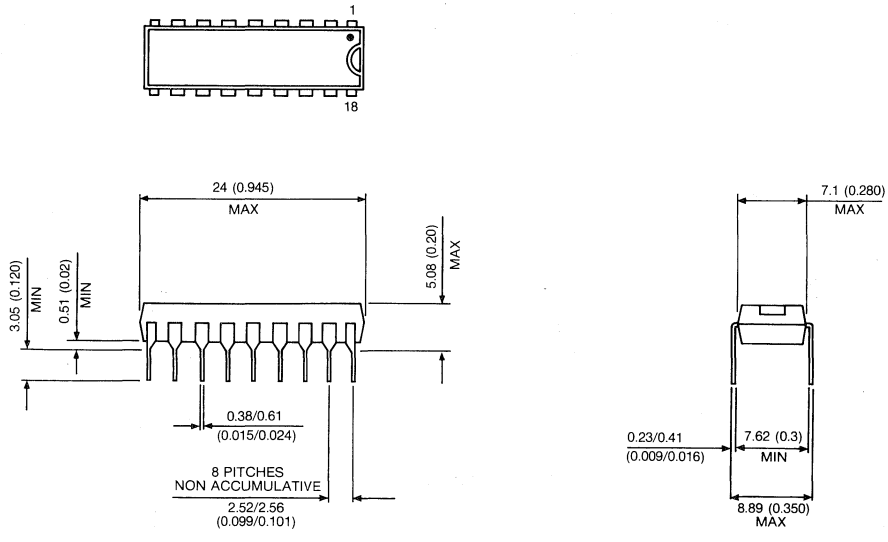
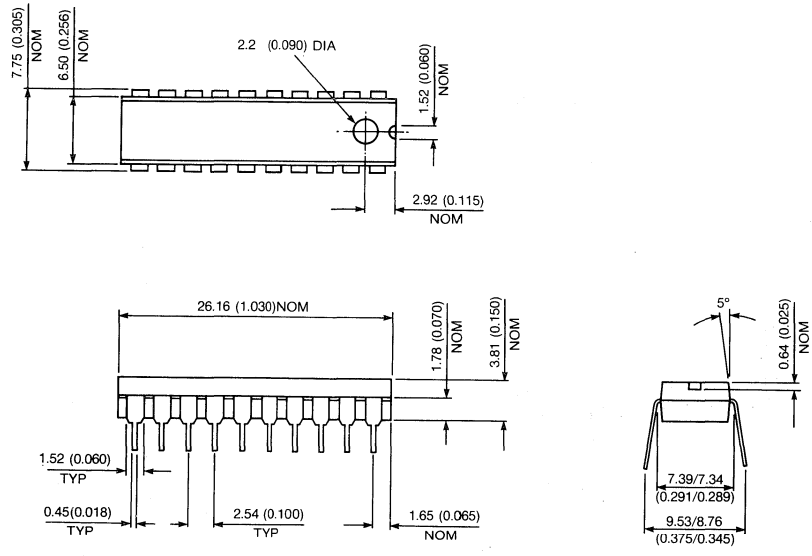


18-LEAD PLASTIC DIL - DP18



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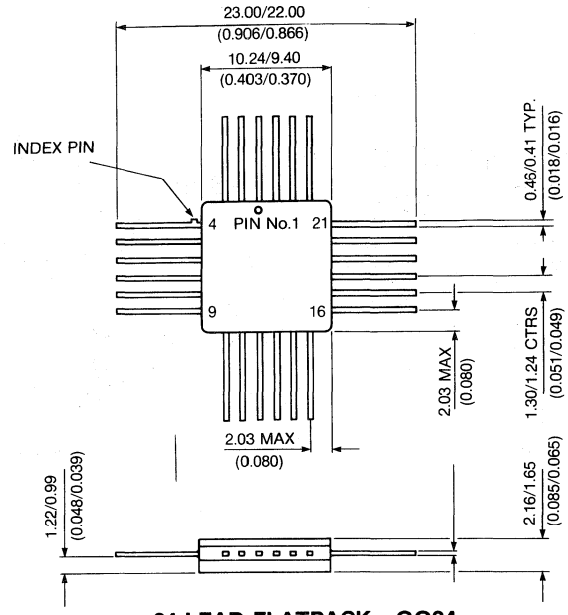
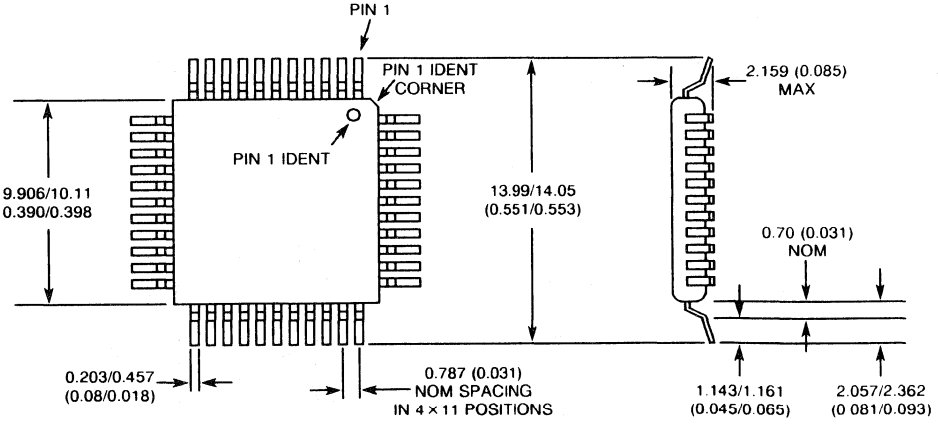
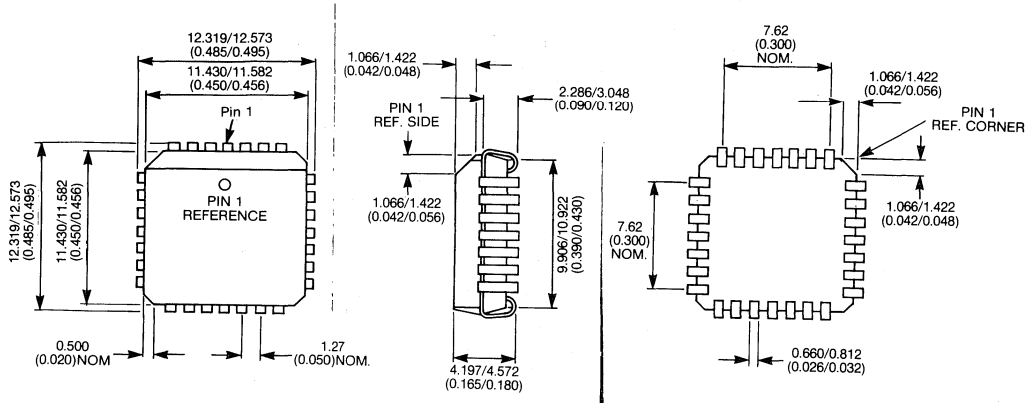


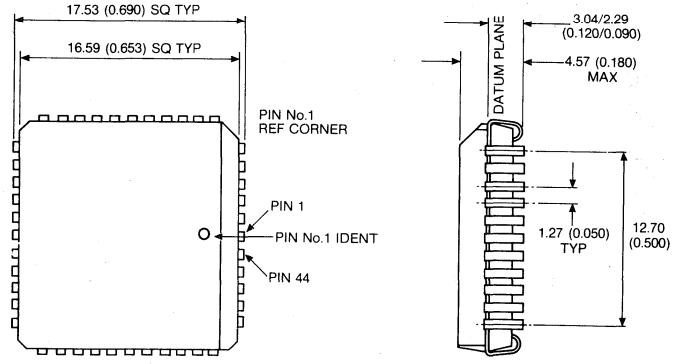
24 LEAD FLATPACK - GG24



44-LEAD PLASTIC QUAD FLATPACK - GP44



28-LEAD QUAD PLASTIC J LEAD - HP28



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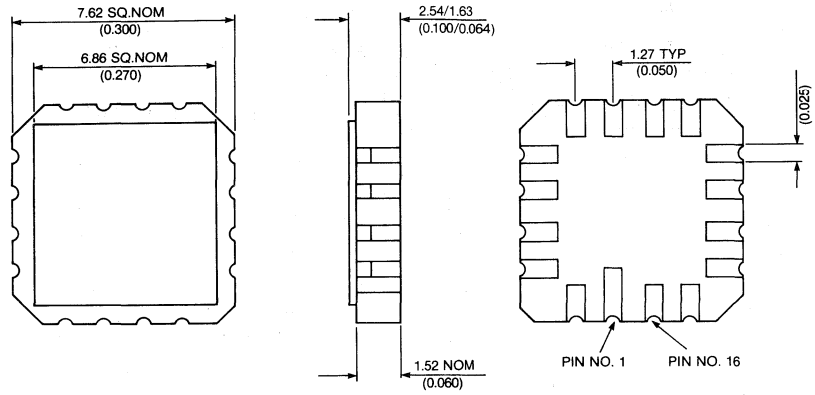
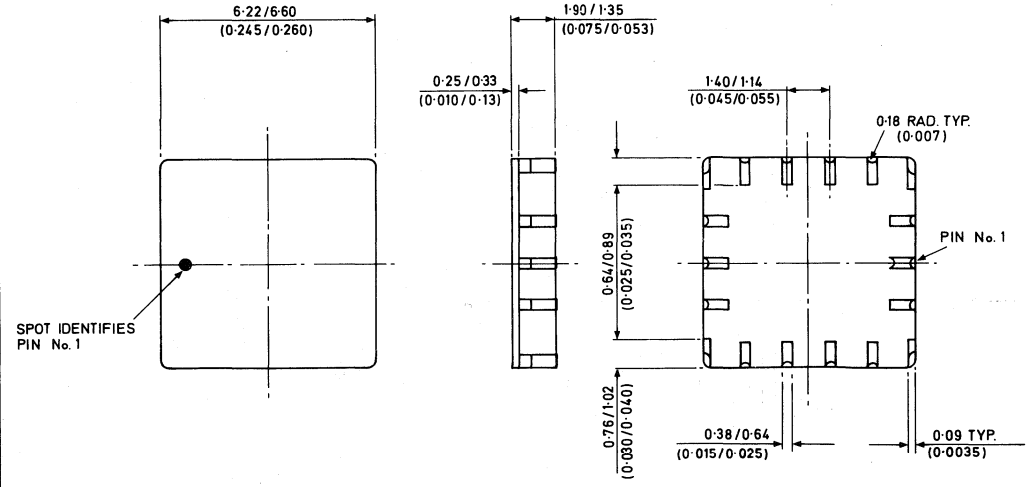


16-PIN LEADLESS CHIP CARRIER - LC16
(HERMETIC)



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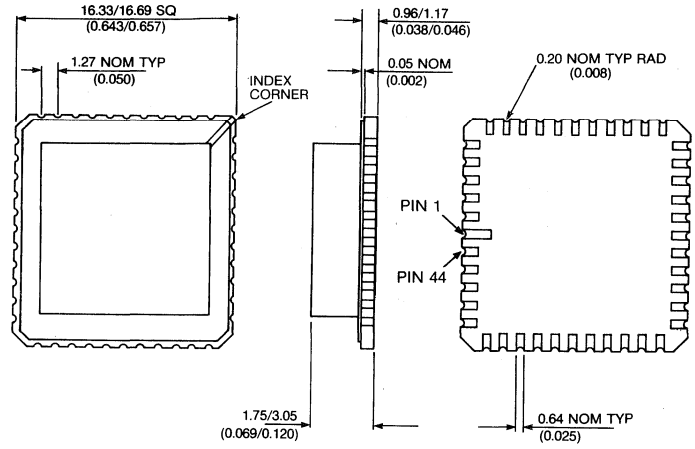
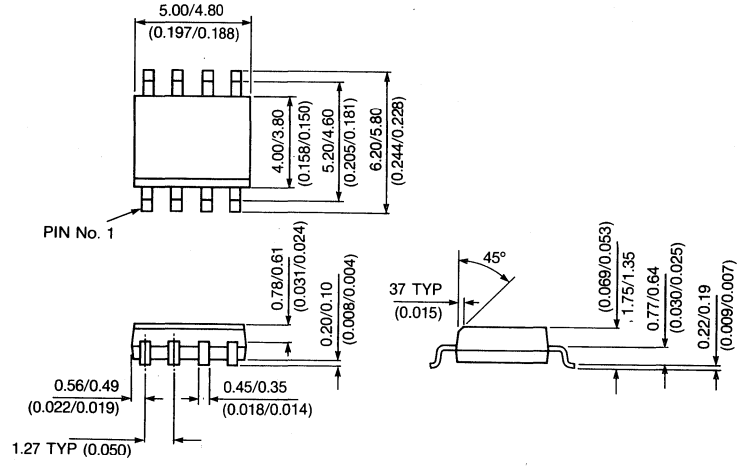
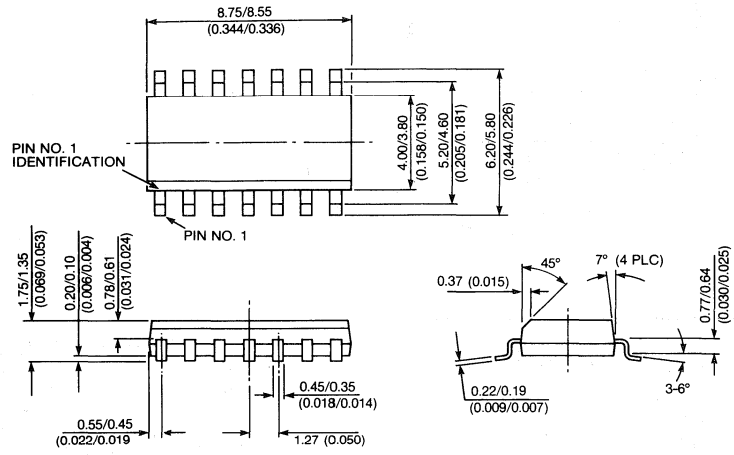


44-PIN LEADLESS CHIP CARRIER - LE44
(NON-HERMETIC)



8-LEAD MINIATURE PLASTIC DIL - MP8



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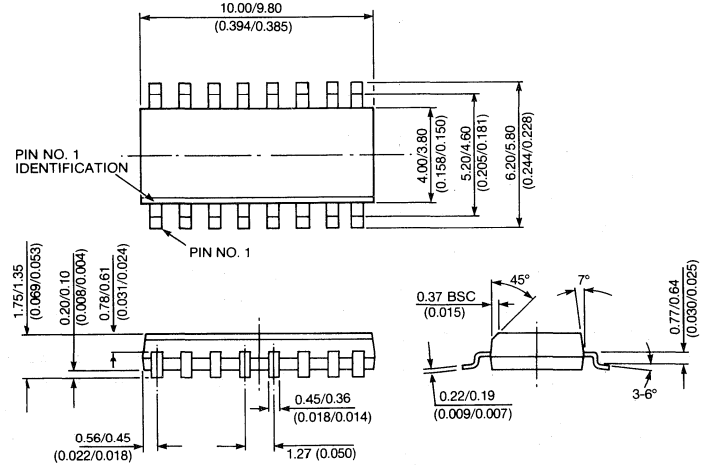

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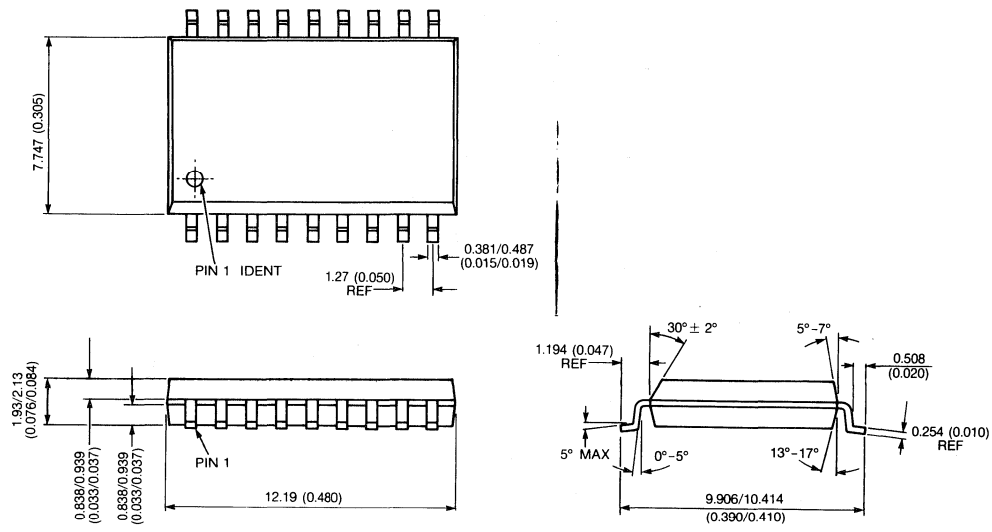

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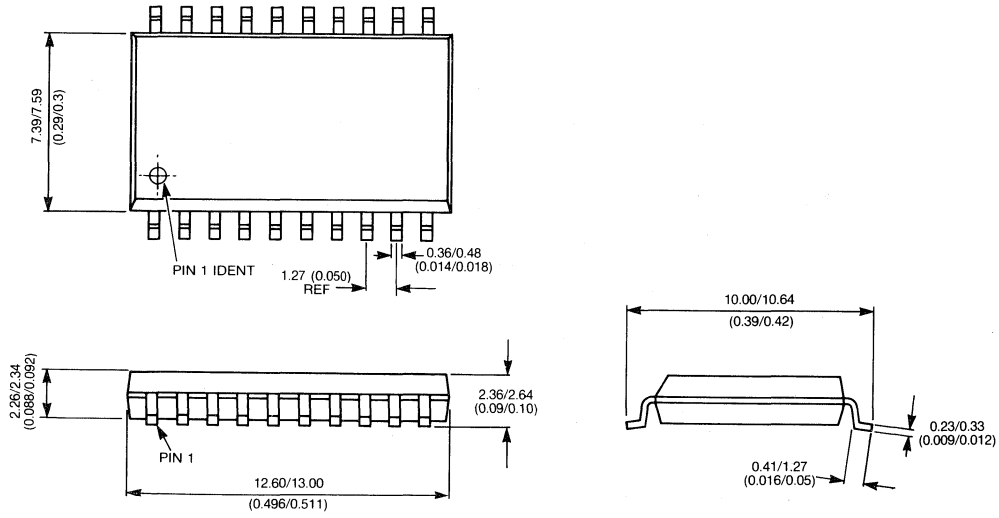

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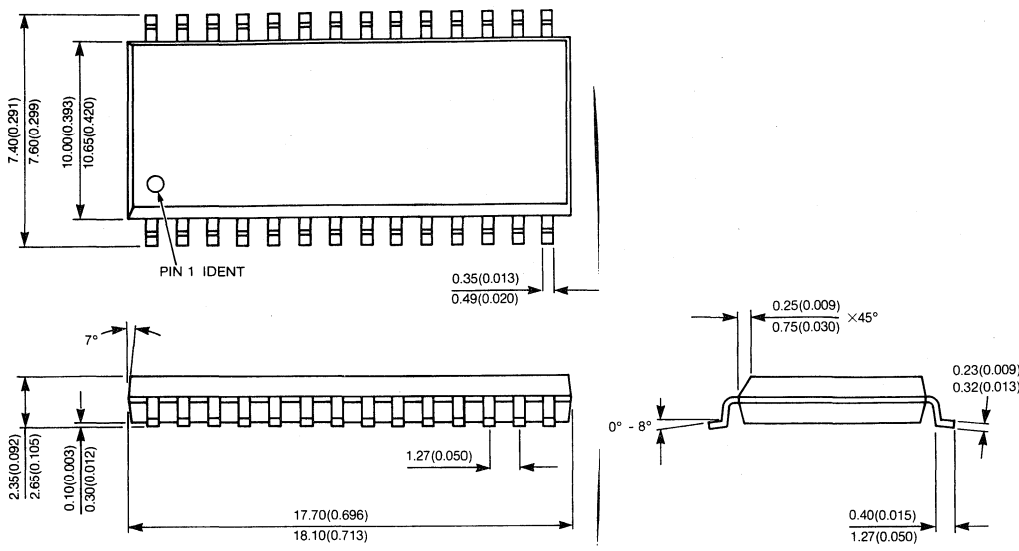


28-LEAD MINIATURE PLASTIC DIL - MP28

Stop Press

NJ88C33

FREQUENCY SYNTHESISER (I^2C BUS PROGRAMMABLE) WITH CURRENT SOURCE PHASE DETECTOR OUTPUTS

The NJ88C33 is a synthesiser circuit fabricated on Plessey Semiconductors' 1.4 micron CMOS process, assuring very high performance. It is I²C compatible and can also be programmed at up to 2MHz. It contains a 16-bit R counter, a 12-bit N counter and a 7-bit A counter.

A digital phase comparator gives improved loop stability with current source outputs to reduce loop components. A voltage doubler is provided for the loop driver to give a wide control voltage range to the VCO.

FEATURES

- Easy to Use
- Low Power Consumption (15 mW)
- Digital Phase Comparator with Current Source Outputs
- Serial (I²C Compatible) Programming, 2MHz max; Channel Loading in 20μs
- 120MHz Input Frequency Without Prescaler at 4.5V (50MHz at 2.5V)
- Standby Modes
- Use of Two-Modulus Prescaler is Possible

APPLICATIONS

- Cordless Telephones (CT2)
- Cellular Telephones (GSM, ETACS)
- Hand Held Portable Radios
- Sonarbuoys

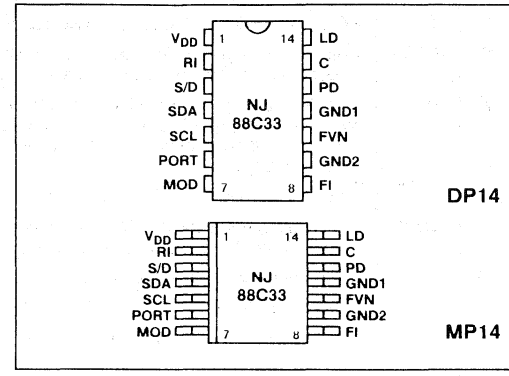


Fig.1 Pin connections (not to scale) - top views

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	-0.3V to 7V
Input voltage, V_{IM1}	-0.3V to V_{DD} + 0.3V
Output voltage on pin 13, V_{IM2}	-V_{DD} to 0V
Storage temperature, T_{stg}	-55°C to + 125°C

ORDERING INFORMATION

NJ88C33 DP (Industrial - Plastic DIL package)
NJ88C33 MP (Industrial - Miniature Plastic DIL package)

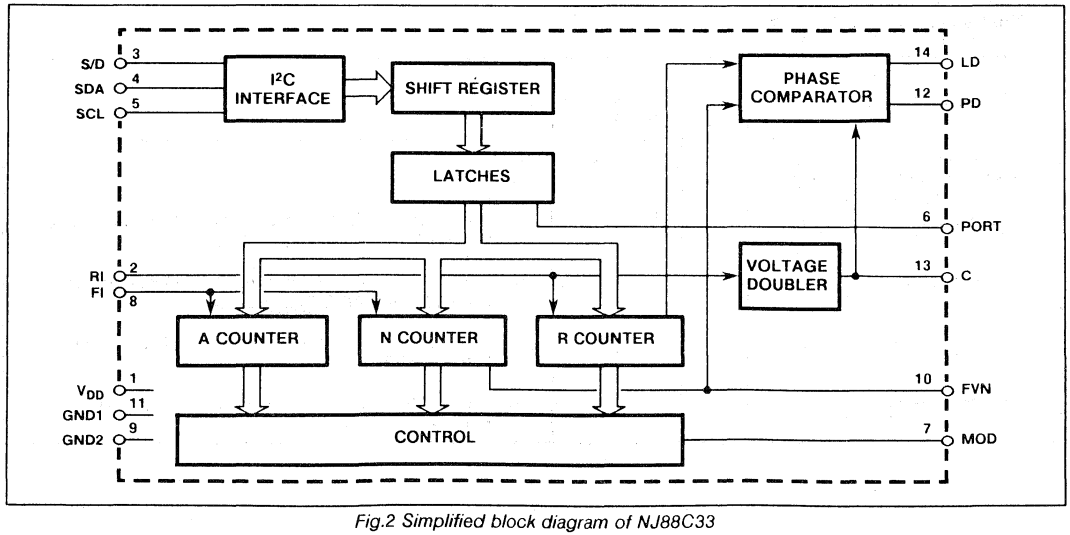


Fig.2 Simplified block diagram of NJ88C33

PIN DESIGNATIONS

Pin No.	Pin Name	Description
1	V_{DD}	Supply voltage (normally 5V or 3V).
2	RI	Reference frequency input from an accurate source, normally a crystal oscillator. The input should be AC coupled.
3	S/D	Single/dual modulus operating mode selection input. Single modulus operation is selected by driving the pin low. 'High' selects dual modulus mode.
4	SDA	I²C bus data input pin. It is also an open-drain output for generating I²C bus acknowledge pulses.
5	SCL	I²C bus clock input. It can be clocked at up to 2MHz.
6	PORT	Output control pin, which can be programmed via the I²C bus. It can be connected to the S/D pin to select single or dual modulus mode under bus control.
7	MOD	Modulus control pin. It is high in single modulus mode but switches in dual modulus operation. In dual modulus mode, MOD remains low during operation of the A counter until A = 0; MOD then remains high until N = 0, when both counters are reloaded. It can be programmed via the I²C bus as an open-drain or push-pull output.
8	FI	Frequency input from a VCO or prescaler. The input should be AC coupled.
9	GND2	Dedicated ground for the FI input buffer. It should be connected to the VCO ground or the prescaler ground, if used. Any noise on this pin will affect the performance of the VCO loop.
10	FVN	Open-drain output from the N counter.
11	GND1	Ground supply pin (global).
12	PD	Tristate current output from the phase detector. The polarity of the output can be programmed via the I²C bus.
13	C	Voltage doubler output. The operation of the doubler can be controlled via the I²C bus. In applications where the voltage doubler is switched off, this pin should be connected to GND1; a reservoir capacitor should be connected from this pin to GND1 for applications where it is switched on.
14	LD	Open-drain lock detect output - requires integration if used.

OPERATING RANGE

Test conditions (unless otherwise stated):
PLL locked, RI = 10MHz

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	2.5	5	5.5	V	
Ambient temperature	T_{amb}	-40		+85	°C	
Supply current						
Single modulus	I_{DD}		2.5		mA	FI = 50MHz, V_{FI} = 150mV, N,R > 1000 without voltage doubler, V_{DD} = 5V, T_{amb} = 25°C
Dual modulus	I_{DD}		2		mA	FI = 10MHz, V_{FI} = 500mV, N,R > 1000 without voltage doubler, V_{DD} = 5V, T_{amb} = 25°C
Standby mode	I_{DD}			1	μA	FI = 50MHz, V_{FI} = 150mV, preamp off, divider off, V_{DD} = 5V, T_{amb} = 25°C
Standby mode	I_{DD}		1.5		mA	FI = 50MHz, V_{FI} = 150mV, preamp on, divider off, V_{DD} = 5V, T_{amb} = 25°C

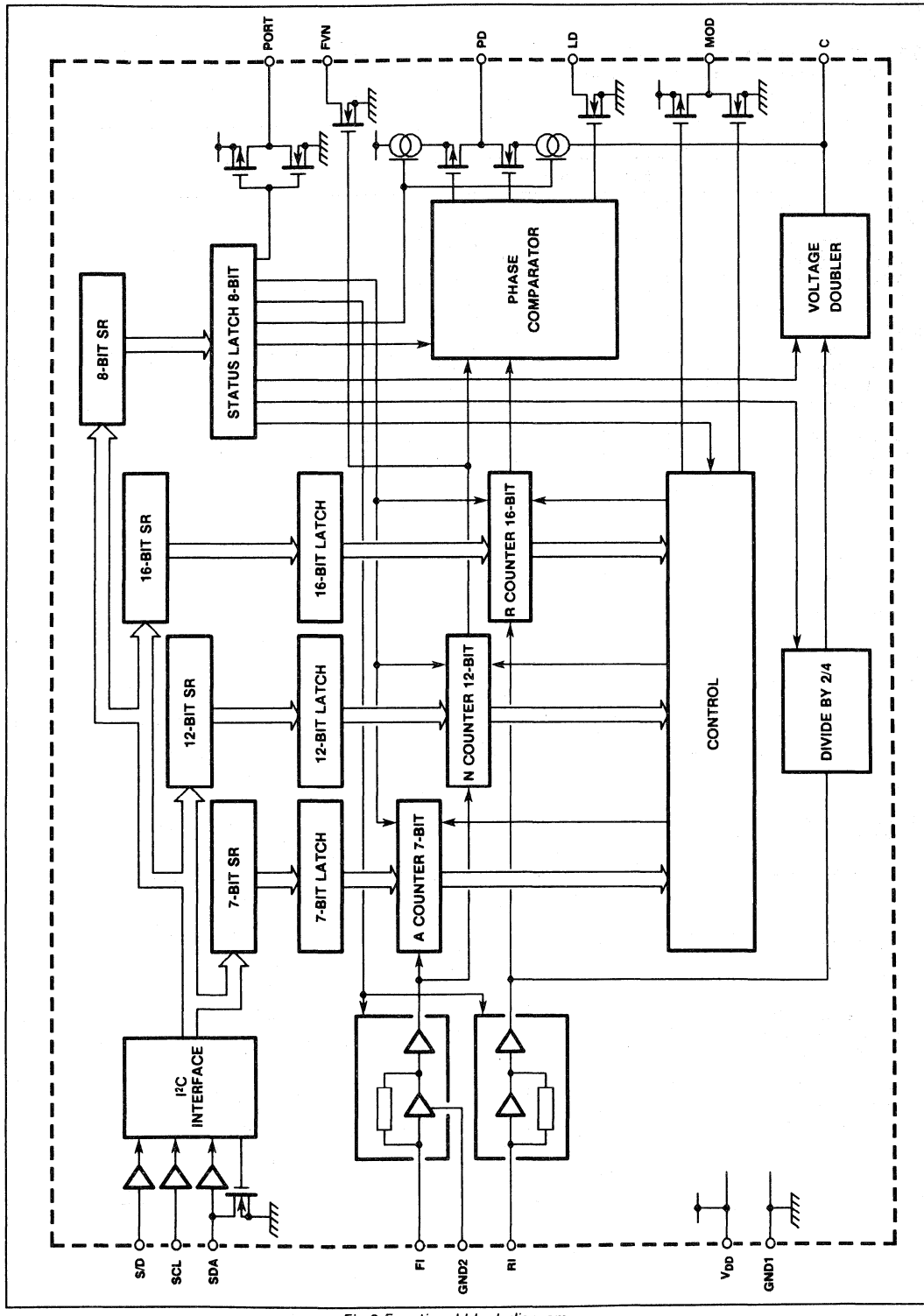


Fig.3 Functional block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} = 4.5V to 5.5V, T_{amb} = -40°C to +85°C

INPUT SIGNALS

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Input Signals SDA, SCL, S/D						
Input voltage high	V_{IH}	$0.7V_{DD}$		V_{DD}	V	
Input voltage low	V_{IL}	0		$0.3V_{DD}$	V	
Input capacitance	C_I			10	pF	
Input current	I_{IN}			10	μA	$V_{IN} = V_{DD} = 5.5V$
Input Signal RI						
Input frequency	f_{max}			50	MHz	V_{DD} = 4.5V, sinewave input
Input voltage	V_{Irms}	100			mV	
Input capacitance	C_I			10	pF	
Input current	I_{IN}			10	μA	$V_{IN} = V_{DD} = 5.5V$
Input Signal FI						Dual modulus operation
Input frequency	f_{max}			50	MHz	V_{DD} = 4.5V, sinewave input
Input voltage	V_{Irms}	50			mV	
Input capacitance	C_I			10	pF	
Input current	I_{IN}			10	μA	$V_{IN} = V_{DD} = 5.5V$
Input Signal FI						Single modulus operation
Input frequency	f_{max}			120	MHz	V_{DD} = 4.5V, sinewave input
Input voltage	V_{Irms}	10			mV	
Input capacitance	C_I			10	pF	
Input current	I_{IN}			10	μA	$V_{IN} = V_{DD} = 5.5V$

OUTPUT SIGNALS

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Output Signals SDA, LD						
Output voltage low	V_{OL}			0.4	V	Open drain, I_{OL} = 3mA
Output Signal PD						C_L = 400pF, tristate output
High current mode (see Fig.4)	I_{HU}	+1.9	+2.5	+3.1	mA	$-5 < V_{PD} < 4.75$, V_{DD} = 5V
	I_{HD}	-1.9	-2.5	-3.1	mA	$-4.8 < V_{PD} < 5$, V_{DD} = 5V
Low current mode	I_{LU}	+0.475	+0.625	+0.775	mA	$-5 < V_{PD} < 4.75$, V_{DD} = 5V
	I_{LD}	-0.475	-0.625	-0.775	mA	$-4.8 < V_{PD} < 5$, V_{DD} = 5V
Tristate	I_Z		50		nA	T_{amb} = -25°C to +60°C
Output Signal FVN						Open drain output
Output voltage low	V_{OL}			0.4	V	I_{OL} = 1mA
Output low pulse width	t_{WL}			1/FI		C_L = 30pF
Output Signals MOD, PORT						Push-pull output
Output voltage high	V_{OH}	V_{DD}-0.4			V	I_{OH} = 0.5mA
Output voltage low	V_{OL}			0.4	V	I_{OL} = 0.5mA
Output Signal LD						Open drain output
Output voltage low	V_{OL}			0.4	V	I_{OL} = 3mA, CL = 30pF
Output low pulse width	t_{WL}		10	1/FVN	ns	Loop locked
				$1/f_C$		Loop not locked
						FVN = FI/N
						f_C = RI/R

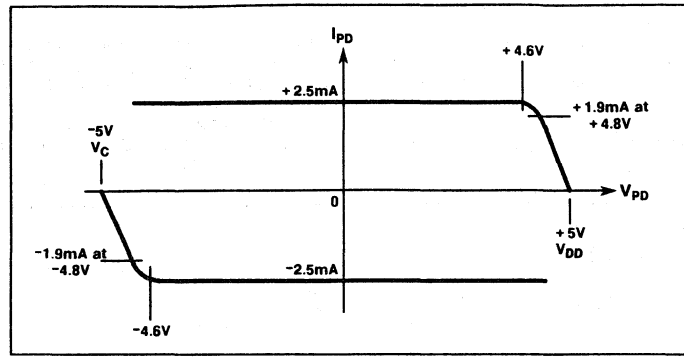


Fig.4 Output signal PD, high current mode, V_{DD} = 5V

VOLTAGE DOUBLER

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Output Pin C						
Output voltage	V_C	$-V_{DD}$		$-V_{DD}+0.8V$	V	f_{VD} = 2MHz, I_{OC} = 0μA, V_{DD} = 5V
	V_C	$-V_{DD}$		$-V_{DD}+1.5V$	V	f_{VD} = 2MHz, I_{OC} = 100μA, V_{DD} = 5V
	V_C	$-V_{DD}$		$-V_{DD}+0.8V$	V	f_{VD} = 2MHz, I_{OC} = 0μA, V_{DD} = 3V
	V_C	$-V_{DD}$		$-V_{DD}+1.5V$	V	f_{VD} = 2MHz, I_{OC} = 100μA, V_{DD} = 3V
Current Consumption						
	I_D			100	μA	f_{VD} = 2MHz, I_{OC} = 0μA, V_{DD} = 5V
	I_D			100	μA	f_{VD} = 2MHz, I_{OC} = 0μA, V_{DD} = 3V

TIMING INFORMATION

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Input Signal RI						Pulse
Input frequency	f_{max}			50	MHz	V_{DD} = 4.5V
Rise time	t_R	1			ns	
Fall time	t_F	1			ns	
Pulse width	t_W	3			ns	
Input Signal FI						Dual modulus, pulse
Input frequency	f_{max}			50	MHz	V_{DD} = 4.5V
Rise time	t_R	1			ns	
Fall time	t_F	1			ns	
Pulse width	t_W	3			ns	
Input Signal FI						Single modulus, pulse
Input frequency	f_{max}			120	MHz	V_{DD} = 4.5V
Input frequency	f_{max}			50	MHz	V_{DD} = 3V
Rise time	t_R	1			ns	
Fall time	t_F	1			ns	
Pulse width	t_W	3			ns	
Output Signal PORT						
Rise time	t_R			1	μs	C_L = 30pF
Fall time	t_F			1	μs	C_L = 30pF
Output Signal FVN						
Fall time	t_F		20		ns	C_L = 30pF
Output Signal MOD						
Rise time	t_R			10	ns	C_L = 30pF
Fall time	t_F			10	ns	C_L = 30pF
Delay time (L→H on FI)	t_{DLH}			25	ns	C_L = 30pF
Delay time (H→L on FI)	t_{DHL}			15	ns	C_L = 30pF

PHASE COMPARATOR

The phase comparator produces current pulses of duration equal to the difference in phase between the comparison frequency ($f_C = RI/R$), and f_{VN}, the divided-down VCO frequency (FI/N).

When status bit 4 is set high the positive polarity mode of the output PD is selected. When f_C leads f_{VN} the PD output goes high; when f_{VN} leads f_C it goes low. Similarly, selecting the negative polarity mode of PD by programming bit 4 of the status register low causes PD to have the inverse polarity. The loop filter integrates the current pulses to produce a voltage drive to the VCO. No pulses are produced when locked. The lock detect output, LD, produces a logic '0' pulse equal to the phase difference between f_C and f_{VN}.

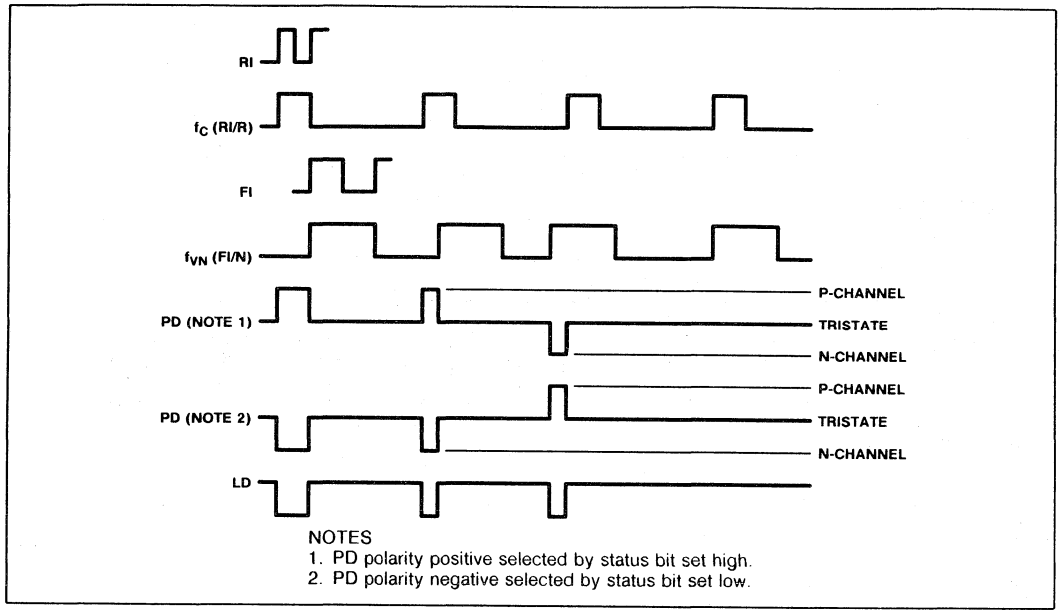


Fig.5 Phase comparator phase diagram

PROGRAMMING

Transmission Protocol

I²C programming messages consist of an address byte followed by a sub-address byte followed by 1, 2 or 3 bytes of data. Bit 7 of the address byte must match the setting of the S/D pin for the address to be recognised. This allows for separate addressing of two NJ88C33 synthesisers on the same bus. The sub-address should be set to select the correct registers to be programmed and should be followed by the appropriate number of data bytes. Registers are not programmed until the complete message protocol has been checked.

Each message should commence with a START condition and end with a STOP condition unless followed immediately by another transfer, when the STOP condition may be omitted.

Data is transferred from the shift register to the latches on a STOP condition or by a second START condition.

A START condition is indicated by a falling edge on the Serial Data line, SDA, when the Serial Clock line, SCL, is high.

A rising edge on SDA when SCL is high indicates a STOP condition as shown in Fig.6.

Data on SDA is clocked into the NJ88C33 on the rising edge of SCL. The NJ88C33 acknowledges each byte transferred to it by pulling the SDA line low for one cycle of SCL after the last bit has been received.

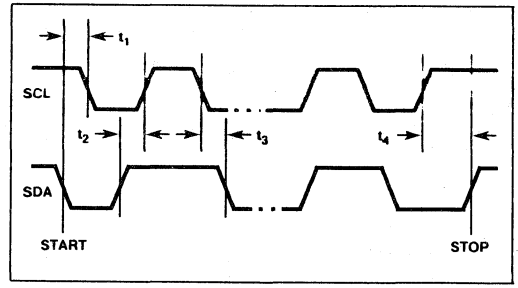


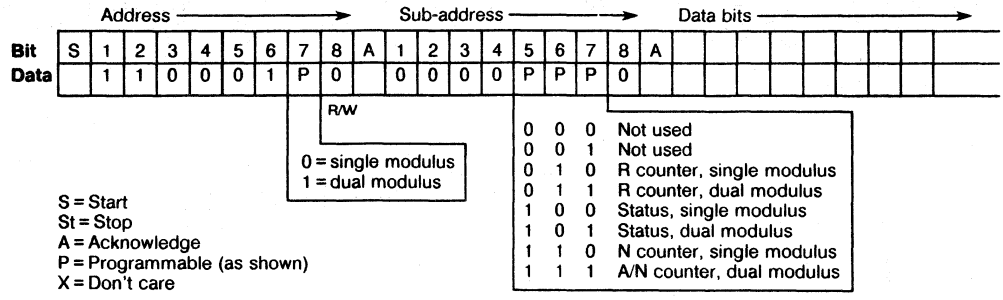
Fig.6 I²C timing diagram

I²C TIMING INFORMATION

Parameter	Symbol	Value		Unit
		Min.	Max.	
Serial clock frequency	f_{SCL}		2	MHz
SCL hold after START	t_1	20		ns
Data set-up time	t_2	20		ns
Data hold after SCL low	t_3	0		ns
SCL set-up before STOP	t_4	20		ns

Address and Sub-Address Formats

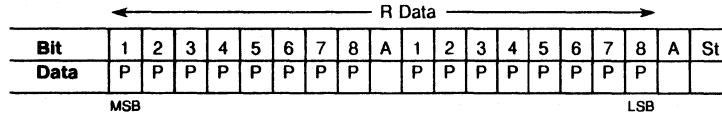
The correct addressing sequence for the NJ88C33 is shown below. The START condition is followed by the address byte, the acknowledge from the NJ88C33, the sub-address byte, another acknowledge then the associated data. The correct values for each address and sub-address are listed, together with the message selection options.



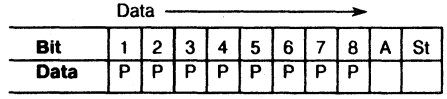
Data Formats

Each of the data formats should be preceded contiguously by the addressing sequence given above.

R counter : single or dual modulus



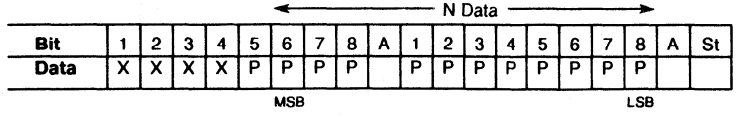
Status : single or dual modulus



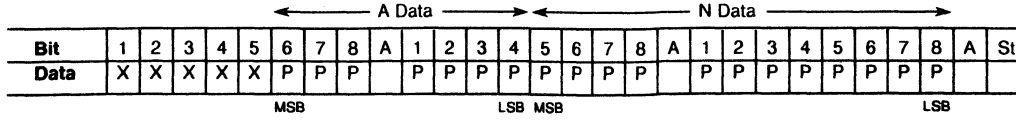
Status Byte		
Bit	**0**	**1**
1	PORT = low	PORT = high
2	Counters off (1)	Counters on
3	FI and RI off (2)	FI and RI on
4	PD = polarity negative	PD = polarity positive
5	PD bias = 0.625mA	PD bias = 2.5mA
6	f_{VD} = RI/2	f_{VD} = RI/4
7	Doubler off	Doubler on
8	MOD = push-pull	MOD = open drain

NOTES
1. In this standby mode the counters are disabled but the voltage doubler and I²C interface can both function.
2. In this standby mode the FI and RI preamplifiers are disabled, which stops the counters and the voltage doubler. The I²C interface still operates.

N counter : single modulus



A/N counters : dual modulus



APPLICATION CIRCUITS

Single Modulus

In this mode, the NJ88C33 synthesiser can be used with or without a fixed modulus prescaler. The R counter is programmed with a value to produce a comparison frequency f_C. When the N counter is changed by 1 the loop is no longer in lock and the phase detector output produces current pulses to bring the loop back into lock. These pulses are integrated by the loop filter to produce the VCO voltage drive. When the VCO loop is locked, $FI/N = f_C$ i.e., the VCO frequency is $N \times f_C$.

Using a prescaler with a division ratio P, the smallest VCO output frequency step is Pf_C and the VCO frequency is PNf_C.

If a low pass filter is connected to the lock detect output as shown and sampled by the microprocessor, the proximity of the synthesiser loop to lock can be evaluated.

The A counter is not used in this mode.

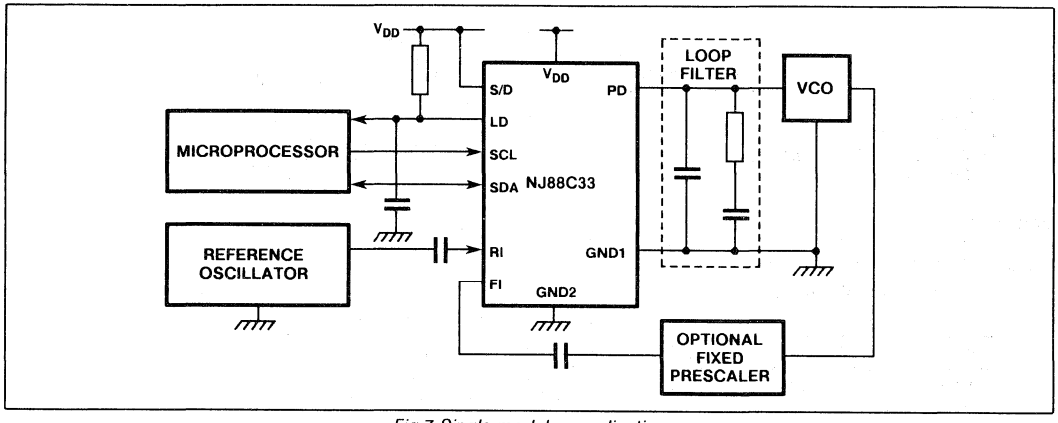


Fig.7 Single modulus application

Dual Modulus

This mode allows much higher frequencies to be used in conjunction with a prescaler but maintains the step size, f_C. In this mode, a dual modulus prescaler (with ratios P and P + 1) must be used with the NJ88C33. The A counter controls the MOD output, which is used to select the division ratio of the prescaler.

When the A counter is non-zero, the MOD output is low and goes high when the A counter has counted down to zero. MOD remains high until the N counter reaches zero, when both counters are re-loaded. Thus, the prescaler divides by P for N-A cycles and by P + 1 for A cycles of f_C. The VCO frequency is given by $PNf_C + Af_C$.

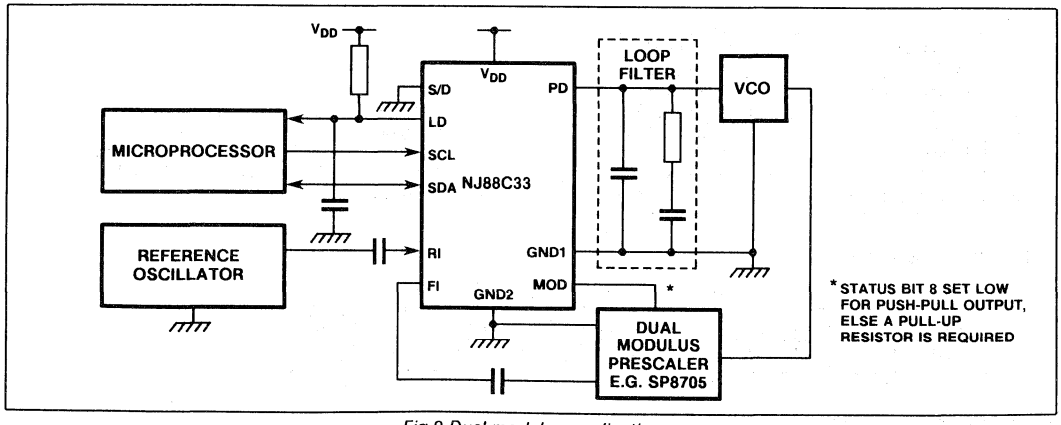


Fig.8 Dual modulus application

VCO Driving Without Voltage Doubler

To switch off the voltage doubler, bit 7 of the status register is programmed low. This will reduce current consumption and minimise noise. The voltage doubler output C should be connected to GND1 as connection to GND2 would induce noise in the VCO loop.

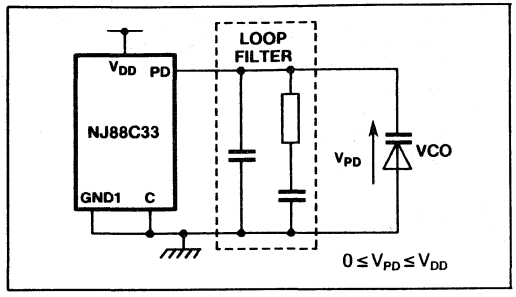


Fig.9 Driving a VCO without voltage doubler

VCO Driving With Voltage Doubler

The voltage doubler is switched on by setting bit 7 of the status register high. It is recommended that a reservoir capacitor of at least 1μF be connected from C to GND1.

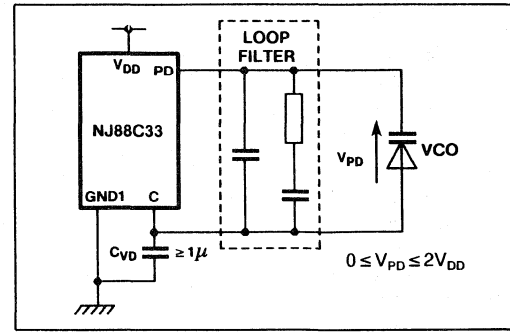


Fig.10 Driving a VCO using the voltage doubler

Further Applications Information

A stand-alone programmer card and an evaluation board are available for evaluating the NJ88C33. The programmer card allows two sets of variables to be programmed into both the divider and status registers during alternate programming cycles, at either the standard I²C bus rate of 100kHz or at the NJ88C33's maximum clock rate of 2MHz.

Initialisation is with either a manual push-button or by an external logic level pulse; a synchronisation output is provided to allow a quick assessment of 'step' and 'settle' responses to be made.

The NJ88C33 evaluation board (Fig. 11) demonstrates the preferred layout technique - providing a reference oscillator, a 60 to 120MHz VCO and a simple loop filter to complete a minimal frequency synthesiser loop. The two units allow analysis of different loop variables as well as the selection of comparison frequencies for fast frequency-hopping loops.

Application Note: AN-94, *'Using the NJ88C33 PLL Synthesiser'* explains the design equations and demonstrates the use of the device.

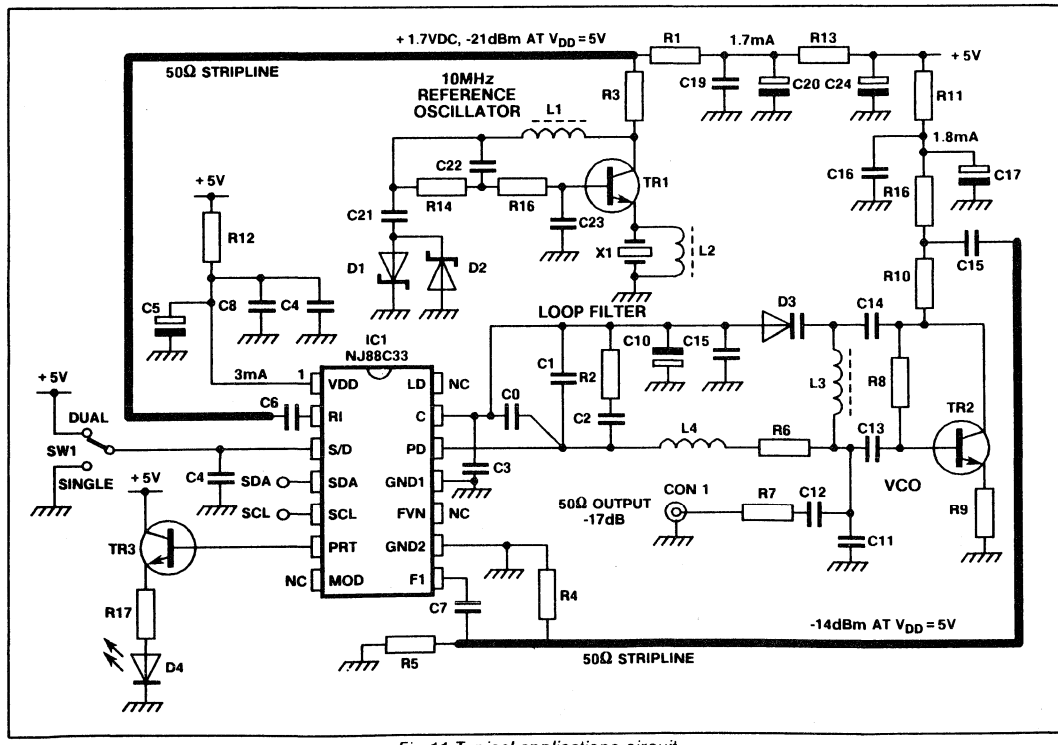


Fig.11 Typical applications circuit

COMPONENT LIST FOR FIG.11

Capacitors				Resistors		Inductors		Miscellaneous	
C0	1nF 10%	C17	22μF/35V Elect.	R1	56Ω	L1	15μH 10%	IC1	NJ88C33
C1	100nF 10%	C18	1nF 10%	R2	1.8kΩ	L2	220μH 10%	X1	10.00MHz 20ppm
C2	1nF Tant.	C19	1nF 10%	R3	560Ω	L3	470nH 20%	SW1	Miniature slide switch
C3	1nF 10% NPO	C20	22μF/35V Elect.	R4	100Ω	L4	470μH 10%	CON1	SMC socket
C4	1nF 10%	C21	10nF 10%	R5	100Ω				
C5	22μF/35V Elect.	C22	4.7nF 10%	R6	1kΩ	**Diodes**			
C6	4.7nF 10%	C23	47pF 5% NPO	R7	120Ω				
C7	1nF 10%	C24	22μF/35V Elect.	R8	47kΩ	D1	1N6263 Schottky		
C8	1nF 10%			R9	10Ω	D2	1N6263 Schottky		
C9	1nF 10%			R10	1.8kΩ	D3	BBY40 varicap		
C10	2.2μF/35V Tant.			R11	10Ω	D4	5mm red LED		
C11	330pF 5% NPO			R12	10Ω				
C12	1nF 10%			R13	10Ω	**Transistors**			
C13	1nF 10%			R14	47kΩ				
C14	1pF ±0.5pF NPO			R15	2.7kΩ	TR1	BFS17 RF NPN		
C15	22pF 5% NPO			R16	100Ω	TR2	BFS17 RF NPN		
C16	1nF 10%			R17	100Ω	TR3	2N3904 Switching		

NOTES
1. With the exception of electrolytics, all capacitors are surface mount types
2. All resistors are 0.25W, ±2%
3. C0, C1, C2, C11, C12, C13 and C14 must be low leakage types.

PLESSEY
Semiconductors

PRELIMINARY INFORMATION

SL6670-1

LOW VOLTAGE DC/DC VOLTAGE CONVERTER

(Supersedes February 1988 edition)

The SL6670-1 is a novel bipolar monolithic voltage multiplier designed to operate from supply voltages as low as 1.1V.

Voltage tripling uses a capacitor pump technique and no external inductor is required.

Full load regulation is provided and the output can be preset to the desired voltage.

The SL6670-1 also incorporates a battery flag monitor.

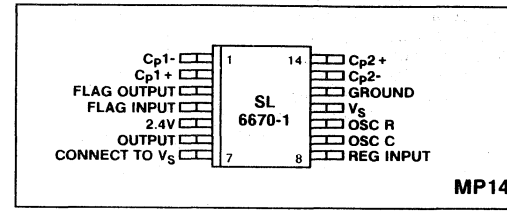


Fig.1 Pin connections - top view

FEATURES

- High Power Efficiency
- 1.1V to 5V Operation
- No Inductors Required
- Low Radiation
- Surface Mount Plastic Package

APPLICATIONS

- Radio Pager Power Supplies
- Memory Back-up Supplies
- High Efficiency Battery Powered DC/DC Converters

ORDERING INFORMATION

SL6670-1 NA MP

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+8V
Storage temperature	-55°C to +125°C

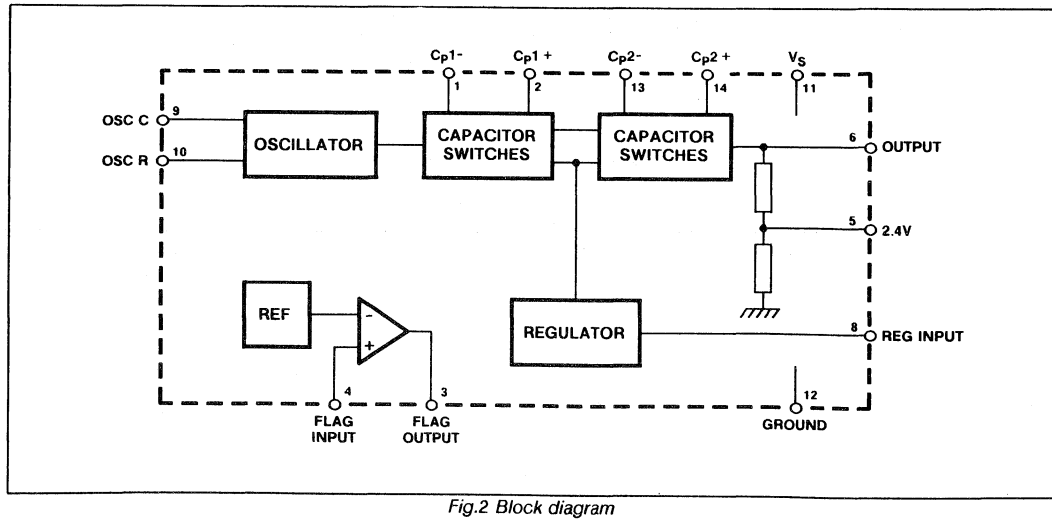


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = +25°C, V_{OUT} (nominal) = 3.0V, f_{CLOCK} = 3kHz (approx.), V_S = 1.50V

Characteristic	Pin No.	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage range	11	1.10		5.0	V	-10°C to +40°C
Supply current	11		250	350	μA	I_L = 0
Output voltage	6	2.75	3.0	3.25	V	I_L = 0
Output current	6	1.150			mA	
		0.80			mA	V_S = 1.10V
Operating frequency range	9,10			10	kHz	
Load regulation	6		-0.150	-0.250	V	I_L = 0 to 1.15mA
				-0.30	V	V_S = 1.10V, I_L = 0 to 0.8mA
Regulator input reference voltage	8		0.70		V	
Flag reference voltage	4		0.70		V	
Flag output high voltage	3	70			% V_S	
Flag output low voltage	3			30	% V_S	
Fixed output voltage option	6	2.250		2.650	V	
Change in V_0 with temperature (note 1)	6		+0.175		V	-10°C to +40°C, I_L = 0

NOTE

1. Ultimately depends on circuit configuration, load current and V_S.

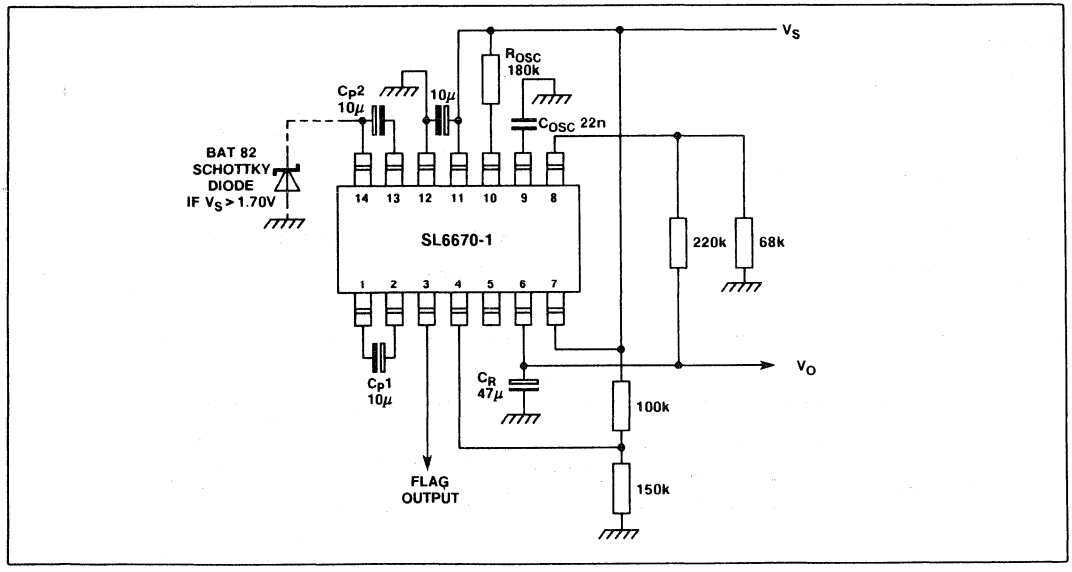


Fig.3 Test circuit

PIN DESIGNATIONS

Pin No.	Description
1	**C_P1-.** Negative terminal of charge pump capacitor 1.
2	**C_P1 +.** Positive terminal of charge pump capacitor 1.
3	**Flag output.** This output is low when pin 4 is lower than the flag reference.
4	**Flag input.** Pin 3 output will be low when this pin is below the flag reference.
5	**2.4V nominal.** Tying this pin to the regulator input (pin 8) will set the output to nominally 2.4V.
6	**Output, V_O.** This pin drives the reservoir capacitor, C_R, and can be adjusted to any voltage between 0.9V and 5V.
7	**Connect to V_S (pin 11)**
8	**Regulator input.** The output voltage on pin 6 is set by an external resistive divider connected from pin 6 to pin 8 and ground. The regulator will keep this pin at 0.7V. Tying pin 8 to pin 5 will regulate the output at 2.4V.
9	**Oscillator capacitor, C_{OSC}.** A capacitor is connected from this pin to ground and determines the oscillator frequency.
10	**Oscillator resistor,R_{OSC}.** A 180kΩ resistor connected from this pin to V_S (pin 11) is required.
11	**Supply/battery voltage, V_S.** 1.1V to 5V.
12	**Ground.**
13	**C_P2-.** Negative terminal of charge pump capacitor 2.
14	**C_P2. +.** Positive terminal of charge pump capacitor 2. A Schottky diode is required to be connected from this pin to ground if V_S is greater than 1.7V.

PRINCIPLE OF OPERATION

Because of the low input voltage, the SL6670-1 uses a two-stage pump circuit, using external pump capacitors, which will provide up to three times the supply voltage at the output reservoir capacitor. A regulator is provided to enable the output to be set at any voltage below this tripled output.

The operation of the device can best be described by considering Fig. 4, which shows an idealised voltage tripler. Switches S1 are closed for half the clock cycle, with switches S2 open. In the next clock half-cycle, switches S2 are closed and switches S1 open. With switches S1 closed, the capacitors charge up towards V_S. When switches S2 close, the charged capacitors are stacked one above the other onto V_S, giving a maximum output of $3V_S$.

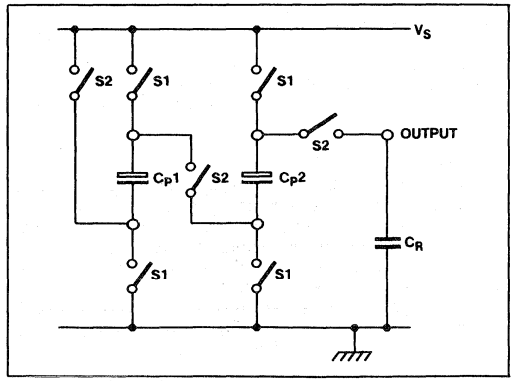


Fig.4 Voltage tripler equivalent circuit

GENERAL DESCRIPTION

Regulator

The regulator uses a charge control method to charge the pump capacitors sufficiently to keep the reservoir capacitor at a defined voltage regardless of load, thus achieving current and voltage regulation. The regulated output voltage is selected by providing a feedback voltage to the regulator input pin using an external resistive divider. Alternatively, a preset 2.4V nominal output pin is provided to minimise external components.

Oscillator

The clock is provided by an on-chip oscillator, the frequency of which can be selected by choosing appropriate R and C values.

Flag Circuit

A flag circuit is included which can be used to signal that the output has dropped below a preset level. Hysteresis can be provided with a feedback resistor. The flag circuit can also be used to check the battery supply if desired.

EXTERNAL COMPONENTS

Oscillator Resistor and Capacitor

The resistor value determines the amount of hysteresis in the oscillator and should be 180kΩ for correct operation. The capacitor value, which will depend on the frequency of operation required, can be calculated as follows:

$$C_{OSC} = \frac{26}{f}$$

where C is in μF and f is in Hz.

Pump Capacitors

The pump capacitors C_P store the pumping charge before it is transferred to the reservoir capacitor C_R. For the regulator to maintain optimum efficiency, the pump capacitors must be equal in value. The pump capacitor value is chosen to ensure the droop voltage ΔV_P is acceptable.

$$\Delta V_P = \frac{I_{LOAD}}{fC_P}$$

The magnitude of $\Delta V_P$is chosen considering the worst case input-output voltage expected:

$$\Delta V_P < \frac{[3V_S - V_O]}{2}$$

where ΔV_P is droop voltage on each capacitor.

If this consideration is not met, the output will fall out of regulation.

Reservoir Capacitor

The reservoir capacitor C_R integrates the ripple at the output. To reduce the ripple ΔV_O the reservoir capacitor must be of the correct value:

$$\Delta V_O = \frac{I_{LOAD}}{2C_R f}$$

where f is the clock frequency in Hz.

Schottky Diode

A Schottky diode is required from pin 14 to ground if V_S exceeds 1.7V. This protects the chip should the output be short circuited. If the diode is not present, the device will remain in a non-destructive latched state; removing the supply will restore normal operation. The inclusion of the diode will not affect the device operation and no change in device specification is required; the diode only acts as a catching diode under fault conditions and carries no current under normal operation.

CONSIDERATIONS FOR HIGH EFFICIENCY

Frequency

The efficiency of the SL6670-1 is dependent on the oscillator frequency. As the oscillator frequency is increased the switching losses increase, so lowering the efficiency.

Pump Capacitors

The regulator controls the amount of charge transfer assuming that both pump capacitors have the same charge characteristic. Therefore, for optimum efficiency, the pump capacitors should have the same value. To obtain optimum efficiency, the value of pump capacitors must be chosen so that the regulator is always in regulation.

Reservoir Capacitor

The reservoir capacitor must be chosen to reduce the output ripple. For optimum efficiency, the regulator must see a signal at its inputs which has no large ripple component.

Regulator

The regulator will control the output voltage to any level between 0.9V and 5V, depending on the value of V_S. The control range in any application is set by V_S but the SL6670-1 wil not necessarily be efficient at all settings of output voltage.

When the output voltage is set close to V_S, there is a limit to the amount of charge that can be transferred from the pump capacitors to the reservoir capacitor and so efficiency will fall. When the output is set close to $3V_S$ ($V_{O\ max.} = 5V$), the charge transfer may be insufficient, due to internal voltage drops, to achieve the required output. The regulator will attempt to drive the output higher than is possible, by driving large currents into the switches, even with no load current. This will reduce the efficiency near the upper limit of the regulator.

DESIGN EXAMPLE

2.4V Supply from a Single Alkaline Cell, for use in a Radio Pager

A major use of the SL6670-1 is in providing a voltage supply suitable for operating CMOS circuits from battery voltages down to 1.1V. The battery voltage can vary from 1.7V when new to 1.1V when exhausted, so the maximum output open circuit voltage is 3.3V when the battery voltage falls to 1.1V. A good choice of output voltage would be 2.4V because this enables the on-chip potential divider to be used.

The choice of frequency is dependent on the ripple requirement and capacitor values.

With a 3kHz clock frquency, the maximum droop voltage that can be allowed is:

$$\frac{[3V_S - V_O]}{2} = 450mV$$

Using a load of 1mA and 10μF capacitors for C_P:

$$\frac{I_{LOAD}}{fC_P} = 33mV \text{ droop voltage}$$

This is well below the 450mV and is an acceptable value.

Using a 47μF reservoir capacitor will give:

$$\frac{I_{LOAD}}{2C_R f} = 3.5mV \text{ output ripple}$$

Since the maximum supply voltage is 1.7V, a Schottky diode will not be required.

TYPICAL APPLICATIONS

Simple Positive Voltage Converter

A typical application of the SL6670-1 in a simple positive voltage converter is shown in Fig. 5. The 2.4V output is obtained by connecting pin 5 to pin 8, using on-chip resistors and so reducing the external component count.

External Clocking of SL6670-1

In some applications it may be advantageous to externally control the internal oscillator. This can be achieved as shown in Fig. 6.

Paralleling SL6670-1s

Any number of SL6670-1 voltage converters may be connected in parallel to increase output current capability, as shon in Fig. 7. The reservoir capacitor, pump capacitors and oscillator components serve all devices. Individual components could be used for the oscillator and pump capacitors on each device if required.

C_{OSC} should be doubled when paralleling two devices for the same operating frequency. R_{OSC} should be adjusted (to maintain the same DC conditions).

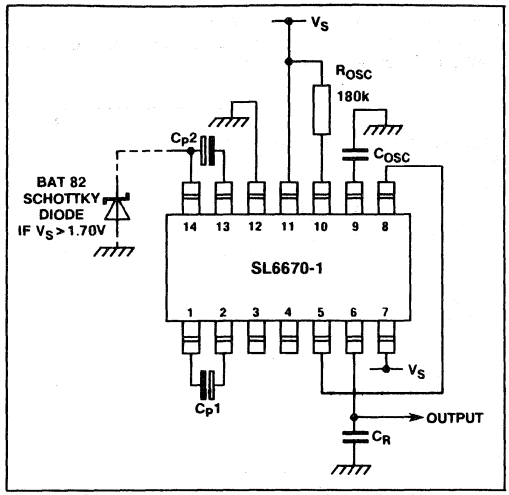


Fig.5 Simple positive converter with fixed 2.4V output

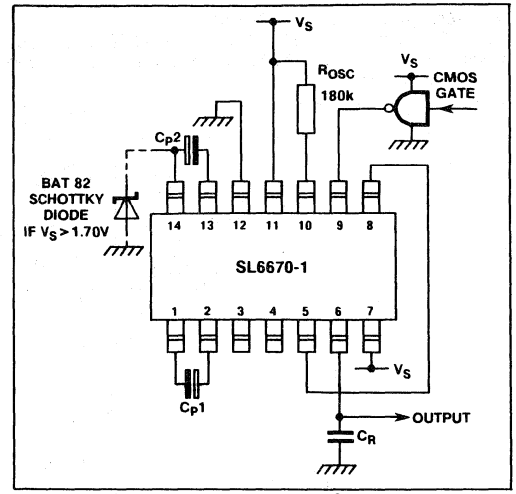


Fig.6 External clocking of SL6670-1

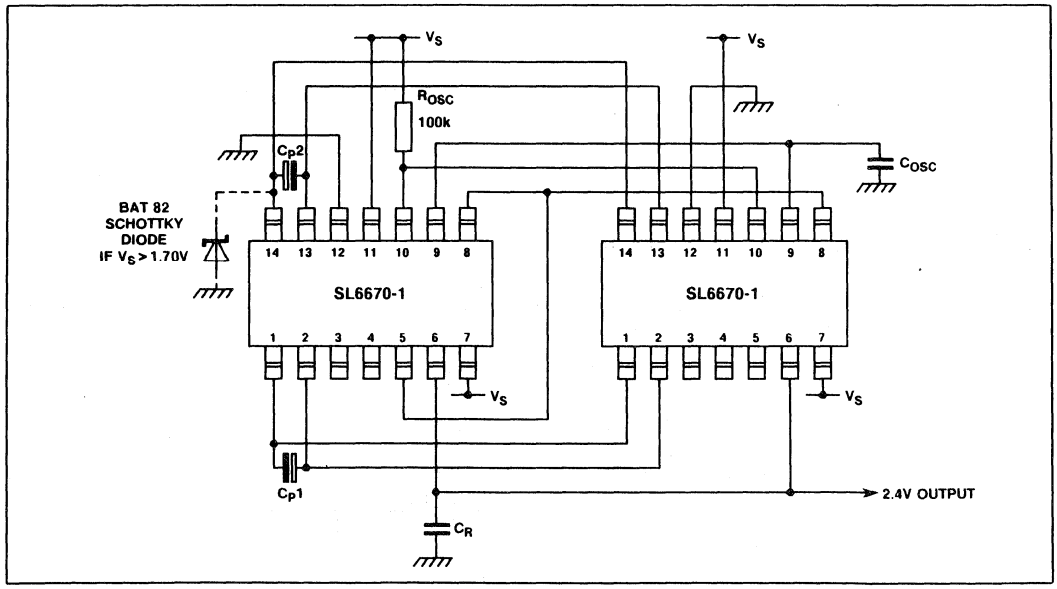


Fig.7 Paralleling SL6670-1s with fixed 2.4V output

Uninterruptible Memory Supply

Fig. 8 shows the SL6670-1 being used as a standby memory supply. The battery flag senses when the battery is nearly discharged.

Remote Sensing for Regulator

The input to the regulator can be used for remote sensing applications, as shown in Fig. 9.

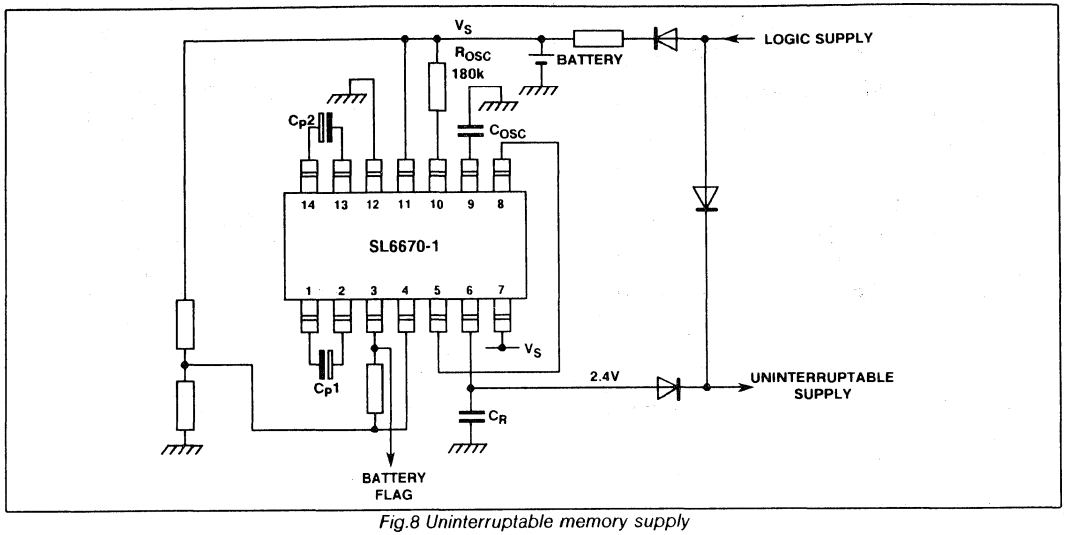


Fig.8 Uninterruptable memory supply

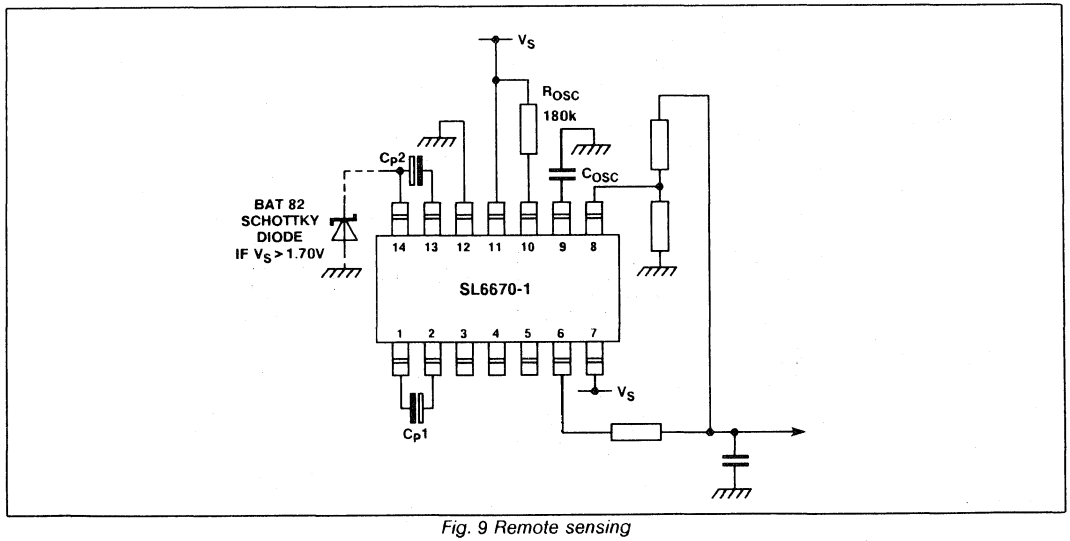


Fig. 9 Remote sensing

Separate Regulator Decoupling

In applications where high output ripple can be tolerated, the regulator can be separately decoupled with a small capacitor as shown in Fig. 10. In applications where large load glitches appear on the output, a more complex smoothing network can be incorporated between the output, pin 6, and pin 8 or, for fixed 2.4V output, between pin 5 and pin 8.

A 3V Battery to 5V Logic Supply

Fig. 11 shows the SL6670-1 used to provide a 5V supply from a 3V battery. The circuit continues to work even when the battery is exhausted at 1.8V. The battery flag will sense when the battery is exhausted.

R1 and R2 set the voltage at which the flag is required to switch and R_F sets the value of hysteresis required.

R3 and R4 set the regulated output voltage. In normal operation, 0.7V will appear across R4 and V_O-0.7V will appear across R3.

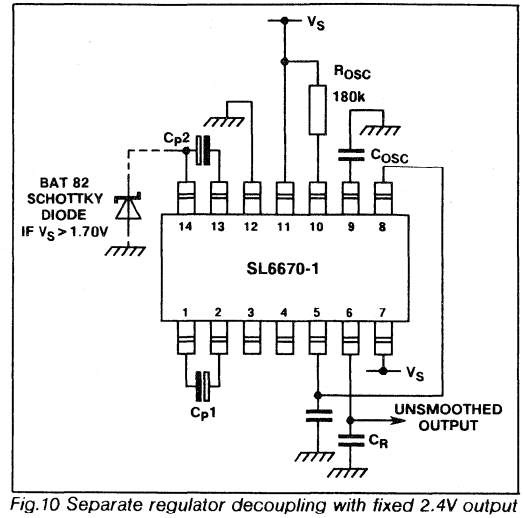


Fig.10 Separate regulator decoupling with fixed 2.4V output

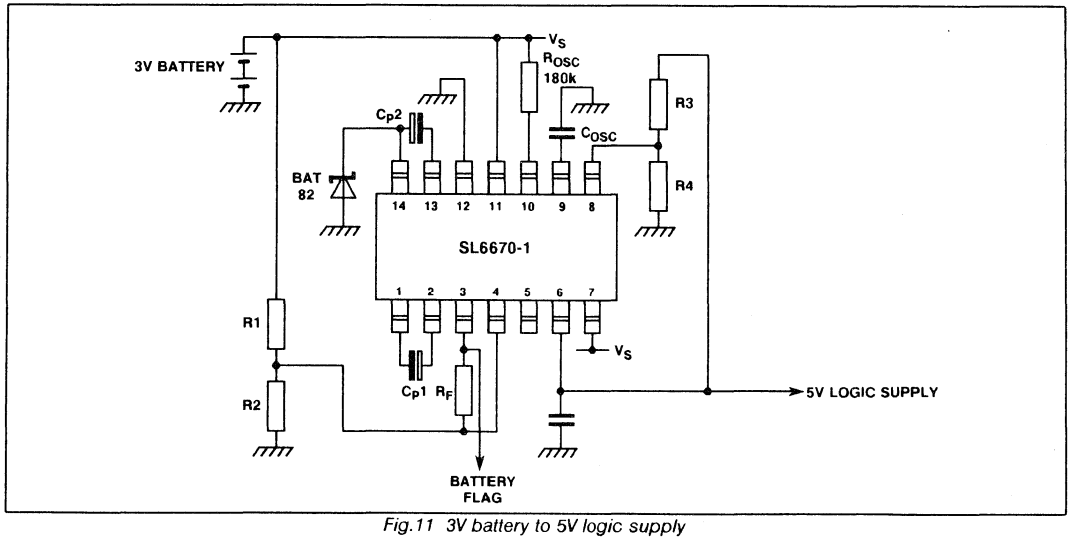


Fig.11 3V battery to 5V logic supply

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